Column-Parallel Dual-Slope Integrating ADC

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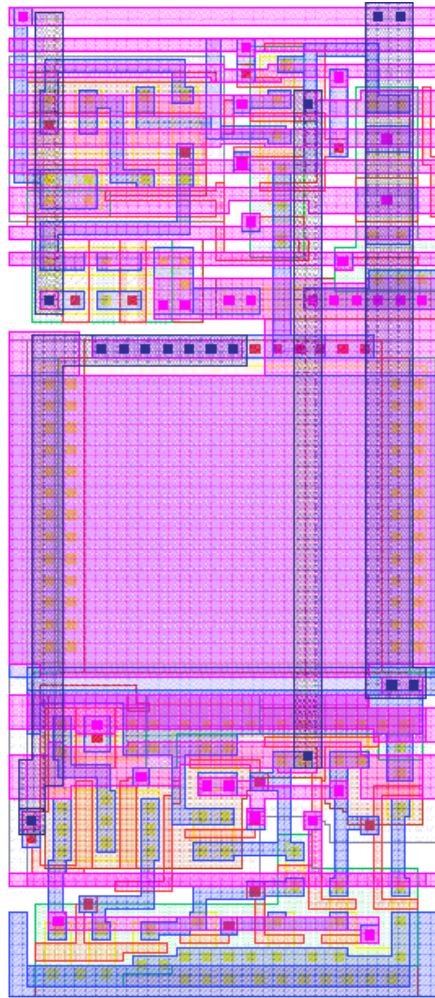
A single ADC cell (no control or bias circuitry)

Objectives

A column-parallel analog-to-digital converter was designed for use with CMOS active pixel sensors (APS). The design goals included simplicity, small size, moderate speed (>10kHz), current input, and reasonable accuracy (6-bits). The ADC was designed to get a rough digital output from pixels that serve some other primary function (image quality sensing, stereo vision, etc.).

Specifications

The ADC was designed with a current input. This greatly decreases the area necessary to implement the ADC; a dual-slope ADC with a voltage input (from a high impedance source) requires a transconductance amplifier in order to integrate the voltage over time. The ADC works in three steps. During the first step switch S1 is turned on, resetting the capacitor to a known, fixed voltage. Switch S1 is then turned off. During the second step switch S2 is turned on for a fixed time period. The change in voltage on the capacitor is then directly proportional to the input

current (which is assumed to be constant over the integration time). During the third step the capacitor is discharged with a known reference current I2. The time taken for the capacitor to reach the original reference voltage V1 is then directly proportional to the input current. This time is independent of the value of capacitor C1 (ignoring non-idealialities is the current sources). The cycle then repeats again. A more detailed schematic and layout can be seen in the appendix.
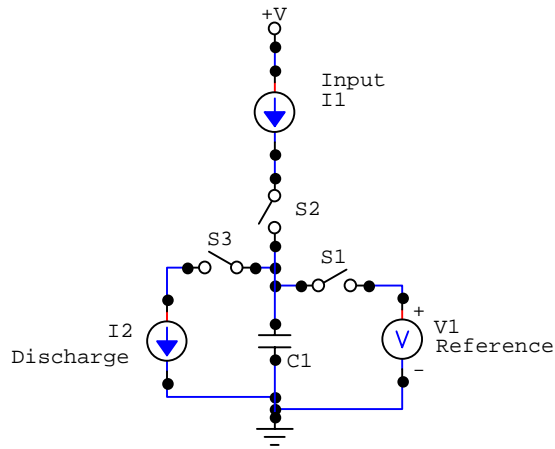

Figure 1: Functional Diagram of the Dual-Slope ADC

The voltage on the capacitor is compared against the reference voltage using a latched comparator (the layout and schematic are shown in the appendix) [1]. The comparator is clocked 64 times (representing 6 bits) during the discharge cycle. The number of latches needed before a high output is reached represents the output value of the ADC. The design required only a comparator, a capacitor (implemented as a PFET capacitor), two current mirrors, and several switches. As much of the necessary circuitry was separated from the single ADC as possible, such that N ADCs may share one counter, a bias circuit for the comparator's current source, and a bias circuit for the discharge circuit. This enabled the single ADC cell to be only 228 x 99λ^2. The ADCs were designed to abut such that *N* ADCs take 228 x (*N* x 99)λ^2 of area.

The reference current is produced by a cascode mirror, whose current is controlled by a β-multiplier reference (see schematic and layout appendix) [2]. The input current was mirrored using cascode mirrors, allowing the circuit to operate on sources with lower output impedance than would be possible if the input current were directly integrated.

The control circuitry was designed to accept two inputs: a clock (*T*=48ns) and a reset signal. The reset signal must be held high for at least one clock period at power up. After the initial reset the control circuitry generates all of the necessary non-overlapping clocks. The central component of the control circuit is the 6 bit counter; this counter counts upwards (incrementing from 0 to 63, with the next increment going to 0) for three full cycles (reset, charge, and discharge) for each conversion. The control circuit schematic and layout are shown in appendix. A single counter bit-slice (schematic and layout) can also be seen in the appendix.

Compliments were required for the main clock, the charge clock, and the reset clock. These were generated using a non-overlapping clock generation circuit, shown in appendix.

Currently the chip does not store the converted values produced by the ADC. The output value is the value of the counter when the comparator first outputs a high pulse. Future improvements could include a 6-bit latch for each ADC to allow for storage of the digital output. An output multiplexer could allow hundreds of ADCs to fit on a single 2.25mm^2 MOSIS "TinyChip".

The ADC was designed for fabrication on the AMI C5N 0.5μm process (λ=0.6μm). The area used by 8 ADC cells and the control circuitry was 2350 x 260λ^2 (excluding output buffers). While the ADC layout was optimized for minimum area and for pitch matching, the control circuitry's layout was not fully optimized; future improvements could yield significant area reductions in the control circuitry. A pad driver was designed using four series inverters (each having a β$_n$ and a β$_p$ of about *e* times greater than the previous inverter).

The circuit's pinout is shown in the table below. [The circuit has not yet been fully connected to the padframe, so the pinout described below is tentative.] Currently the ADCs continue to produce high pulses after the pulse indicating the conversion value. These pulses must be ignored; future improvements to the circuit will gate the pulses, such that only one output pulse is produced for each conversion. The lack of an output pulse for each conversion indicates an input "overflow," a current that is beyond the conversion scale (of 0-346nA). Prior to fabrication, analog buffers will be designed to buffer the voltage on the ADC capacitors so that they can be measured from a pin (for debugging purposes). Internal decoupling capacitors were added to the three internally-generated reference voltages (one for the comparator bias current, two for the discharge current).

Padframe Pinout
Note: NI = not yet implemented; N/C = no connection

1	Cap5 (*NI*)	40	Cap4 (*NI*)
2	Cap6 (*NI*)	39	Cap3 (*NI*)
3	Cap7 (*NI*)	38	Cap2 (*NI*)
4	N/C	37	Cap1 (*NI*)
5	V_{SS}	36	Cap0 (*NI*)
6	Discharge	35	V_{SS}
7	Charge	34	Out7
8	Reset	33	Out6
9	CntrBit0	32	Out5
10	CntrBit1	31	Out4
11	CntrBit2	30	Out3
12	CntrBit3	29	Out2
13	CntrBit4	28	Out1
14	CntrBit5	27	Out0
15	V_{DD}	26	N/C
16	ClkMan (*NI*) (enable manual override)	25	V_{DD}
17	Charge (*NI*) (manual override input)	24	V_{ref}
18	Discharge (*NI*) (manual override input)	23	N/C
19	Reset (*NI*) (manual override input)	22	Clr
20	Latch (*NI*) (manual override input)	21	Clk

*Out*X are the comparator outputs, *CntrBit*X are the bits from the 6-bit counter. V_{DD} and V_{SS} are the supply connections. V_{ref} should be a low impedance source of about 1.5V. Small (±0.2V) DC variations on this pin are allowable. AC variations on this pin will decrease ADC accuracy; higher frequencies are more harmful than low frequency (<1kHz) variations. It is recommended to place a high-speed external decoupling capacitor on pin 40 (V_{ref}); a 0.1µF ceramic disk capacitor would suffice.

Results

Specification	Value	Units
Conversion Time (nom.)	9.216	μs
Conversion Frequency (nom.)	108.5	kHz
Clock Frequency (nom.)	20.8333	MHz
Accuracy (approx.)	5	bits
Output	6	bits
LSB Current	5.4	nA
Min. Measured Current	0	nA
Max. Measured Current	346	nA
V_{DD}	5	V
V_{SS}	0	V
V_{REF}	1.5	V
P_{RMS} (one ADC, excluding control ckts)	65	μW

A simulation of one conversion cycle (excluding most of the reset phase) is shown in Figure 2. It can be seen that the comparator starts producing high pulses when the voltage on the capacitor goes below the reference voltage. A single ADC cell consumes approximately 65μW of RMS power over the entire conversion cycle. Most of this power is consumed in the comparator input stage, which uses about 9μA of bias current. Peak power during latching is between 0.5 and 1mW, generally in the lower end of that range. Variations in clock frequency of ±20% do not affect the output significantly. Increasing the clock frequency increases conversion speed, but lowers accuracy. The maximum clock period at which operation is possible was found to be approximately 25nS (f=40MHz), giving a conversion time of 4.8μS. At this frequency accuracy is less than 5 bits. Decreasing the clock frequency could result in the capacitor voltage going above 3.2V, at which point the input current mirror no longer produces a constant current. A plot of the control circuit output is shown in Figure 3. Note that the comparator is latched only during the discharge phase.
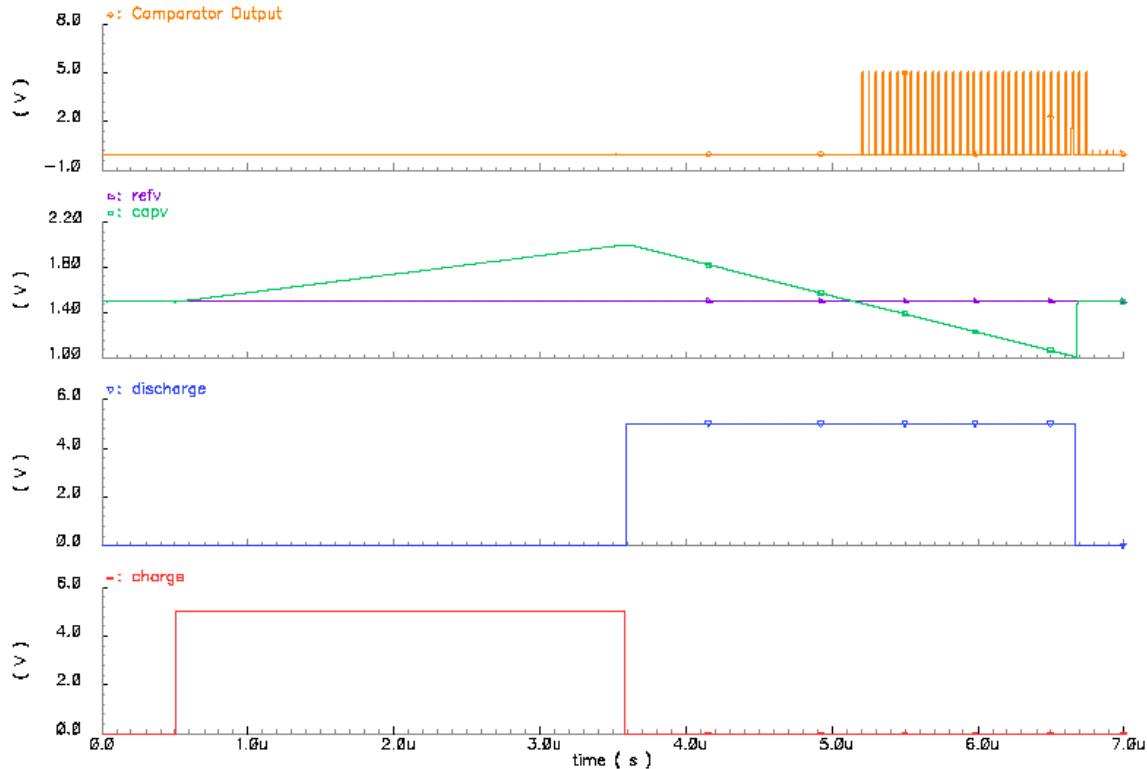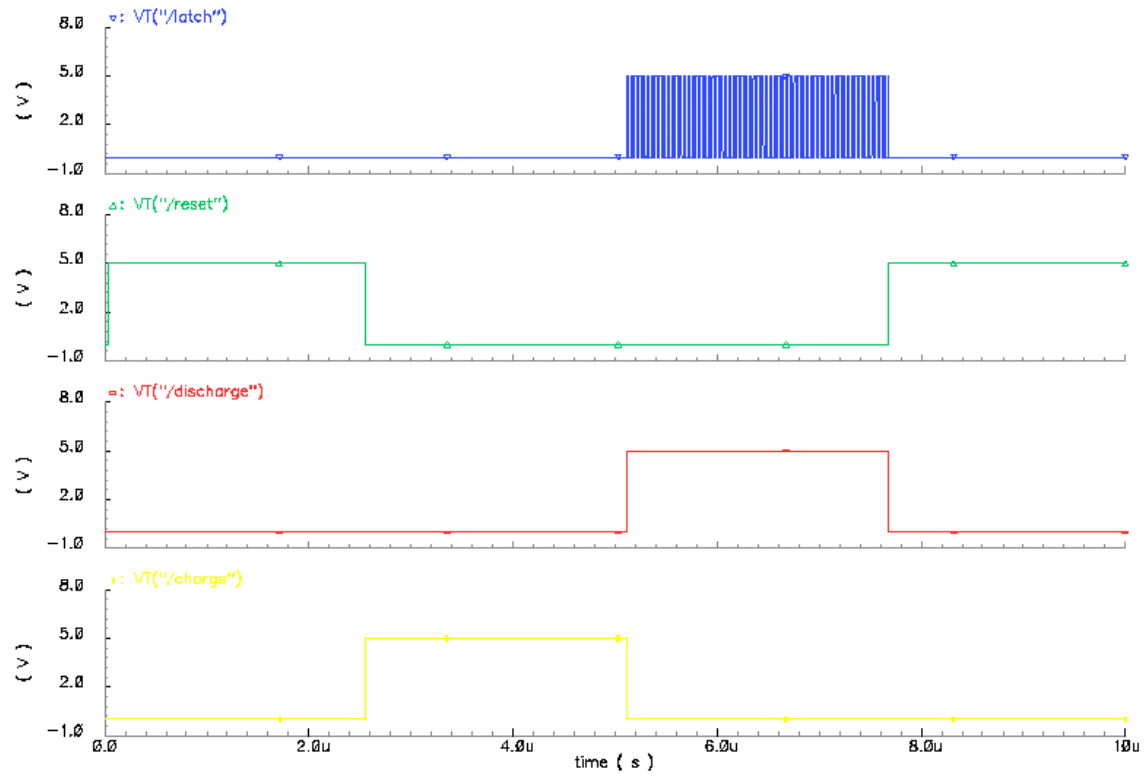

Figure 2: ADC Cell Transient Simulation

Figure 3: Control Circuit Output
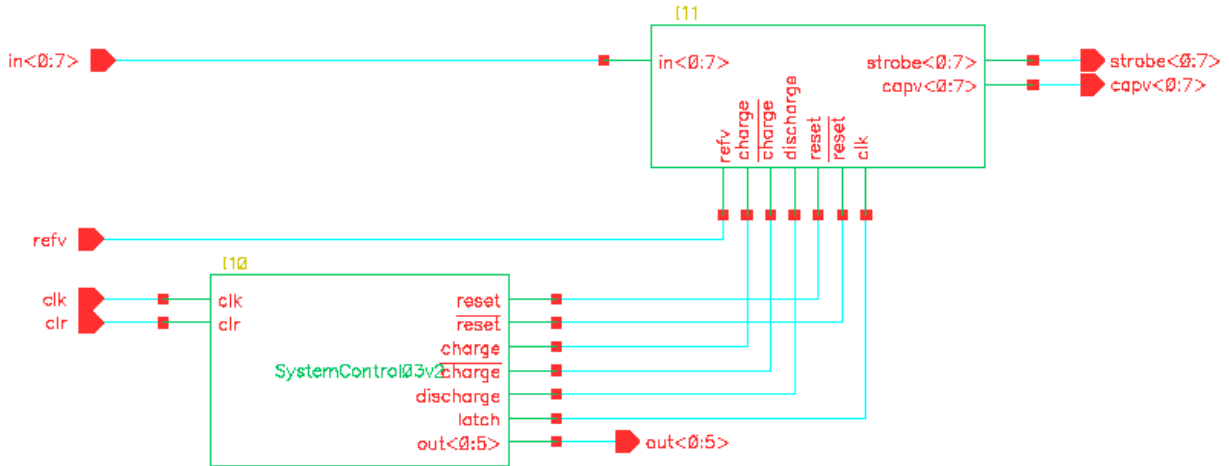
Appendix: Schematics and Layouts

Figure A1: 8 Channel ADC
(note: The top instance is simply 8 ADC cells, the reference voltage generators, and decoupling capacitors.)
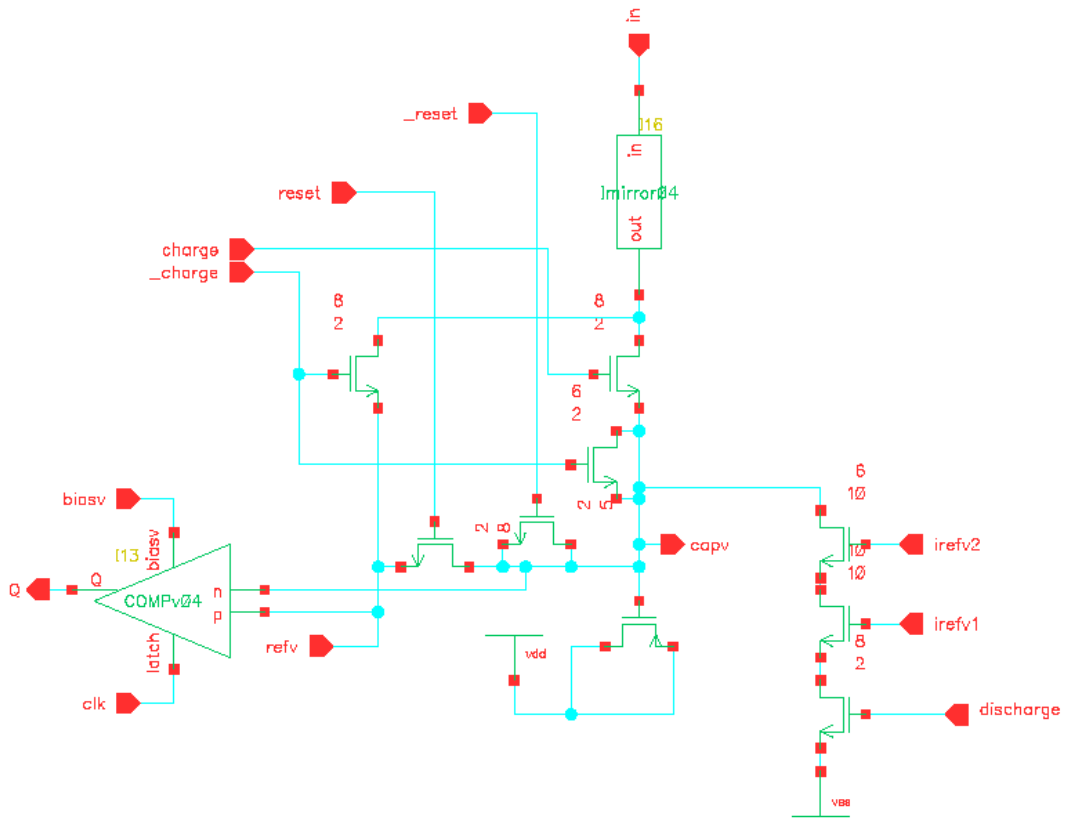

Figure A2: 8 Channel ADC Layout
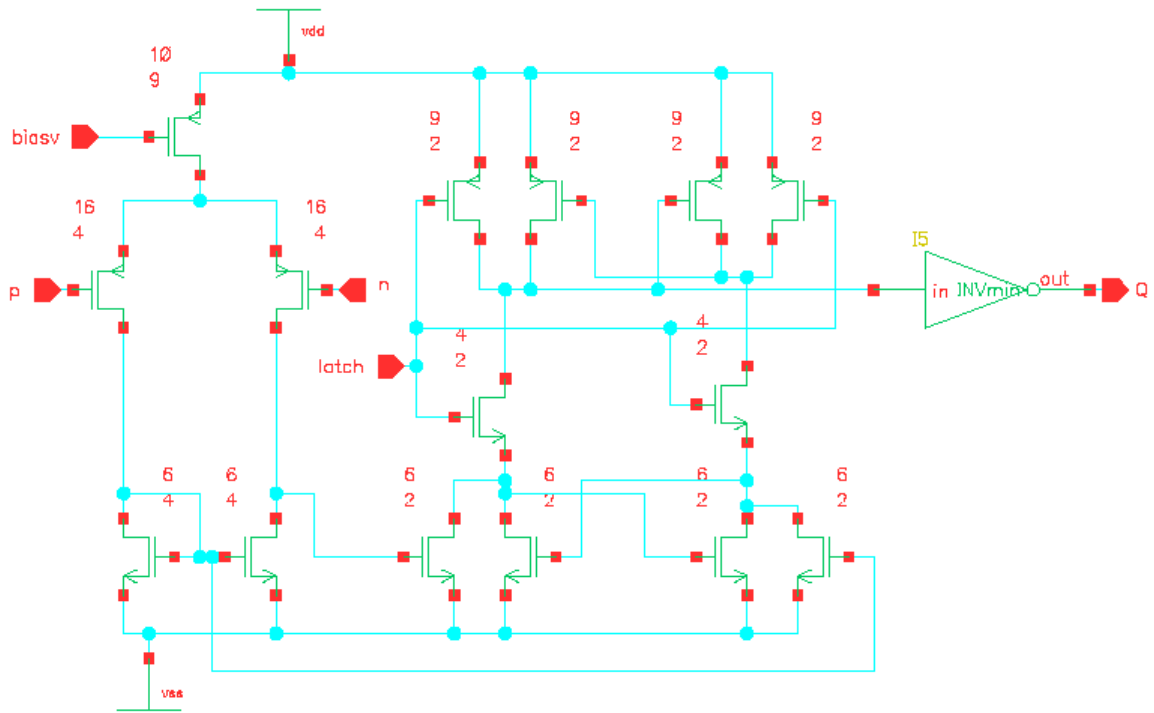
Figure A3: ADC Cell Schematic
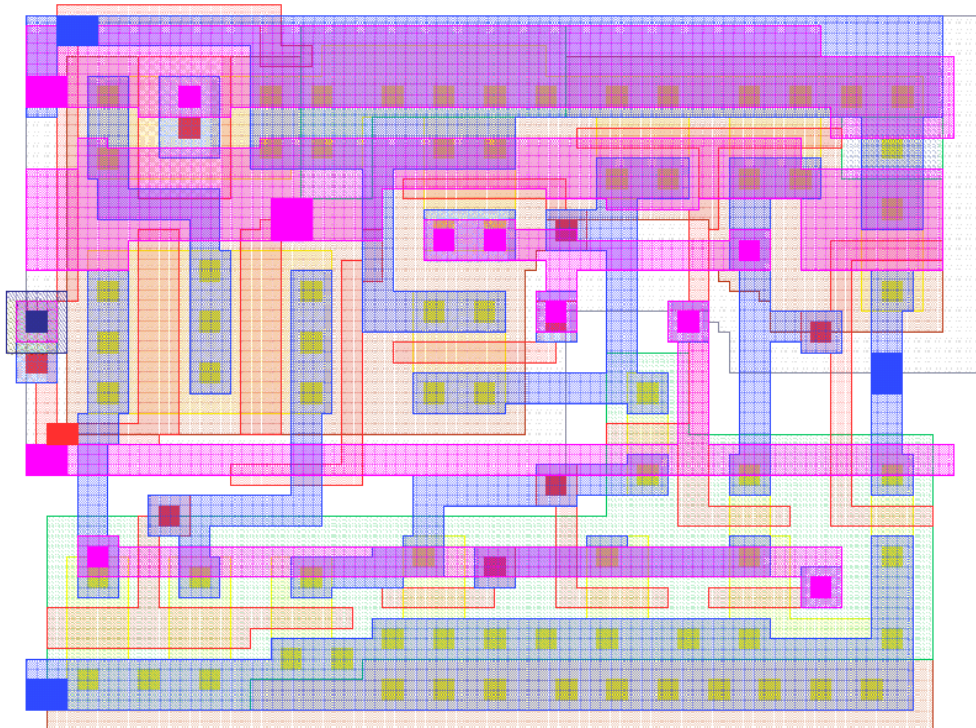
Figure A4: Latched Comparator
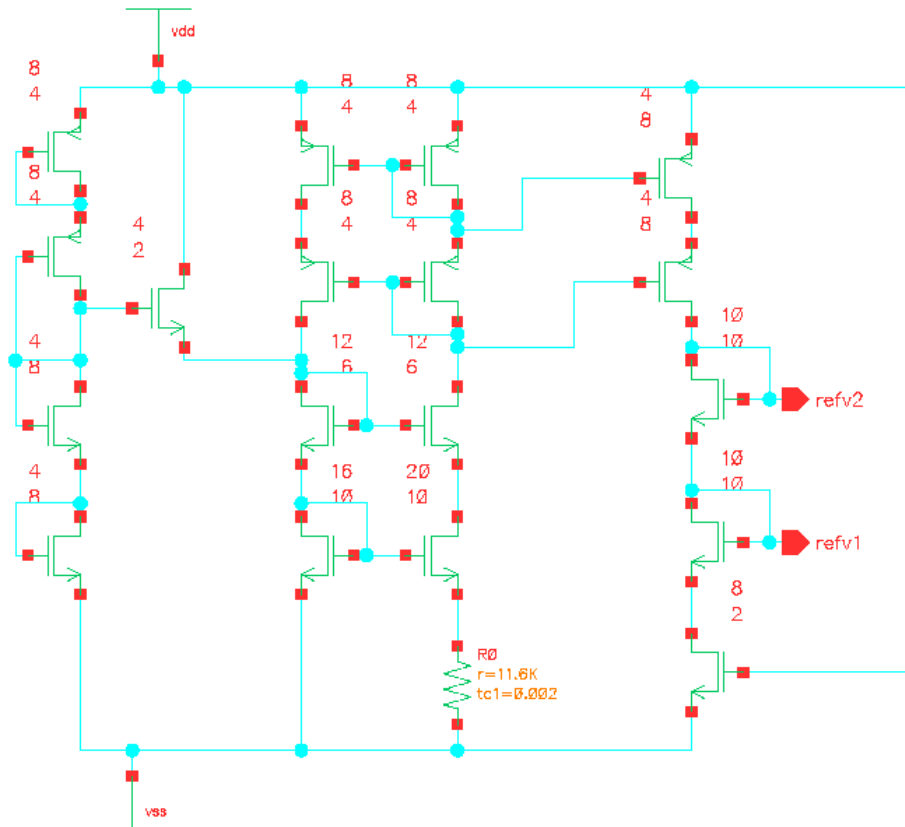

Figure A5: Latched Comparator Layout

Figure A6: β-*Multiplied Current Reference*
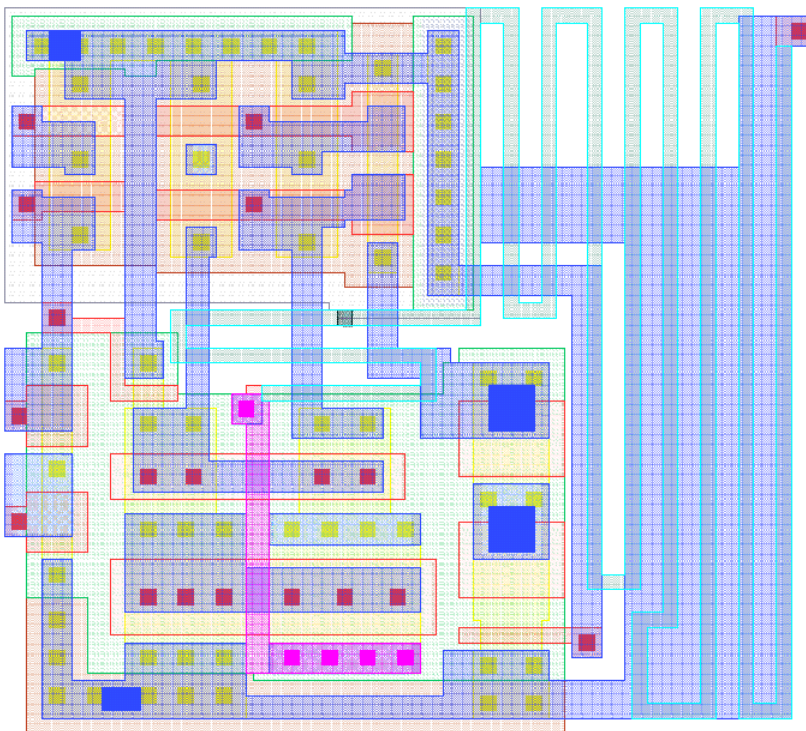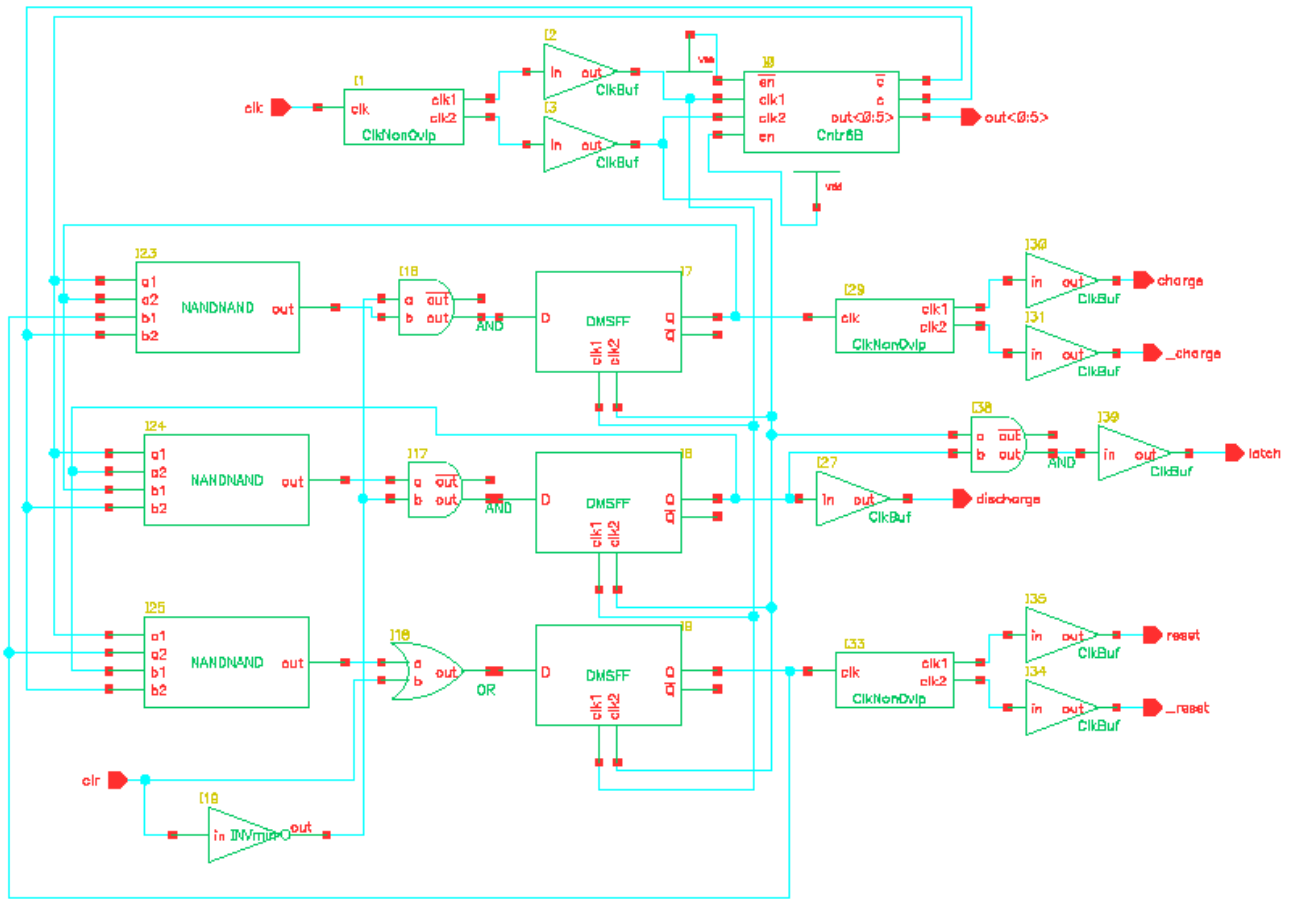

Figure A7: β-*Multiplied Current Reference Layout*

Figure A8: Control Circuit
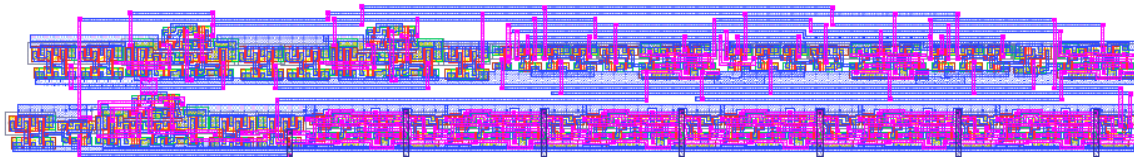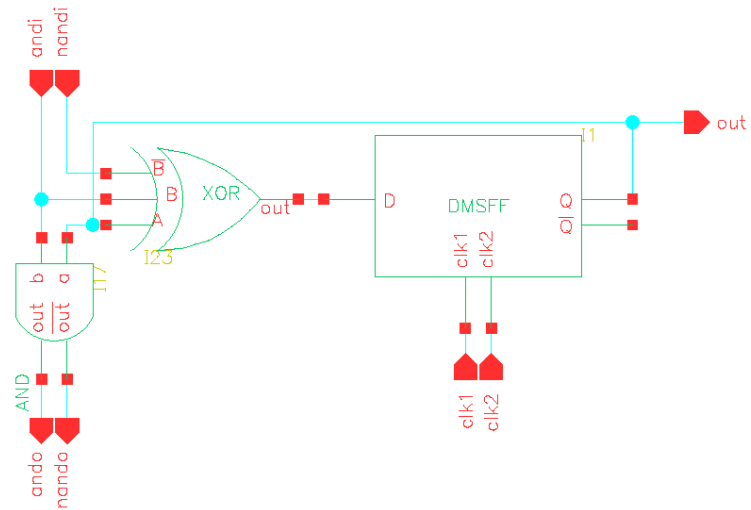

Figure A9: Control Circuit Layout
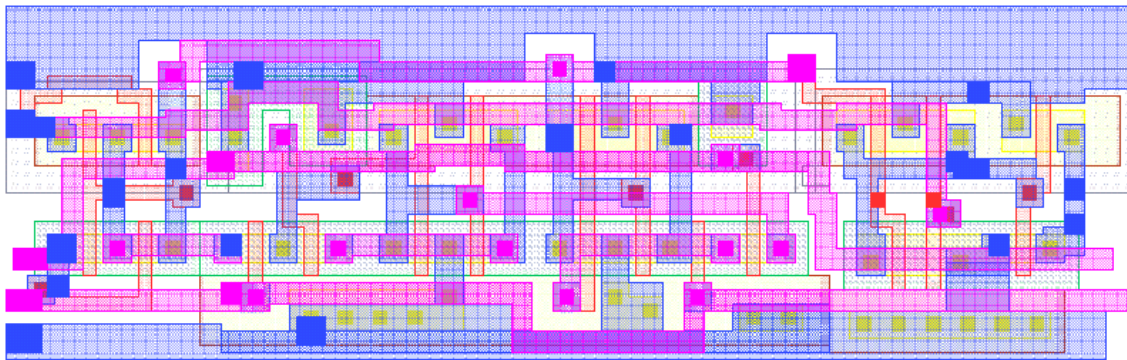
Figure A10: Counter Bit-Slice
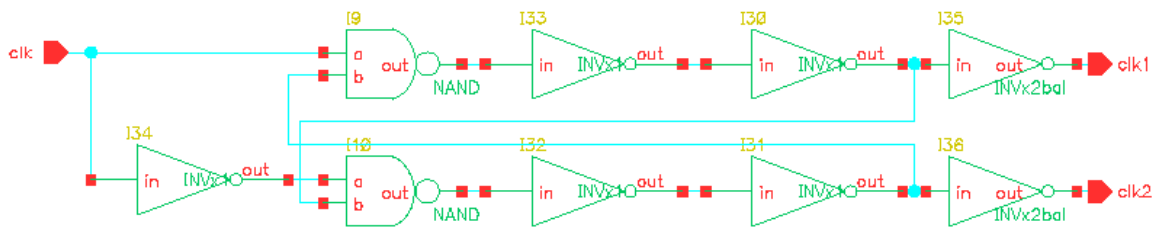

Figure A11: Counter Bit-Slice Layout

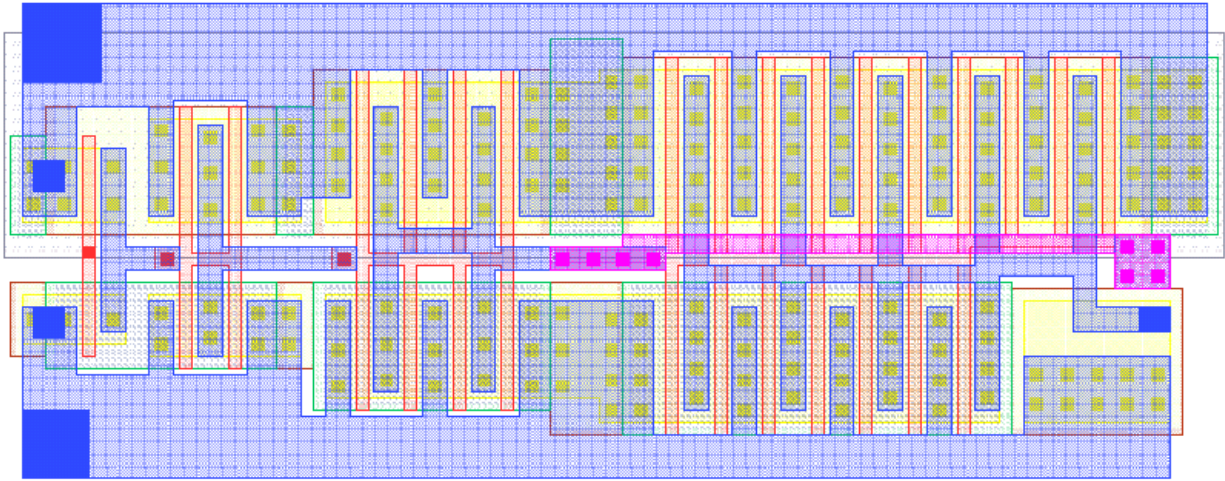*Figure A12: Non-Overlapping Clock Generation*

Figure A13: Digital Pad Driver Layout

References

[1] R. Baker, H. Li, D. Boyce. *CMOS: Circuit Design, Layout, and Simulation*, IEEE Press, 1998. p. 698. ISBN 0-7803-3416-7.

[2] E. Vittoz and J. Fellrath, "CMOS Analog Integrated Circuits Based on Weak Inversion Operation," *IEEE Journal of Solid State Circuits*, Vol. SC-12, No. 3, pp. 223-231, June 1997.