520.492: Mixed-Signal VLSI Systems and Architecture

Assignment #1
Due 2/18/2005

This assignment consists of a small design and layout (mostly layout) project, in preparation of the final project. The project is also to master the Cadence tools including design rule checking and netlist extraction/verification. No simulation is required (simulation will be part of assignment #3).

*Submit **the path to** your Cadence library containing your schematic and layout by e-mail to gert@jhu.edu and yunbin@jhu.edu. Do not send actual files.*

Part 1: Schematic:

The design you will be implementing is a small-scale random-access current-mode CMOS imager containing an 8 X 8 array of photosensors, address decoders, and output demultiplexer. An example for the schematic, which you may adopt, is given in the Figure below. You may come up with alternative structures— the structure shown is simple but far from optimized for optical sensitivity and speed. Keep in mind that an imager structure is very regular and repetitive, and the layout should take advantage of that. By virtue of hierarchy in the design and layout, it is straightforward to extend the structure to a larger size (e.g. a 256 X 256 array). So, economize on the design and layout of cells (and especially the number of different cells!) as much as possible.

Generate the schematic, whether it is the same as or different from the one shown in the Figure. Keep a consistent hierarchical structure in the cells of your design, and the layout.

Bonus challenge: modify the design so it registers temporal change in intensity rather than raw intensity, to implement a simple motion detector on the focal plane. Change detection can be accomplished, for instance, by high-pass filtering of the photocurrent in each pixel prior to random-access output.

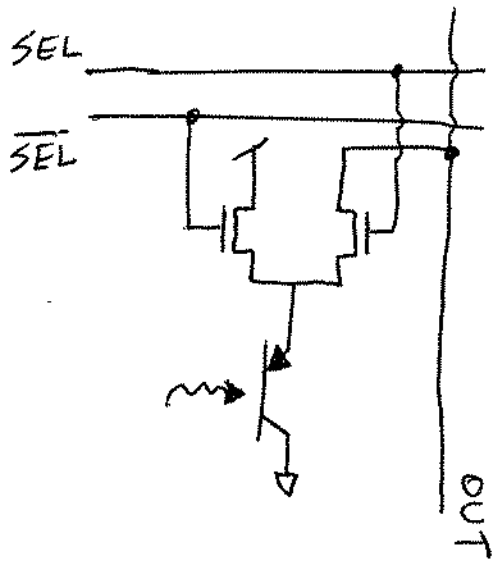
Part 2: Layout:

Layout the cells, and the composition of cells constructing the complete design. It is *not* necessary to include a padframe. Try to optimize the design in area and in efficiency of interconnections, and make the cells abut properly. Regularity in the layout is important. Also, keep in mind the trivialities, e.g. provide a sufficient number of substrate and well contacts, make W/L sufficiently large (L=2λ for digital), use metal layers for critical long lines, make Vdd and GND metal lines wide and straight, etc. It is a good idea to systematically run different metals in orthogonal directions to avoid making too many "via" bridges in long lines.

Part 3: Verification:

The layout should be free of design rule violations, which you can check using the integrated DRC function. Also, check the layout with the schematics using LVS ("layout vs. schematic," tool for verifying the functional equivalence between layout and schematic). The tool compares extracted netlists from the layout and schematic. For examples of these and other procedures, see the simplified Cadence manual. Correct errors in the design or the layout until the verification procedure converges and the circuits are equal (euphoric moment!). It is a good idea to start verifying at the very beginning of the layout, on a cell by cell basis.

Photopixel :



Decoder and Demux :