520.492: Mixed-Signal VLSI Systems

Homework # 2
Due 2/25/2005

Problem 1 (10 points):

Consider the APS (active pixel sensor) circuit implemented by the silicon structure shown in cross-section in Figure 1, and the corresponding timing diagram of the clock signals controlling the operation.

a. Draw the schematic of the implemented circuit. Label the devices and signal nodes consistent with Figure 1.

b. Estimate the total parasitic capacitance on the APS integrating node. Use the device geometries given in Figure 1, and the MOSIS parametric data at http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/ami-c5/t48x-params.txt. Of the tabulated capacitance parameters, consider all area and fringe capacitances that apply except those involving metal lines.

c. Estimate the photocurrent onto the integrating node, assuming a uniform flux of 1,000 photons per square micron and per second, and perfect quantum efficiency (i.e., each incident photon generates one electron-hole pair). Neglect the contribution from the drain junction at the reset nMOS transistor.

d. At 30fps (frames per second), estimate the voltage excursion on the integrating node.

e. The output current on the OUT node is measured just before and after activation of reset (RST). Assume that OUT is held at 100mV below the supply Vdd, and the reset voltage Vinit is lower than a pMOS threshold V_{TP} below Vdd. Estimate the change in output current before and after reset. In general, what is this current difference as a function of photocurrent?

f. *BONUS (for the adventurous)*: How would you implement the circuit at the periphery of the APS array to apply the voltage on the OUT line while registering the difference current? Draw a transistor-level schematic.

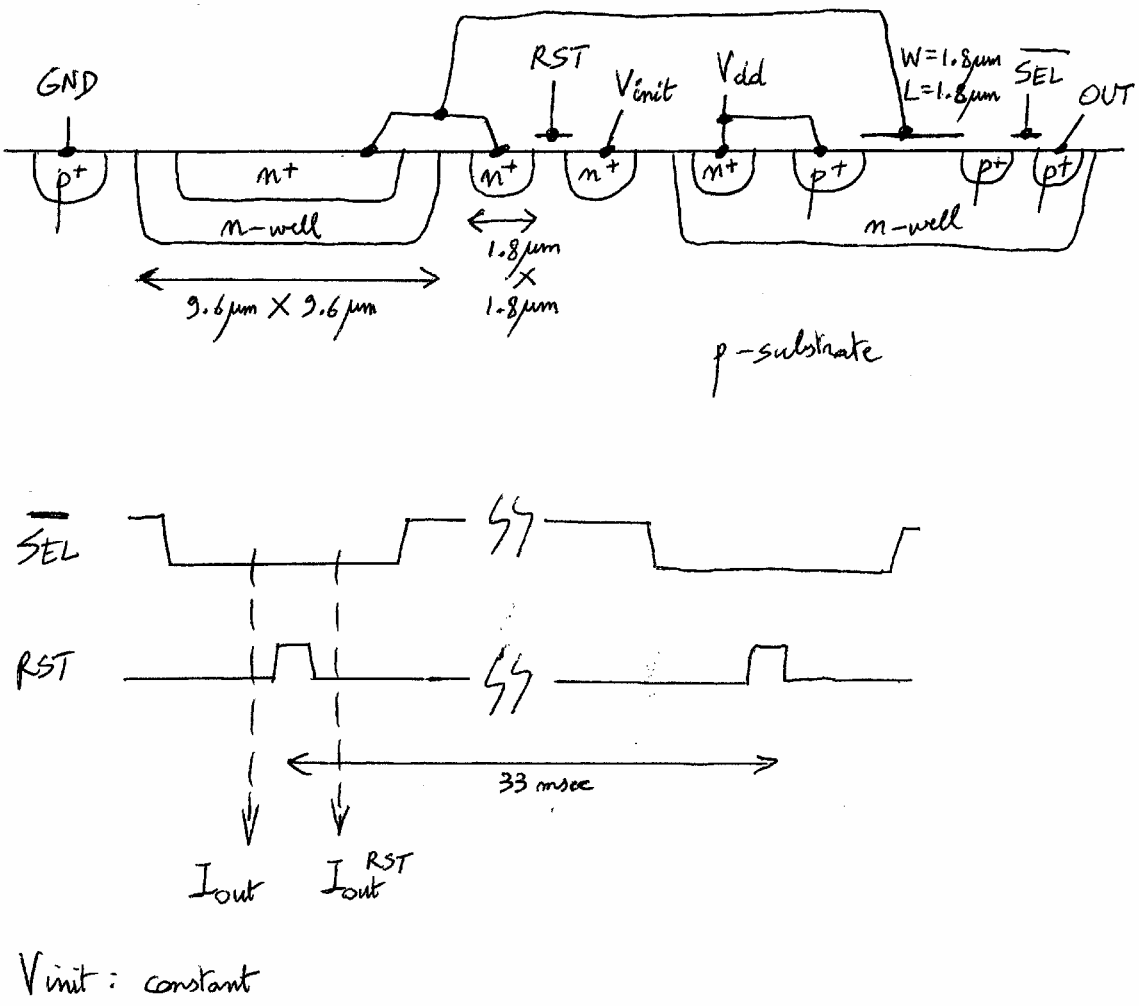
GND
RST
Vinit
Vdd
W=1.8μm
L=1.8μm
SEL
OUT
p+
n+
n-well
1.8μm
9.6μm X 9.6μm
1.8μm
p-substrate
SEL
RST
33 msec
Iout
Iout RST
Vinit : constant

Figure 1

Problem 2 (5 points):

Consider the following 4-input logic functions, OUT1 and OUT2:

A	B	C	D	OUT1	OUT2
0	0	0	0	0	1
0	0	0	1	0	1
0	0	1	0	0	1
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	1	1
0	1	1	0	1	1
0	1	1	1	1	0
1	0	0	0	0	1
1	0	0	1	1	1
1	0	1	0	1	1
1	0	1	1	1	0
1	1	0	0	1	1
1	1	0	1	1	0
1	1	1	0	1	0
1	1	1	1	1	0

(a) Implement the functions each using a CMOS complementary logic gate.

(b) Implement the functions using CMOS transmission gate logic.

(c) Do you recognize these functions? Implement them as efficiently (least number of transistors) as you can.

No schematic entry, just draw the schematic.

Problem 3 (5 points):

Consider the CMOS inverting amplifier shown in Figure 2. Assume subthreshold operation with identical tail currents I'_0 and identical device sizing W/L for nMOS and pMOS transistors.

(a) Find the output voltage V_{out} as a function of input voltage V_{in}.

(b) Find the output current I_{out} as a function of V_{in}. What does this do?

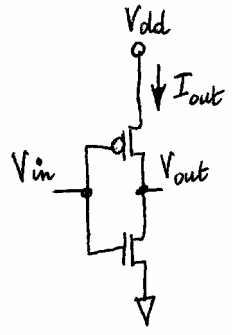

Figure 2