520.492: Mixed-Signal VLSI Systems

Homework # 3

Due 3/4/2005

Design and simulate a 6-bit current-mode dual-slope integrating analog-to-digital converter. The input current *Iin* is single polarity ranging from 0 to 64nA. The reference current *Iref* is -64nA (supplied as a current sink). The sampling rate is 10ksps (10,000 samples per second). The technology is AMIS C5 0.5um CMOS, and the power supply is *Vdd*=3V. Besides the reference current, you may use one current source (bias current *Ibias*) supplied for the entire circuit. You may also use one reference voltage source *Vref*.

No layout is necessary. Design your circuit for correct operation, and minimum power dissipation. Enter your schematic in Cadence. Simulate the circuit with Spectre to verify operation for at least the following four (piecewise constant) values of input current: 0, 31nA, 32nA, and 63nA. Show all six bits output by the counter. Evaluate the power dissipation by observing the time integral of the current through the *Vdd* supply (and *Vref*, if it draws a DC current).

Send the path to your Cadence directory to yunbin@jhu.edu and gert@jhu.edu as before. Return hardcopy printouts of your entire schematic (all cells) and simulation outputs.