520.490: Analog and Digital VLSI Systems and Architecture

Fall Semester 2001

Midterm

NAME: _____

SS: _____

Guidelines:

1. Open book, open notes, open mind.
2. Time limit: 1 hour 15 minutes (in-class).
3. Mark directly on the handout.

The midterm counts for 25% towards the final grade.

Problem 1 (20 Points):

Sketch the cross-section of possible fabricated structures for the following devices in a standard CMOS process. Denote *n* and *p* doped regions (including substrate, well and base regions, if any). For a *p*-well process, you may assume *n*-base is available. Connect unused bulk/substrate terminals to GND or Vdd.

1a. A diode-protected input in an *n*-well process (input node IN with reverse diodes to GND and Vdd, where the substrate is at GND);

1b. An *n*-channel mosfet transistor in an *n*-well process, with bulk separate from the substrate;

1c. An *npn* vertical bipolar phototransistor in a *p*-well process (denote light-sensitive region);

1d. A CMOS switch in a *p*-well process (IN, OUT, C and ~C).

Problem 2 (30 Points):

Design a CMOS digital voting circuit that detects a majority, and a possible tie. Your circuit has four binary inputs, A, B, C, and D, and two binary outputs M (majority) and T (tie). M needs to go high whenever *at least* two of the inputs are high. T goes high whenever *exactly* two of the inputs are high. Minimize the number of transistors used. If you need complements of the inputs, you need to generate these as part of your circuit. Show the entire transistor-level circuit diagram. You can save ink by using sub-circuit "cells" as long as you clearly specify each of them and their terminals.

Problem 3 (50 Points):

Design a current-mode analog random number sequence generator. Each cell in the cascade generates a (pseudo-)random output current I_{out} from the incoming current I_{in} of the previous cell output, by computing the residue of comparing I_{in} with a threshold current I_{ref}, and multiplying the residue by a factor two, as you would for an algorithmic A/D converter. Show the transistor-level circuit diagram implementing a *single* cell. The cell takes an input I_{in}, output I_{out}, and reference input I_{ref}, and operates in continuous time (*i.e.*, there is no sampling or a clock).

All MOS transistors in saturation have zero drain conductance (*i.e.*, ignore the Early effect). Keep your design as simple as possible.

NOTE: The cell needs to *output* one copy of the current I_{out}, and present another copy of that current going to the input of the next cell. Similarly, you cannot assume that one current I_{ref} is distributed to each cell. Instead, the reference input I_{ref} is supplied in the form of a common gate voltage V_{bias} on an nMOS transistor with grounded source.

BONUS: Come up with a pipelined version, where now each random value of the current is sampled over time, with one clock cycle of delay for each cell from input to output. For this, assume that you have a two-phase clock ϕ_1 and ϕ_2 and their complements available.