520.490: Analog and Digital VLSI Systems and Architecture

Fall Semester 2003

Midterm

NAME: SOLUTIONS

Guidelines:

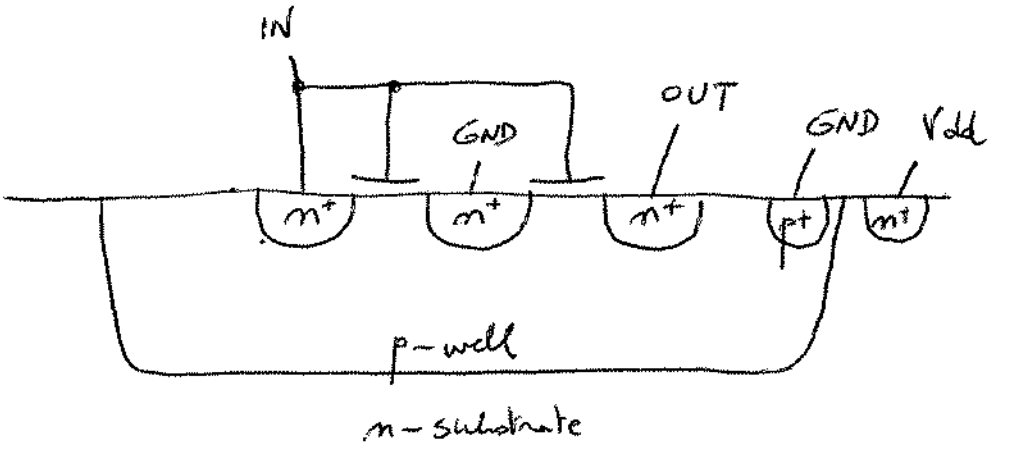
1. Open book, open notes, open mind. No communication with others.
2. Time limit: 1 hour 15 minutes (in-class).
3. Mark directly on the handout.

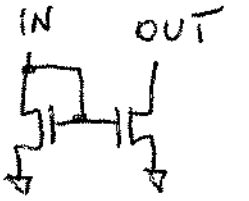
The midterm counts for 25% towards the final grade.

Problem 1 (20 Points):

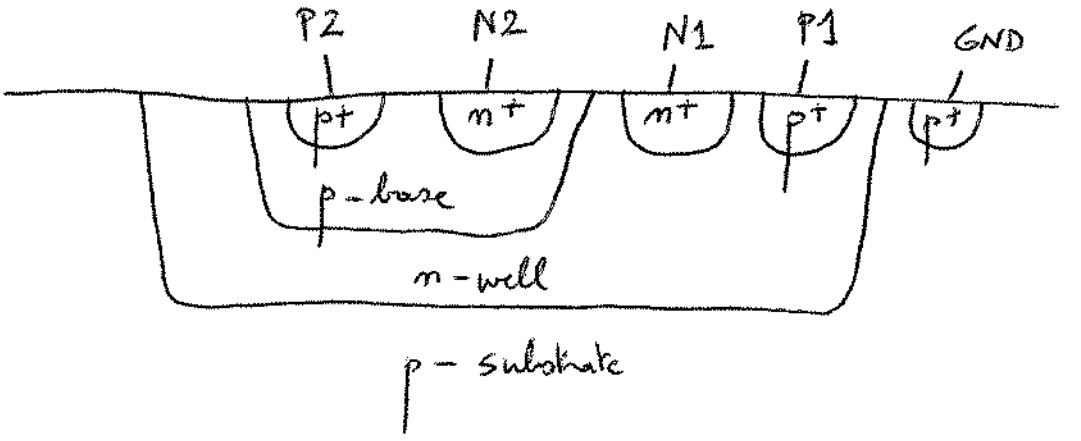
Sketch the cross-section of possible fabricated structures for the following devices in a standard CMOS process. Denote *n* and *p* doped regions (including substrate, well and base regions, if any). You may assume *p*-base is available in an *n*-well process, and *n*-base in a *p*-well process. Connect bulk/substrate terminals to GND or Vdd as needed.

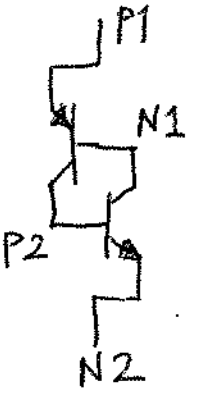
1a. An *n*MOS (non-cascoded) current mirror in a *p*-well process (terminals IN and OUT);



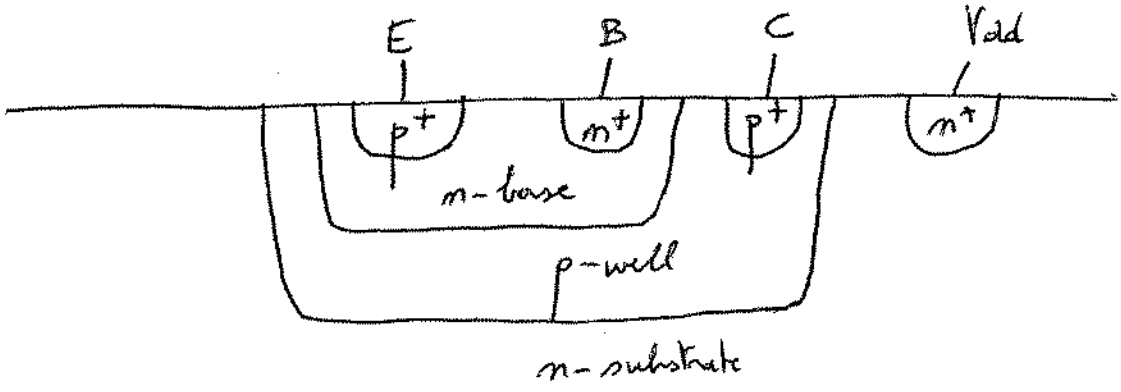


1b. A *pnpn* thyristor in an *n*-well process (terminals P1, N1, P2, N2; all terminals disconnected from the substrate);

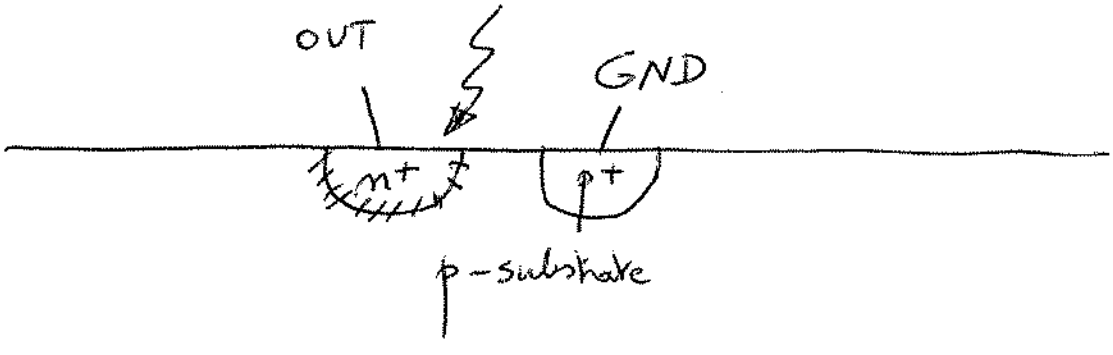




1c. An *pnp* vertical bipolar transistor in a *p*-well process (terminals E, B, C; all terminals disconnected from the substrate);



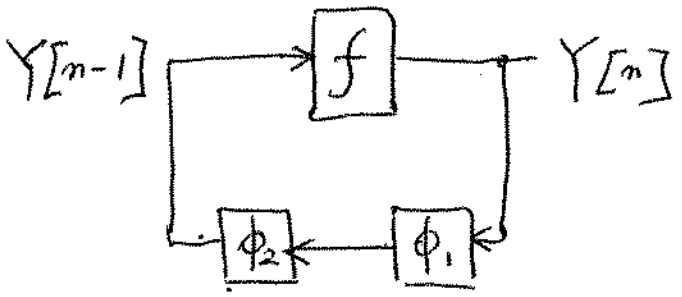
1d. A *pn* photodiode in an *n*-well process (terminals OUT and GND, denote photosensitive region).



Problem 2 (40 Points):

Design a digital CMOS, 2-bit Gray-code counter. Assume you have a non-overlapping two-phase clock ϕ_1, ϕ_2 available, along with their complements. Minimize the number of transistors used. Show the entire transistor-level circuit diagram. You can save ink by using sub-circuit "cells" as long as you clearly specify each of them and their terminals.

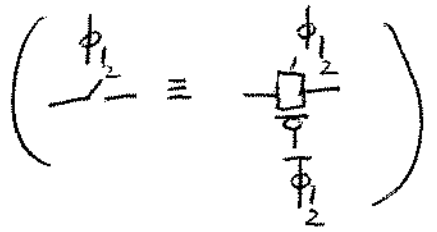
HINT: the counter could be implemented as sequential logic $\mathbf{Y}[n] = f(\mathbf{Y}[n\text{-}1])$, where the outputs $Y_1[n]Y_0[n]$ over time repeat the sequence 00, 01, 11, 10.

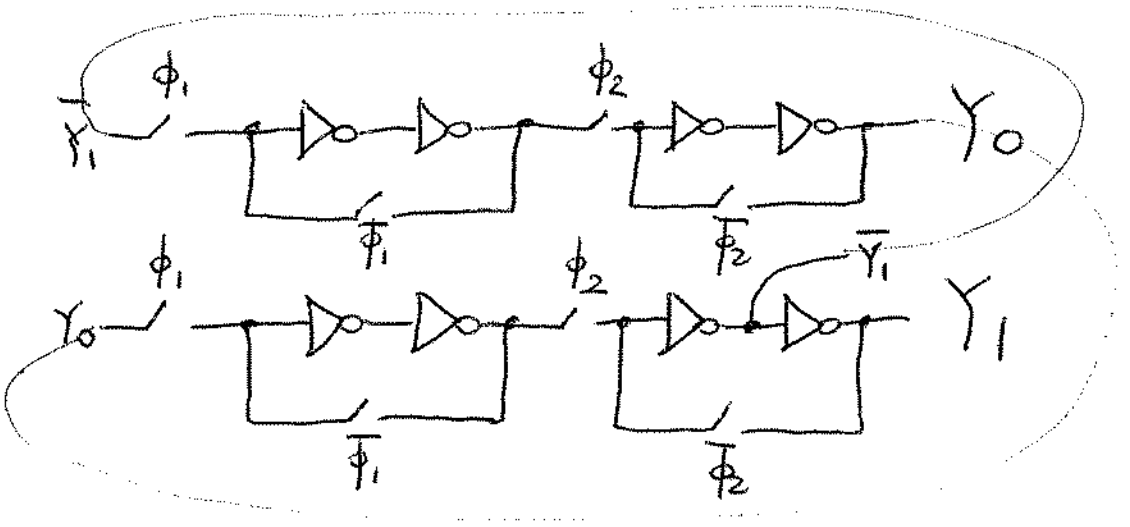


[n-1]		[n]	
Y_1	Y_0	Y_1	Y_0
0	0	0	1
0	1	1	1
1	1	1	0
1	0	0	0

$$\Rightarrow \quad Y_0[n] = \overline{Y_1[n-1]}$$

$$Y_1[n] = Y_0[n-1]$$

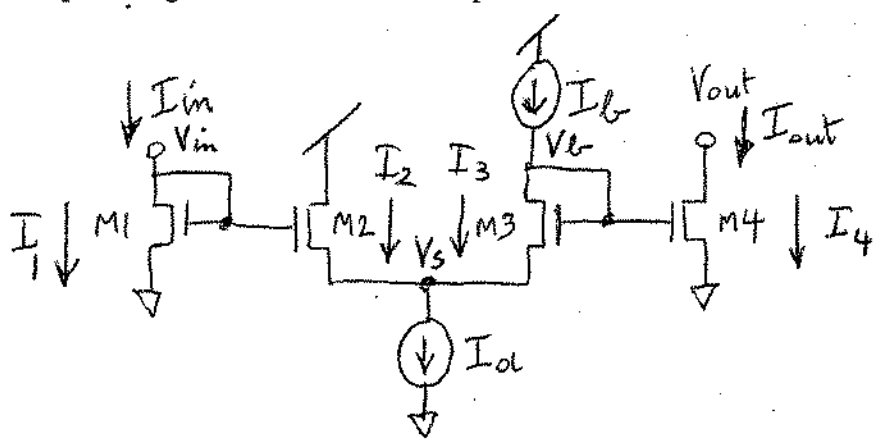




Problem 3 (40 Points):

Consider the current-mode circuit shown below.

1. (*5 points*) Express the currents through MOS transistors M1 through M4 in terms of input and output currents I_{in}, I_{out} and supplied reference currents I_a and I_b.
2. (*35 points*) Find the output current I_{out} as a function of input current I_{in} and reference currents I_a and I_b, assuming the transistors are identically sized and operate in the subthreshold region. You may ignore the Early effect ($\lambda = 0$), and assume the output voltage V_{out} is sufficiently large.
3. *BONUS: (15 extra points)* If I_a represents a 'real' current source realized by an *n*MOS transistor with gate bias V_a, indicate what will happen when the input current reaches lower than a given level of current. Quantify your answer, expressing the effect on the output current.



1. $I_1 = I_{in}$

$I_3 = I_b$ $\quad I_2 = I_a - I_3 = I_a - I_b$

$I_4 = I_{out}$

2. $I_{in} = I_0' \frac{W}{L} e^{\kappa V_{in}/V_t}$ (M1)

$I_a - I_b = I_0' \frac{W}{L} e^{(\kappa V_{in} - V_s)/V_t}$ (M2)

$I_b = I_0' \frac{W}{L} e^{(\kappa V_b - V_s)/V_t}$ (M3)

$I_{out} = I_0' \frac{W}{L} e^{\kappa V_b / V_t}$ (M4)

$$\underset{\frac{(M4)}{(M3)}\frac{(M2)}{(M1)}=1}{\Longrightarrow} \quad I_{out} = \frac{I_b}{I_a - I_b} \cdot I_{in} \qquad (5)$$

3. 

$$I_a = \underbrace{I_0' \frac{W}{L} e^{\kappa V_a/V_t}}_{I_a^0} \left(1 - e^{-V_s/V_t}\right)$$

$$\frac{(M3)}{(M4)} \Rightarrow e^{-V_s/V_t} = \frac{I_b}{I_{out}} \Rightarrow I_a = I_a^0 \left(1 - \frac{I_b}{I_{out}}\right)$$

in (5) $\Rightarrow$ $$I_{out}\left(I_a^0\left(1 - \frac{I_b}{I_{out}}\right) - I_b\right) = I_b \cdot I_{in}$$

$$I_{out}\left(I_a^0 - I_b\right) = I_b I_{in} + I_b I_a^0$$

$$\Rightarrow \quad I_{out} = \frac{I_b}{I_a^0 - I_b} \cdot \left(I_{in} + I_a^0\right)$$

extra term (offset)