BENG 186B: Principles of Bioinstrumentation Design

# Lecture 6

# Comparators, Timers, and Digital Circuits

## References

Webster, Ch. 3 (Sec. 3.5, 3.10, 3.14, 3.16).

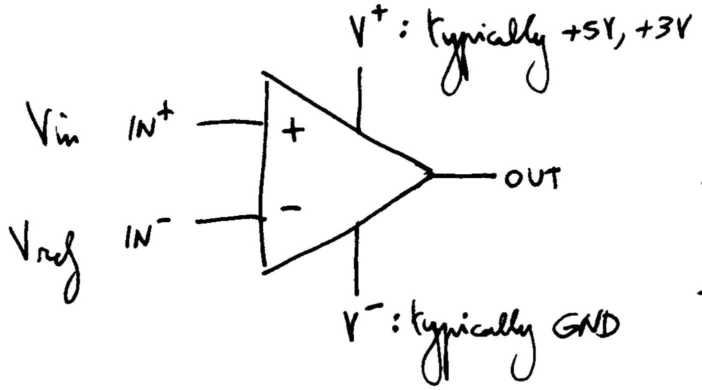
http://en.wikipedia.org/wiki/Comparator

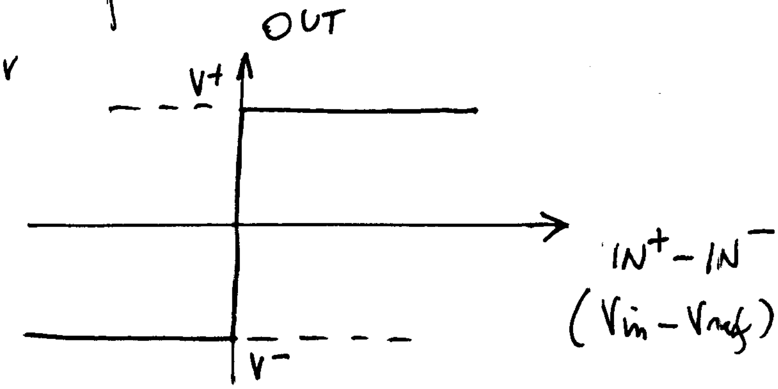
http://en.wikipedia.org/wiki/555_timer_IC

http://en.wikipedia.org/wiki/Logic_gates

## — Comparators : (Webster Sec. 3.5)

→ Like OP-AMPS, but operate in the SATURATION region rather than the LINEAR region, producing a digital output by comparing the two inputs

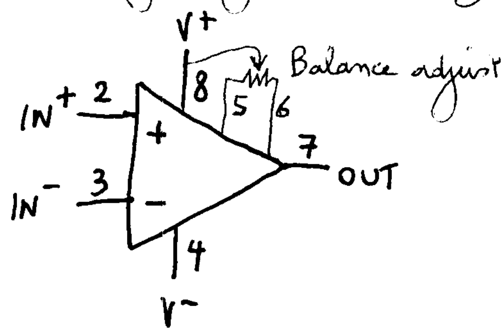


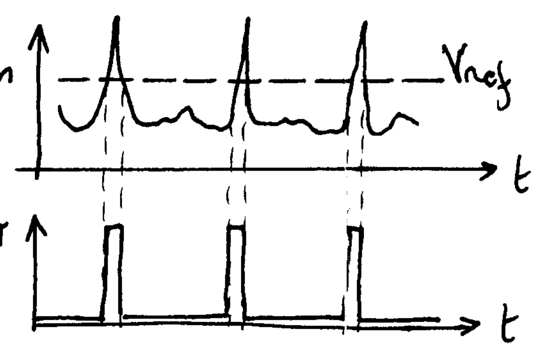

$$OUT = \begin{cases} V^+ & \text{for } IN^+ > IN^- \\ V^- & \text{for } IN^+ < IN^- \end{cases}$$

→ Can use a regular op-amp without feedback, although a "real" comparator is better for this purpose (without internal compensation for faster settling)

Typical comparator: LM311 (National Semiconductor, TI)

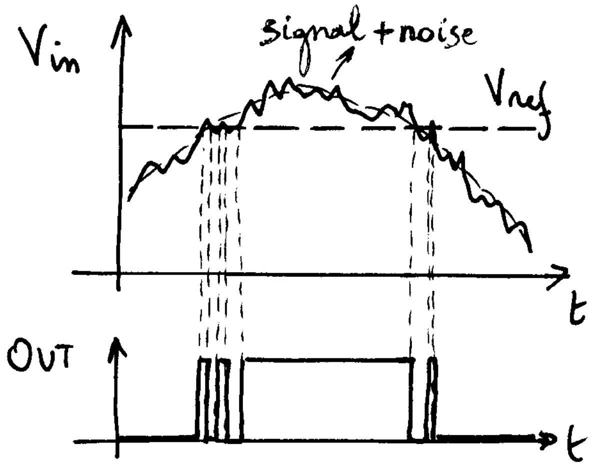



Example application: signal threshold detection

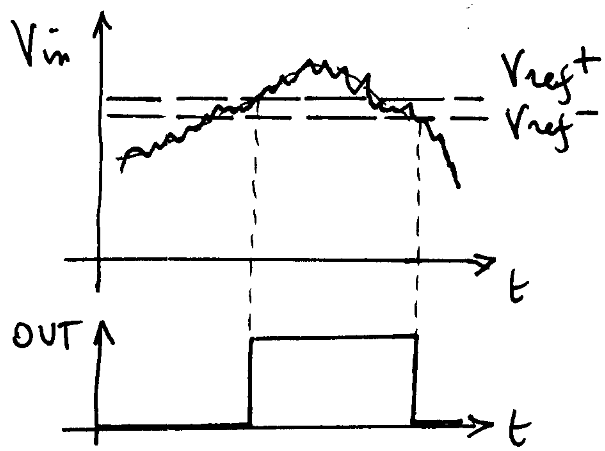


For good signal threshold detection, it is beneficial to include HYSTERESIS in the comparator design:

NO HYSTERESIS:




HYSTERESIS:

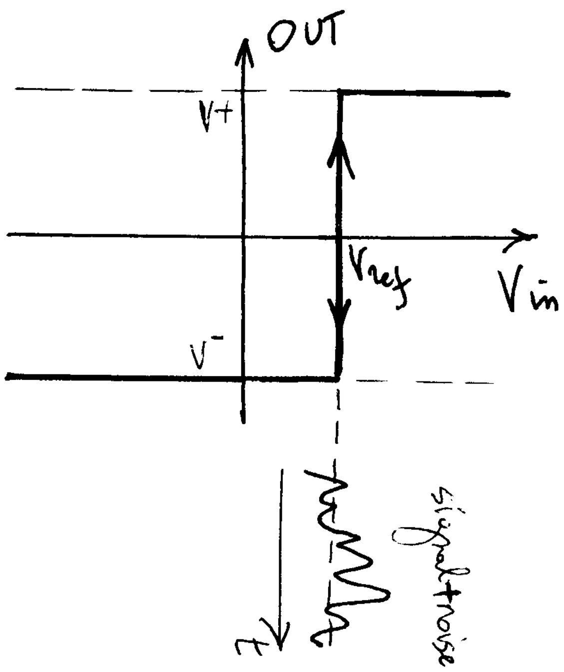



STANDARD COMPARATOR:

single threshold level

$$OUT = \begin{cases} V^+ & \text{when } V_{in} > V_{ref} \\ V^- & \text{when } V_{in} < V_{ref} \end{cases}$$

→ fast, but many erratic transitions



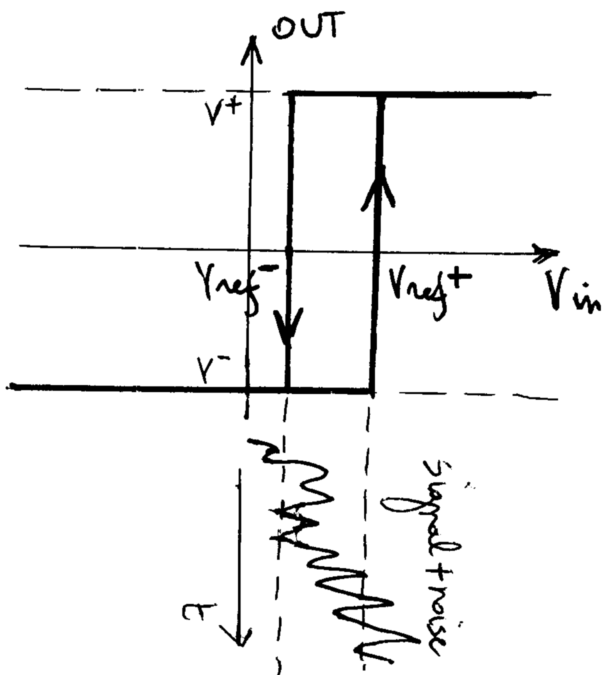

HYSTERETIC COMPARATOR:

two, bistable threshold levels

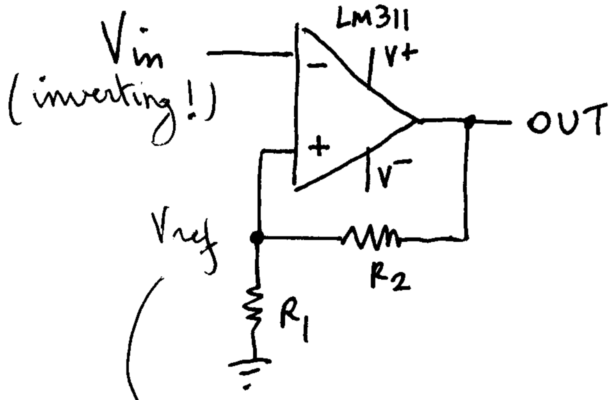
$OUT \leftarrow V^+$ when $V_{in} > V_{ref}^+$ and $OUT = V^-$

$OUT \leftarrow V^-$ when $V_{in} < V_{ref}^-$ and $OUT = V^+$

→ reliable, consistent transitions, but delayed response



## Example: comparator with positive feedback:

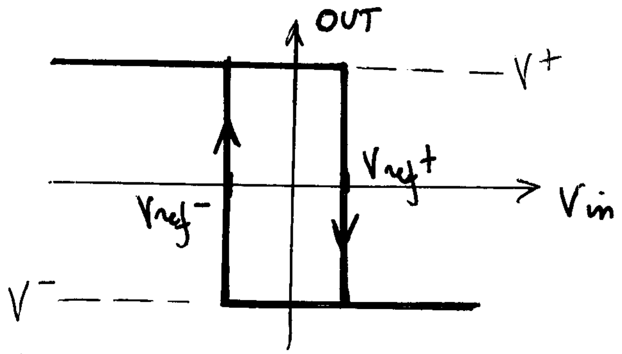



$$OUT = \begin{cases} V^+ & \text{when } V_{in} < V_{ref} \\ V^- & \text{when } V_{in} > V_{ref} \end{cases}$$

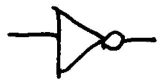
Reference level $V_{ref}$ depends on OUT! (voltage divider)

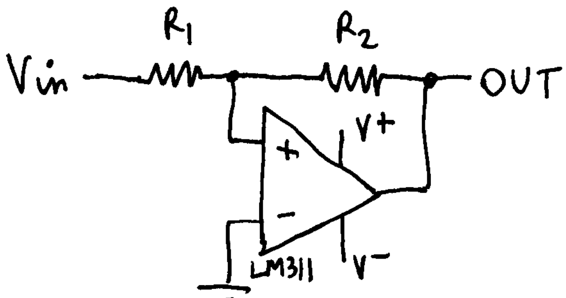
$$OUT = V^- \Rightarrow V_{ref} = V_{ref}^- = \frac{R_1}{R_1 + R_2} \cdot V^-$$

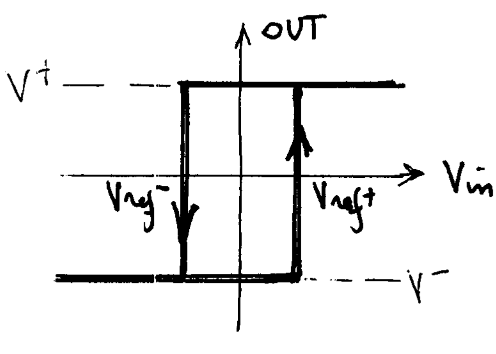
$$OUT = V^+ \Rightarrow V_{ref} = V_{ref}^+ = \frac{R_1}{R_1 + R_2} \cdot V^+$$




NO HYSTERESIS when $R_1 = 0$, or $R_2 \gg R_1$

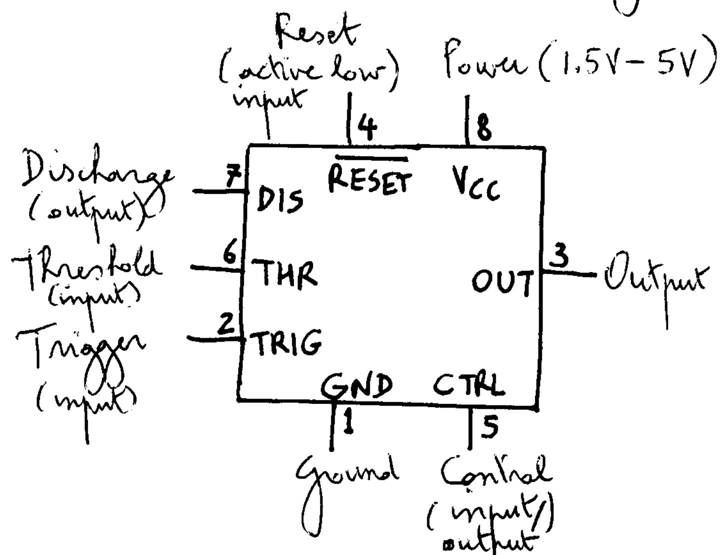
Note: this hysteretic comparator is INVERTING. For a NON-INVERTING hysteretic comparator, simply add a digital inverter  to invert the polarity of the output, or, e.g.:

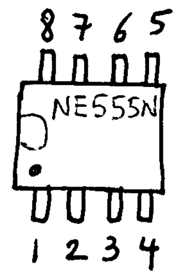


## — Timer circuits :

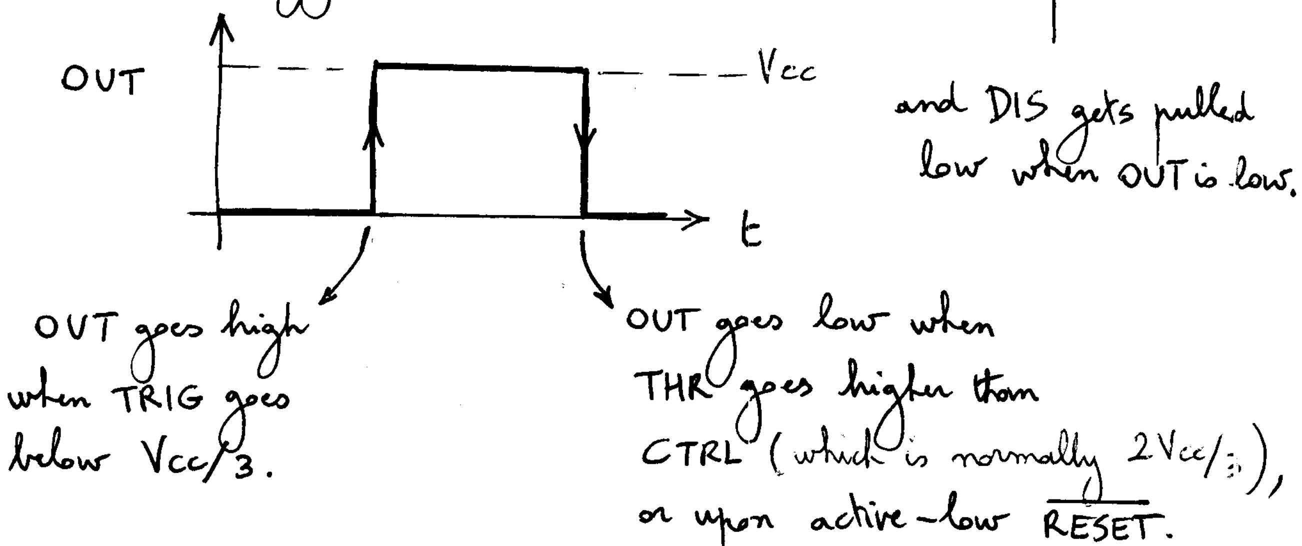
A very common integrated circuit (IC) for timing is the "555" timer IC : (e.g. Texas Instruments TLC555 ; ...)




Typical IC package

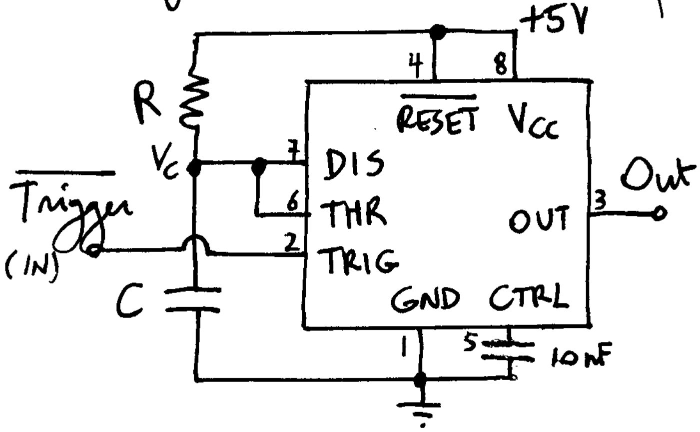
The 555 timer IC produces pulse waveforms at the output in response to trigger and threshold events at its inputs :

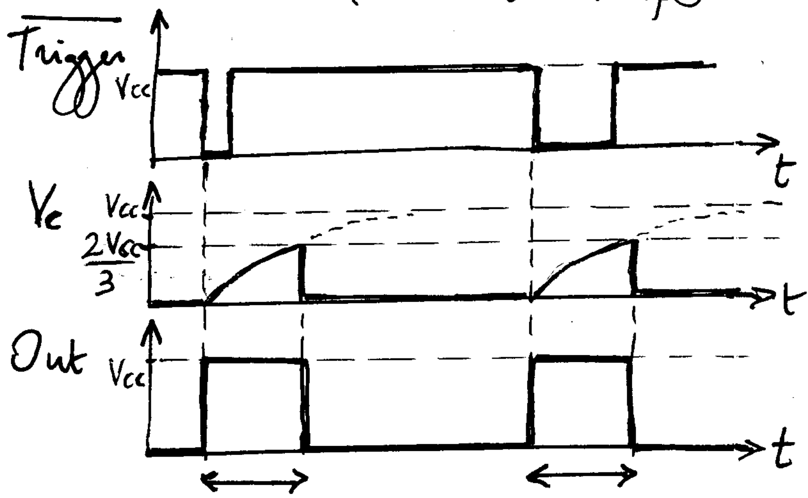



Various timing functions are implemented by connecting resistors, capacitors, and other components to the 555 IC :

## Examples:

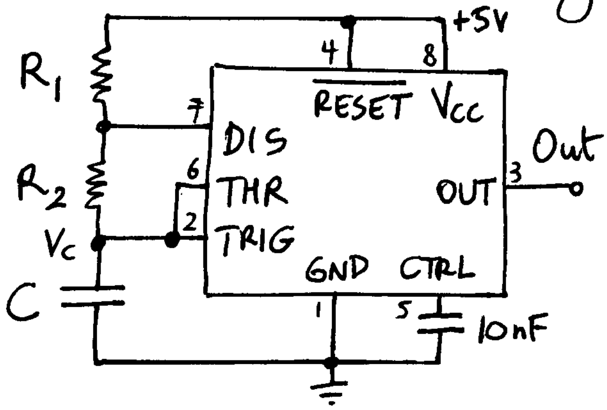
- **Monostable** (single-shot): generates a single pulse of constant width upon a falling edge at the trigger: (downward transition)

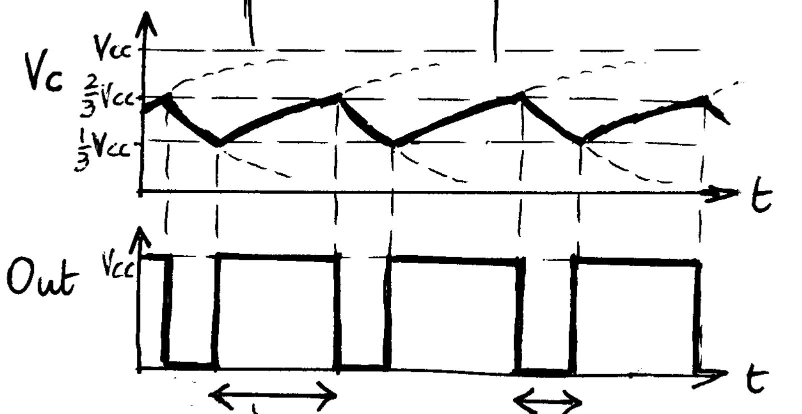



$T = RC\ln(3) \approx 1.1\,RC$     same

- **Astable** (oscillator): generates a periodic square wave:



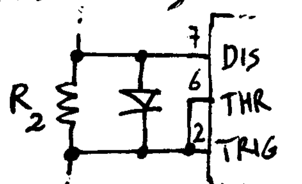




$T_{hi} = (R_1+R_2)C\ln(2) \approx 0.7\,(R_1+R_2)C$     $T_{lo} = R_2 C\ln(2) \approx 0.7\,R_2 C$

$\Rightarrow$ period $T = T_{lo} + T_{hi} = (R_1+2R_2)C\ln(2) \approx 0.7\,(R_1+2R_2)C$

NOTE: Duty cycle > 0.5! ($T_{hi} > T_{lo}$)

FIX for any duty cycle: add diode across $R_2$:




$\Rightarrow T_{hi} = R_1 C\ln(2) \approx 0.7\,R_1 C$

## — Digital circuits

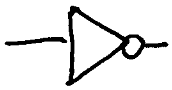
→ operate on binary logic { "0" is GND ; "1" is Vcc (Vdd) typ. 5V or lower (positive power supply)

→ allow simple (switched) control of analog functions, and processing of digitized signals prior to display, logging, or transmission.

**Logic "gates":** Symbols: Truth tables:

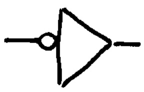
- BUFFER (digital): IN  OUT = IN

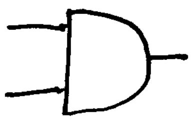
| IN | OUT |
|---|---|
| 0 | 0 |
| 1 | 1 |

- INVERTER (digital): IN  OUT = $\overline{IN}$

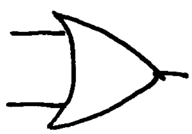
| IN | OUT |
|---|---|
| 0 | 1 |
| 1 | 0 |

In general, the circle at the output or input of a gate denotes signal inversion.

IN  OUT = $\overline{IN}$ is also an inverter.

- AND gate: IN1, IN2  OUT = IN1 • IN2

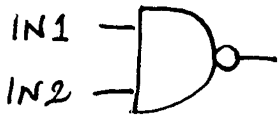
| IN1 | IN2 | OUT |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

- OR gate: IN1, IN2  OUT = IN1 + IN2

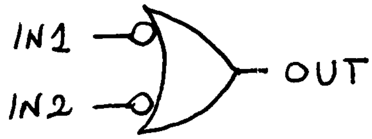
| IN1 | IN2 | OUT |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

## Composite gates:

- NAND (NOT AND):



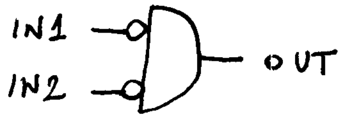

$$\text{OUT} = \overline{\text{IN1} \cdot \text{IN2}} = \overline{\text{IN1}} + \overline{\text{IN2}}$$

( also 

)

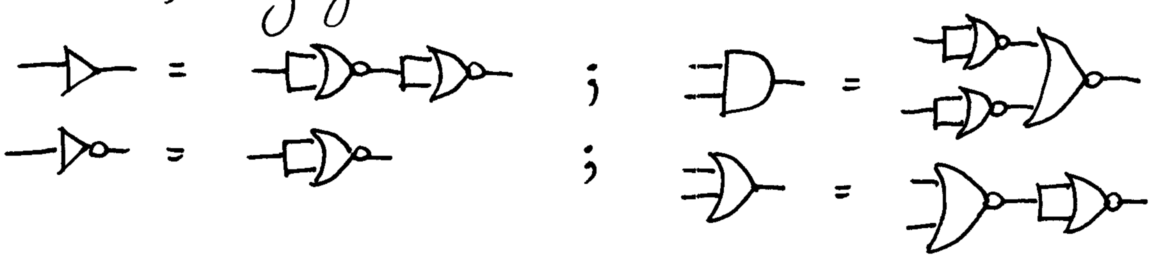
- NOR (NOT OR):


$$\text{OUT} = \overline{\text{IN1} + \text{IN2}} = \overline{\text{IN1}} \cdot \overline{\text{IN2}}$$

( also 

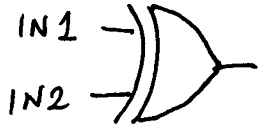
)

<u>NOTE</u>: NAND and NOR are considered fundamental building blocks of digital logic, and are more commonly used than AND and OR in constructing logic, because they are UNIVERSAL, e.g. for NOR:



Field programmable gate arrays (FPGAs) typically use arrays of NOR and NAND gates to synthesize programmable logic functions.

- XOR (exclusive-OR) :




$OUT = IN1 \oplus IN2$

$= IN1 \cdot \overline{IN2} + \overline{IN1} \cdot IN2.$

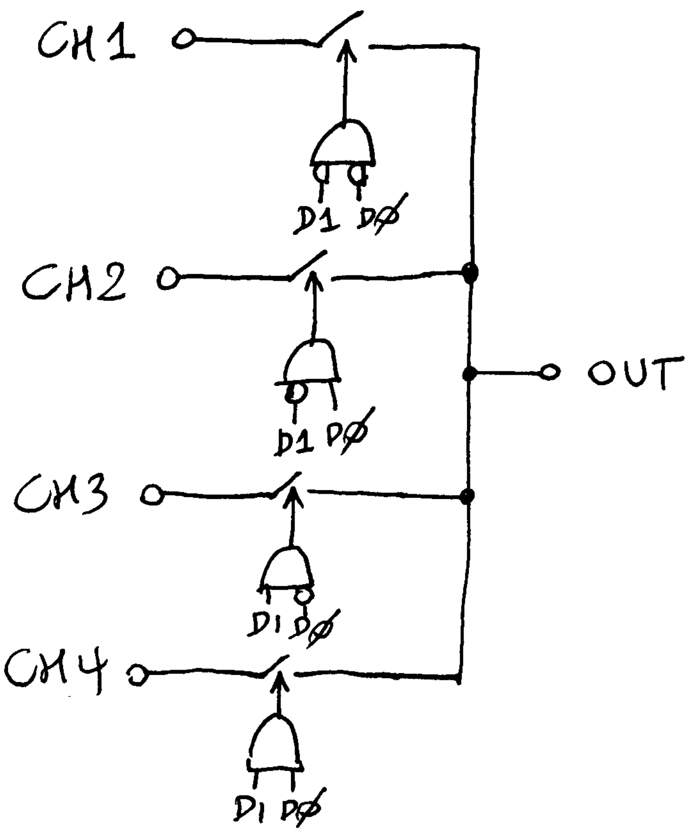
flags when two binary values differ

| IN1 | IN2 | OUT |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

- SUM, CARRY, etc → digital arithmetic

Example : Analog multiplexer : digital control for selection of one out of several input "channels" :

e.g. 4 channels → 2 selection bits
CH1 .. CH4 → D1, DØ (D1 = MSB, DØ = LSB)




| D1 | DØ | OUT connects to: |
|---|---|---|
| 0 | 0 | CH1 |
| 0 | 1 | CH2 |
| 1 | 0 | CH3 |
| 1 | 1 | CH4 |

Useful, for instance, to select between leads in multi-electrode ECG.