Building a VLSI Neuron

Brad Aimone, Stephen Larson and David Matthews

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What is VLSI?

Very-Large-Scale Integrated

- Generating large circuits on a single chip by creating transistors
- Transistors are created by impurity doping
- Analog vs. Digital
How VLSI works subthreshold

Physics of Neural Computation
Silicon and Lipid Membranes

Voltage-dependent p-channel
- Hole transport between source and drain
- Gate controls energy barrier for holes across the channel
- Boltzmann distribution of hole energy produces exponential decrease in channel conductance with gate voltage

Voltage-dependent conductance
- K⁺/Na⁺ transport across lipid bilayer
- Membrane voltage controls energy barrier for opening of ion-selective channels
- Boltzmann distribution of channel energy produces exponential increase in K⁺/Na⁺ conductance with membrane voltage

courtesy Gert Cauwenberghs
Benefits of VLSI

• Efficient modeling (using single transistors rather than software) allows on-line updating of parameters during real-time modeling
• Inherent system noise
• Involves biologically relevant constraints
  – available space (limited wiring)
  – power is at a premium
  – computations must be reliable and robust
Hodgkin-Huxley Model

\[
C \frac{dV}{dt} = g_{Na} m^3 h (E_{Na} - V) + g_K n^4 (E_K - V) + g_{Leak} (E_{Leak} - V) + I_{DC}
\]

\[
\frac{dm}{dt} = \alpha_m (1 - m) + \beta_m m
\]

\[
\frac{dn}{dt} = \alpha_n (1 - n) + \beta_n n
\]

\[
\frac{dh}{dt} = \alpha_h (1 - h) + \beta_h h
\]

...where \(\alpha\)'s & \(\beta\)'s are functions of voltage
HH-Simulated
Goals in designing a HH Neuron

- For any given dynamical state \{V,m,h,n\}
  - System must calculate and apply instantaneous dynamics to calculate state variables
    - \(\frac{dV}{dt} = f(V,m,h,n)\);
    - \(\frac{dm}{dt}=f(a(V),b(V),m)\); ...
  - Therefore, \(a(V), b(V)\)'s must be continuously calculated and fed into \(\frac{dm}{dt}, \frac{dn}{dt}, \frac{dh}{dt}\)
Practical considerations

• Transmit information through circuit as voltages or currents?
  – Some math operations are easier in current, others easier in voltage
  – Currents can be ‘mirrored’ and reversed easily
  – Voltage operations are often more precise

• In our system, most circuit subunits output information as current

• Key state – $V_{\text{neuron}}$ – is a voltage
Alpha/Beta Circuit

- Need to fit unique HH equations for $\alpha$ and $\beta$ for $m, h, n$
- Input is $V_{\text{neuron}}$
- Circuit should be general
Alpha/Beta Circuit

• Can fit with “Bump Circuit”

• Multiple “bumps” can be used to emulate $\alpha$ and $\beta$ curves
  – Each has different $V_{\text{reference}}$ and $I_{\text{bias}}$

Delbruck, 1991
Alpha/Beta Circuit

- Bump circuit implemented
- 4 bumps used to form circuit
Alpha/Beta Circuit

HHNeuron

Voltage (V)

Time (ms)

HHNeuron

Current (pA)

Time (ms)

For Help, press F1
Alpha/Beta Integrator

• Need to calculate \( \frac{dm}{dt} = B \cdot m - A \cdot (1 - m) \)

• Input is a’s and b’s

• Output should be ‘m’, ‘h’, and ‘n’
Alpha/Beta Integrator

- Need to calculate $\frac{dm}{dt} = B \cdot m - A \cdot (1-m)$
- Input is a’s and b’s
- Output should be current representing ‘m’, ‘h’, and ‘n’

Hynna & Boahen, 2006
Alpha/Beta Integrator

- Need to calculate $\frac{dm}{dt} = B \cdot m - A \cdot (1-m)$
- Input is a's and b's
- Output should be current representing ‘m’, ‘h’, and ‘n’
Alpha/Beta Integrator
Multiplier circuit

- Need to combine m’s, h’s and n’s into $m^3h$ and $n^4$
Multiplier circuit

- Need to combine m’s, h’s and n’s into $m^3h$ and $n^4$
- Can use translinear ‘floating gates’ to multiply currents

$\frac{I_n}{I_i} \propto \frac{w_{ni}}{w_{ii}} \times \frac{w_{nk}}{w_{kk}}$

Minch BA et al., 2001
Multipler circuit

- Need to combine m’s, h’s and n’s into $m^3h$ and $n^4$
- Can use translinear ‘floating gates’ to multiply currents
- Diode current charges to capacitors (relative weights are exponents)
  ‘Mirrored’ output current is a function of input currents and capacitive differences

$$I_n \propto I_i^{{w_{ni}/w_{ii}}} \times I_k^{{w_{nk}/w_{kk}}}.$$  

Minch BA et al., 2001
Multiplier circuit
Multiplier circuit
Reversal Potential Scaling

- Current due to conductance and channel states (\(g_{Na}^* m3h\) and \(g_K^* n^4\)) weighted by \((E_{Rev}-V)\)
- Implemented by a “transconductance amplifier”
One whole channel
K+ channel simulated

- Voltage (V) vs Time (ms)
- Current (nA) vs Time (ms)
- Equations: $n^4$, $I_k$
Na+ Channel

- $m$
- $m^3h$
- $I_{Na}$

Graph showing current changes over time with annotations $m$ and $I_{Na}$.
Whole Neuron
Whole Neuron
Results & Conclusions

• Designed and Implemented circuits to calculate
  – alphas and betas from voltage
  – m, h, and n from alphas and betas
  – multiply m, h, and n’s; scale by conductances
  – reference currents to reversal potential and neuron voltage
  – Combine $I_{Na}$, $I_K$, and $I_{Leak}$ to simulate neuron dynamics

• Simulated and began to tune parameters to accurately model HH behavior
Future Directions

• Solve remaining dynamical problems
• Optimize bump circuit approximations
  – Generate more accurate $a(v)$’s and $b(v)$’s
• Tune other parameters ($g_{Na}$, $g_{K}$, $g_{Leak}$, capacitors) to optimize HH behavior
• Work on layout of circuit on chip

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Optimization of Bumps