A VLSI Implementation: Izhikevich's Neuron Model

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In this project, we implemented the circuit which replicates the behavior of a single neuron, by Izhikevich's neuron model. For the ordinary differential equations described in the model, the translinear circuit with the subthreshold-region MOS devices were used. Different neuron models are briefly introduced in chapter 1, followed by the translinear principle in chapter 2. Chapter 3 we discussed the actual circuit we designed, and showed the simulation result.

Contents

1. Introduction to the neuron model

1.1 Hodgkin-Huxley model

In 1952, Hodgkin and Huxley suggested the mathematical model which describes how action potentials in neurons are initiated and propagated. The model uses the electric circuit shown in Figure 1.

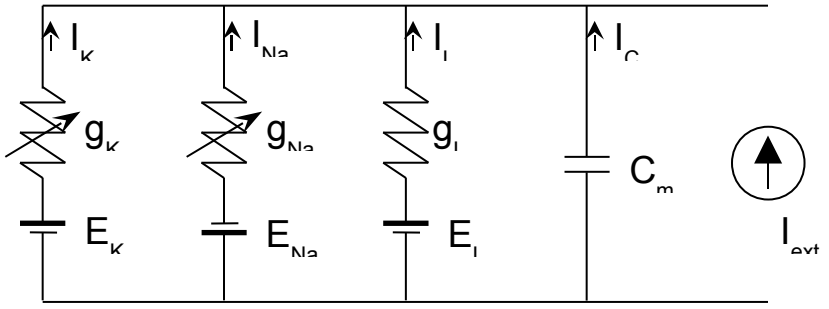

Figure 1. The equivalent electrical circuit of Hodgkin-Huxley neuron model

Current can be carried through the membrane either by charging the membrane capacity or by movement or ions through the resistances I parallel with the capacity. The ionic current is divided into components carried by sodium and potassium ions (I_{Na} and I_K), and a small 'leakage current' (I_L) made up by chloride and other ions. The current for the ion X (I_X) is determined by the product of the conductance of the ion (g_X) and the difference between the membrane potential (V_m) and the equilibrium potential for the ion (E_X).

$$I_K = \overline{g_K} n^4 (V_m - E_K) \tag{1}$$

$$I_{Na} = \overline{g_{Na}} m^3 h (V_m - E_{Na}) \tag{2}$$

$$I_L = \overline{g_L} (V_m - E_L) \tag{3}$$

Hence the differential equation for the circuit can be derived as

$$C_m \frac{dV_m}{dt} = I_{ext} - I_K - I_{Na} - I_L \tag{4}$$

where the channel activation/inactivation probability n, m, and h are given by differential equations

$$\frac{dn}{dt} = \alpha_n (1 - n) - \beta_n n = \frac{n_\infty - n}{\tau_n} \quad \text{, slow K+ activation} \tag{5}$$

$$\frac{dm}{dt} = \alpha_m (1 - m) - \beta_m m = \frac{m_\infty - m}{\tau_m} \quad \text{, fast Na+ activation} \tag{6}$$

$$\frac{dh}{dt} = \alpha_h (1 - h) - \beta_h h = \frac{h_\infty - h}{\tau_h} \quad \text{, slow Na+ inactivation} \tag{7}$$

and channel gate opening rate $\alpha(V_m)$ and closing rate $\beta(V_m)$ are defined as

$$\alpha_n (V_m) = \frac{10 - V_m}{100\left(e^{1 - V_m/10} - 1\right)}; \beta_n (V_m) = \frac{1}{8} e^{-V_m/80} \tag{8}$$

$$\alpha_m (V_m) = \frac{25 - V_m}{10\left(e^{2.5 - V_m/10} - 1\right)}; \beta_m (V_m) = 4e^{-V_m/18} \tag{9}$$

$$\alpha_h (V_m) = \frac{7}{100} e^{-V_m/20}; \beta_h (V_m) = \frac{1}{1 + e^{3 - V_m/10}} \tag{10}$$

Although the Hodgkin-Huxley model can describe the activity of a neuron accurately, the complexity of the model makes it hard to perform the intuitive analysis. The Hodgkin-Huxley model has four variables - V_m, n, m, and h. When plotted, the sodium

activation m closely follows the dynamics of the membrane voltage V_m. Similarly, the sodium inactivation 1-h and the potassium activation n move close to each other.

By using this characteristic, the simplified versions of Hodgkin-Huxley model such as FitzHugh-Nagumo model, or Morris-Lecar model have been suggested which only have two variables instead of four.

1.2 Izhikevich's model

In 2003, Eugene Izhikevich presented a neuron model which is computationally simple and capable of producing the firing patterns exhibited by real biological neurons. It is described as a two-dimensional system of ordinary differential equations of the form

$$\frac{dv}{dt} = 0.04v^2 + 5v + 140 - u + I \tag{11}$$

$$\frac{du}{dt} = a(bv - u) \tag{12}$$

with the auxiliary after-spike resetting

$$\text{if } v \geq 30mV \text{, then } \begin{cases} v \leftarrow c \\ u \leftarrow u + d \end{cases} \tag{13}$$

where v represents the membrane potential of the neuron and u represents a membrane recovery variable, which accounts for the activation of K^+ ionic current and inactivation of Na^+ ionic current. After the spike reaches its upper limit (+30mV), the membrane voltage and the recovery variable are reset according to Eq. 13. Synaptic currents or injected DC currents are delivered via the variable I. a and b are dimensionless parameters which governs behaviors of u. c and d are also dimensionless parameters which defines reset value of v and u.

By selecting different values of these parameters, Izhikevich's model can generate various intrinsic firing patterns as summarized in Figure 2. Also, the coefficients of the function $0.04v^2 + 5v + 140$ in Eq. 11. can be varied, even though they were chosen here to fit the case of large-scale networks of spiking neurons.

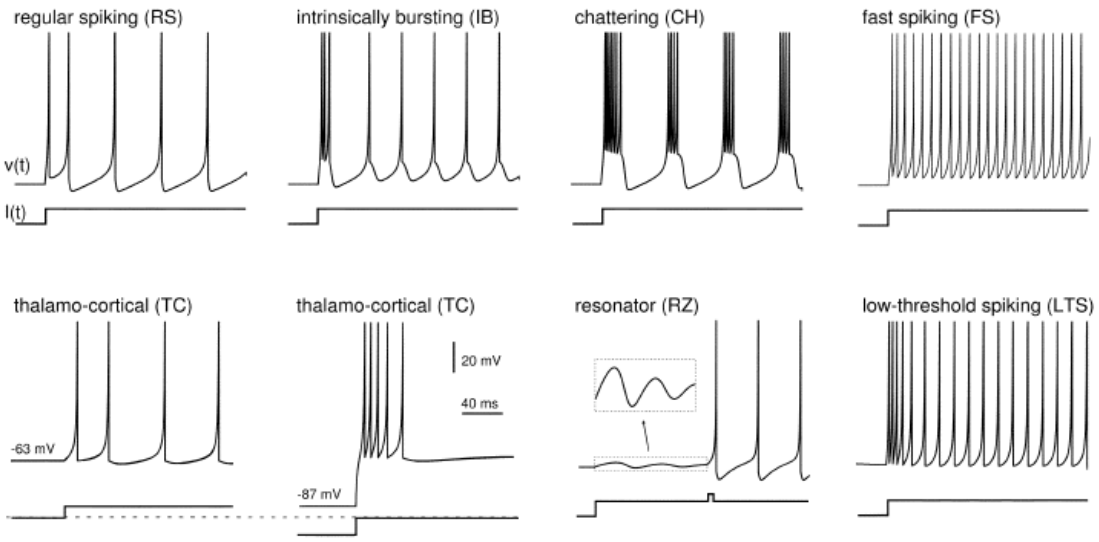

Figure 2. Known types of neurons correspond to different values of the parameters a, b, c, d in the model describe by the Eq. 11 and 12. RS, IB and CH are cortical excitatory neurons. FS and LTS are cortical inhibitory interneurons. Each inset shows a voltage response of the model neuron to a step of DC current $I = 10$ (bottom). Time resolution is 0.1 ms. This figure is reproduced with the permission from www.izhikevich.com. *(Electronic version of the figure and reproduction permissions are freely available at www.izhikevich.com.)*

2. Translinear Circuits

2.1 Introduction

A translinear circuit is a circuit that carries out its function using the translinear principle. The word translinear was coined by Barrie Gilbert, to describe a class of circuits whose large-signal behavior hinges on the extraordinarily precise exponential current-voltage characteristic of the bipolar transistor and the intimate thermal contact and close matching of monolithically integrated devices. At the same time, Gilbert also proposed a general circuit principle, the translinear principle, by which we can analyze the state-state large-signal characteristics of such circuits quickly, usually with only a few lines of algebra, by considering only the currents flowing in the circuits.

The tranlinear principle has been the basis of useful nonlinear circuits, including wideband analog multipliers, translinear current conveyors, translinear frequency multipliers, operational current amplifiers.

2.2 Ideal translinear elements

Figure 3a shows a circuit symbol for an ideal tranlinear element(TE). Ideal TE have the nearly inviolate exponential current-voltage relationship of the bipolar transistor and the infinite input impedance of the MOS transistor. Assuming the ideal TE produces a collector current I , I is exponential in its gate-to-emitter voltage V , and is given by

$$I = \lambda I_S e^{\eta V / U_T} \tag{14}$$

where I_S is a pre-exponential scaling current, λ is a dimensionless constant that scales I_S proportionally, η is a dimensionless constant that scales the gate-to-emitter voltage V ,

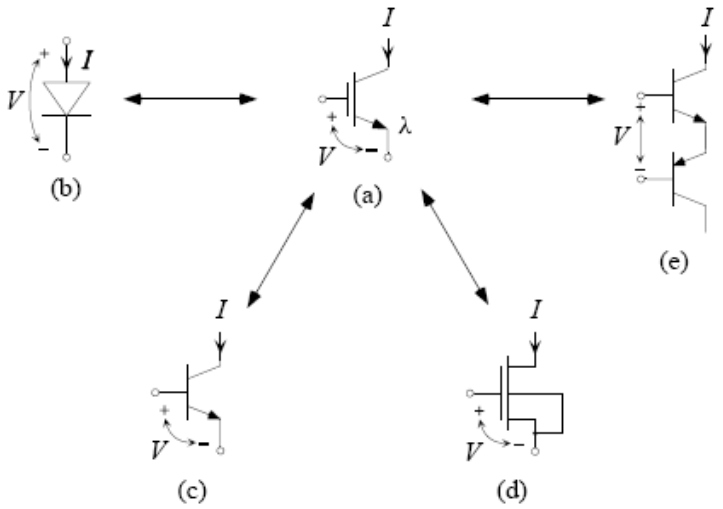

Figure 3. Translinear elements. (a) Circuit symbol for an ideal TE which has a controlling voltage input V and an output current I . (b) – (e) show five practical TE implementation. (b) a diode, (c) an npn bipolar transistor, (d) a subthreshold MOS transistor with its source and bulk connected together, and (e) a compound TE comprising an npn and a pnp with their emitters connected together. The appropriate complementary transistors for the TEs shown in (c) and (d) are also TEs.

and U_T is the thermal voltage, kT/q . To demonstrate that the ideal TE is translinear, we can calculate its transconductance by simply differentiating Eq. 14 with repect to V to obtain

$$g_m = \frac{\partial I}{\partial V}$$

$$= \lambda I_S e^{\eta V/U_T} \times \frac{\eta}{U_T}$$

$$= \frac{\eta I}{U_T} \qquad (15)$$

Figures 3(b) through 3(e) show five practical circuit implementations of the ideal TE. The subthreshold MOS transistor with its source and bulk connected together, shown in Figure 3(d), is used for the project. In this case, the device biased into saturation also has an exponential current-voltage characteristic. λ corresponds to the W/L ratio of the MOS transistor and η is equal to κ, which is the incremental capacitive-divider ratio between the gate and the channel. The requirement that the source and bulk be shorted together stems from the fact that the gate and source do not have the same effect on the energy barrier – i.e., the source-to-channel potential) that controls the flow of current in the channel. The source potential directly affects this barrier height, whereas the gate couples capacitively into the channel and only partially determines the channel potential. The bulk also couples into the channel capacitively and partially determines the channel potential. By connecting the source and bulk together, we can use the bulk in opposition to the source to reduce the source's net effectiveness at controlling the barrier height to match precisely the effectiveness of the gate.

2.3 The translinear principle

In this section, the translinear principle is derived for a loop of ideal TEs. Figure 4 shows the closed loop of N ideal TEs. The large arrow shows the clockwise direction around the loop. If the emitter arrows of a TE points in the clockwise direction, we classify the TE as a clockwise (CW) element. If the emitter arrow of a TE points in the counterclockwise direction, we classify the TE as a counterclockwise (CCW) element.

When we proceed around the loop in the clockwise direction, the gate-to-emitter voltage of a counterclockwise element corresponds to a voltage increase, whereas the gate-to-

emitter voltage of a clockwise element corresponds to a voltage drop. Hence, by applying Kirchhoff's voltage law around the loop of TEs in Figure 4, we have that

$$\sum_{n\in CCW} V_n = \sum_{n\in CW} V_n \tag{16}$$

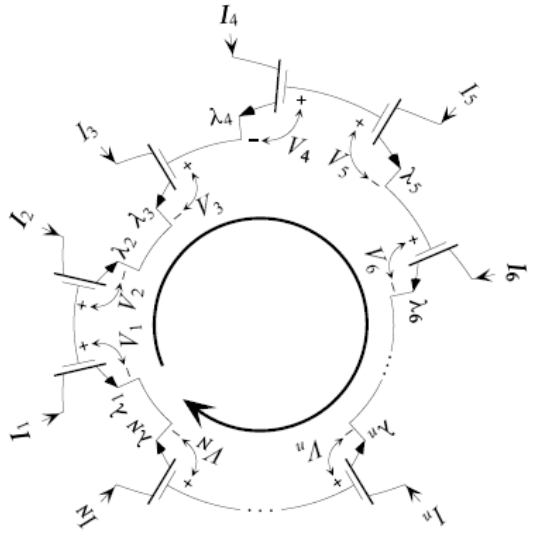

Figure 4. A conceptual translinear loop comprising N ideal TEs. The large arrow shows the clockwise direction around the loop. If a TE symbol's emitter arrow points in the direction opposite to that of the arrow, then we consider the element a counterclockwise element. If a TE symbol's emitter arrow points in the same direction as the large arrow, then the element is a clockwise element. The translinear principle states that the product of the currents flowing through the clockwise elements is equal to the product of the currents flowing through the counterclockwise elements.

By solving Eq. 14 for V in terms of I and substituting the resulting expression for each V_n, Eq. 16 becomes

$$\sum_{n\in CCW} \frac{U_T}{\eta} \log \frac{I_n}{\lambda_n I_S} = \sum_{n\in CW} \frac{U_T}{\eta} \log \frac{I_n}{\lambda_n I_S} \tag{17}$$

Assuming that all TEs are operating at the same temperature, the common factor of U_T/η in all of the terms in Eq. 17 is canceled.

$$\sum_{n\in CCW} \log \frac{I_n}{\lambda_n I_S} = \sum_{n\in CW} \log \frac{I_n}{\lambda_n I_S} \tag{18}$$

Eq. 18 is rewritten using the log characteristic $\log x + \log y = \log xy$

$$\prod_{n \in CCW} \frac{I_n}{\lambda_n I_S} = \prod_{n \in CW} \frac{I_n}{\lambda_n I_S} \tag{19}$$

By exponentiating both sides of Eq. 19 we get

$$\prod_{n \in CCW} \frac{I_n}{\lambda_n I_S} = \prod_{n \in CW} \frac{I_n}{\lambda_n I_S} \tag{20}$$

which we can rearrange to obtain

$$\prod_{n \in CCW} \frac{I_n}{\lambda_n} = I_S^{N_{CCW} - N_{CW}} \prod_{n \in CW} \frac{I_n}{\lambda_n} \tag{21}$$

where N_{CCW} and N_{CW} denote respectively the number of counterclockwise elements and the number of clockwise elements. If $N_{CCW} = N_{CW}$, then Eq. 21 reduces to

$$\prod_{n \in CCW} \frac{I_n}{\lambda_n} = \prod_{n \in CW} \frac{I_n}{\lambda_n} \tag{22}$$

which has no remaining dependence on temperature or device parameters. Eq. 22 is the translinear principle, which can be stated as follows.

> *In a closed loop of ideal TEs comprising an equal number of clockwise and counterclockwise elements, the product of the (relative) current densities flowing through the counterclockwise elements is equal to the product of the (relative) current densities flowing through the clockwise elements.*

If each TE in the loop has the same value of λ, then Eq. 22 becomes

$$\prod_{n \in CCW} I_n = \lambda_n^{N_{CCW} - N_{CW}} \prod_{n \in CW} I_n \tag{23}$$

which, if $N_{CCW} = N_{CW}$, further reduces to

$$\prod_{n\in CW} I_n = \prod_{n\in CCW} I_n \tag{24}$$

Eq. 24 is an important special case of the translinear principle that can be stated as follows.

> *In a closed loop of identical ideal TEs comprising an equal number of clockwise and counterclockwise elements, the product of the currents flowing through the counterclockwise elements is equal to the product of the currents flowing through the clockwise elements.*

3. VLSI implementation of Izhikevich's neuron model

3.1 Why Izhikevich's model?

The mathematical complexity of Hodgkin-Huxley model helps to fully describe the firing nature of a real neuron. Unfortunately, the same feature can be a burden in silicon neuron implementation of a neuron and possibly of a neural network in the future, due to increased complexity of the circuit. Hence, for the circuit implementation, it is required to have a model which is simple enough, yet is able to describe the firing behavior of a neuron without much deviation or error. Izhikevich's model is simpler than Hodgkin-Huxley model, and can express different neuron characteristic by varying the parameters in the equation.

3.2 Equation sensitivity and variable range analysis

In order to map the equations in to analog hardware, it is essential to know what effect the various parameters will have on the dynamics of the equations. Variations can be caused due to device, process, voltage and temperature as well as imperfect matching and second order effects like channel modulation which can cause un-intended non-linearity. In the analog domain, every operation is subject to imperfections as well as noise.

It is important to analyze the ranges that the variables can take so as to simplify the final circuit. The four variables (a, b, c, d) and the two state space variables (u, v) can take

on both positive as well as negative values. Designing a circuit for positive and negative variables adds complexity, increasing area and power consumption.

A simple analysis of the equations indicates that the v^2 term will be most sensitive to

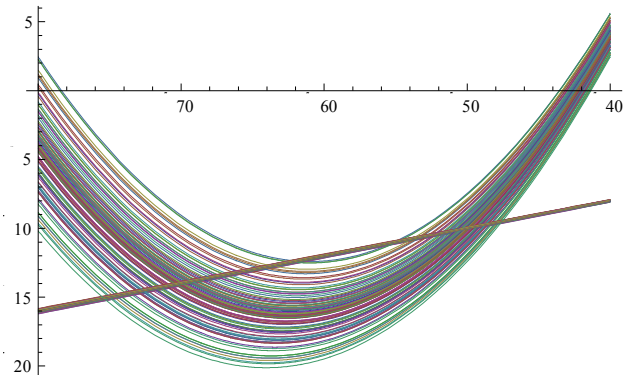

Figure 5. Nullclines due to the variation of the coefficient of v^2 term. The value is varied with 0.04 mean, and 0.0004 sigma.

variations due to the multiplicative effect of the large v value. A Monte-Carlo analysis of the coefficient of the v^2 term indicates the sensitivity of the nullclines to parameter variations. Figure 5 shows the nullclines of the model when the coefficient of the v^2 varied from 0.04, with 0.0004 sigma. As predicted, even the small change in the coefficient can cause drastic change, and can lead to behavior change to spiking without any input.

One way to reduce this dependence is to move the whole state space over to a region where the absolute value of v is small, i.e., near the origin. A simple translation of state space will have no effect on the dynamics and has the beneficial side effect of giving control of u and v variables allowing them to be forced to be positive. Further analysis will need to be done in order to quantify the effects of the changes to other operating modes of the equations.

A subset of the simulation of the effect of the parameter variation shown in Figure 6 proves that even minor changes in parameters can have a seemingly large effect on the dynamics of the circuit. Further analysis will need to be done in order to identify the parts of the circuit most sensitive to changes. It is anticipated based on discussions with the

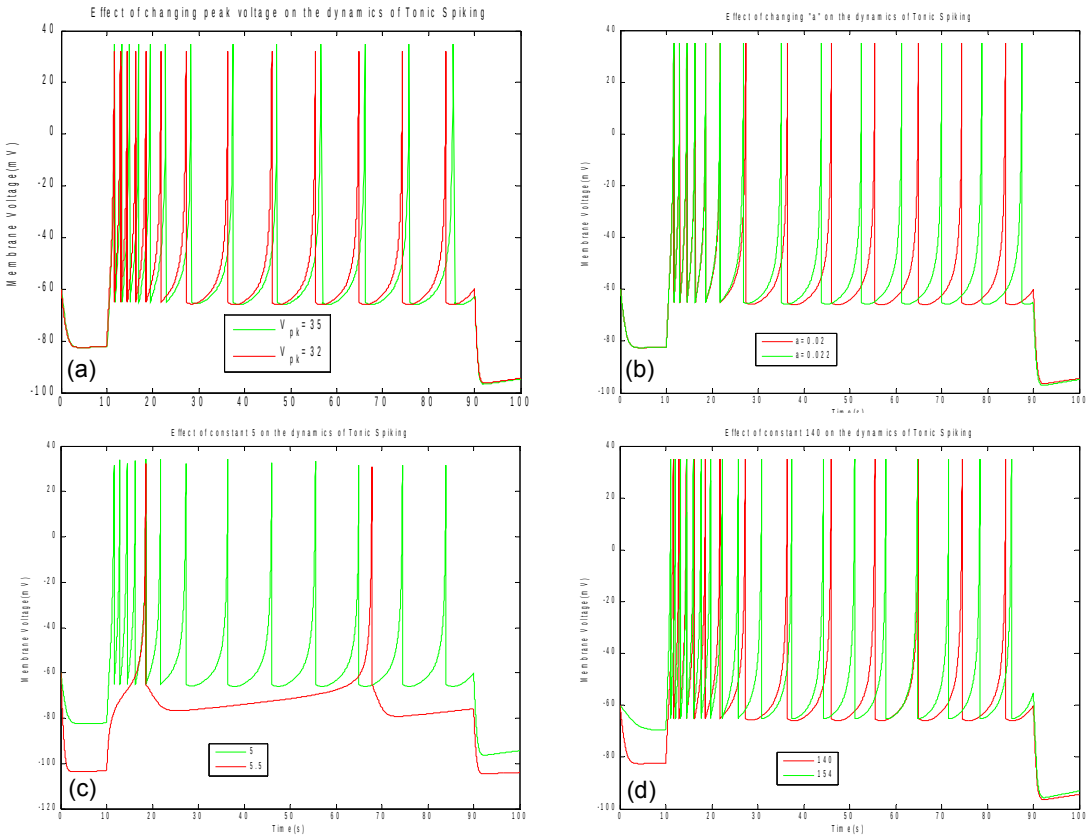

Figure 6. The membrane voltage output is plotted with different parameter variations. (a) the threshold value for the membrane voltage, (b) the parameter a in the u' equation, (c) the coefficient of v term in the v' equation, and (d) the constant in the v' equation.

author of the model that the network will exhibit some degree of robustness to parameter changes as long as the changes are not very large. This view needs to be proven with rigorous analysis as well.

3.3 Implementation of an ordinary differential equation using log-domain filter

To implement the ordinary differential equations in Eq. 11 and Eq. 12, we used log-domain circuit shown in Figure 7.

With Kirchhoff's current law applied at the node V_{xu}, we can obtain

$$C\frac{dV_x}{dt} = I_2 + I_3 - I_5 \tag{25}$$

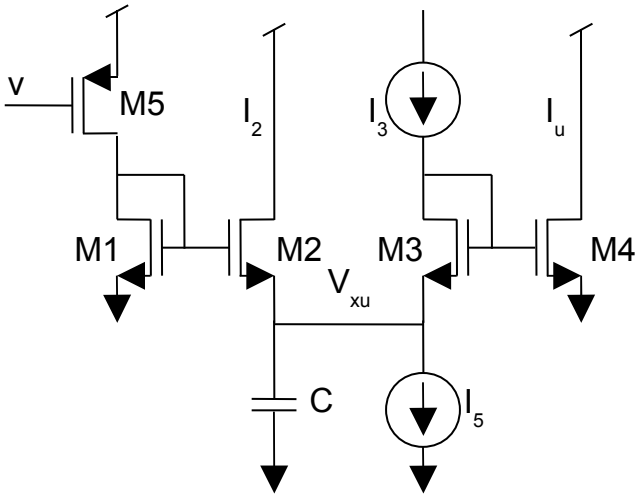

Figure 7. Log-domain filter implementing channel kinetics $\frac{dn}{dt} = \alpha(1-n) - \beta n$

Also, the translinear principle expresses the relation of the currents I_1 through I_4.

$$I_1 I_3 = I_2 I_4 \tag{26}$$

Since the MOS transistors are working in the subthreshold region, the exponential relation between the gate voltage and the output current gives us

$$C\frac{dV_x}{dt} = \frac{I_3}{I_4}\frac{d}{dt}\left(\frac{I_4}{I_3}\right) \tag{27}$$

Using Eq. 25 to Eq. 27, we can derive an ordinary differential equation with the currents in the circuit as variables.

$$C\frac{d}{dt}\left(\frac{I_4}{I_3}\right) = I_1 + \frac{I_4}{I_3}(I_3 - I_5) \tag{28}$$

If we fix I_3 to be a reference current I_{ref}, Eq. 28 is now the ordinary differential equation with variable I_4.

In the next session, we will discuss how we implemented Eq. 11 and Eq. 12 using the log-domain filter more precisely.

3.4 Circuit Implementing u'

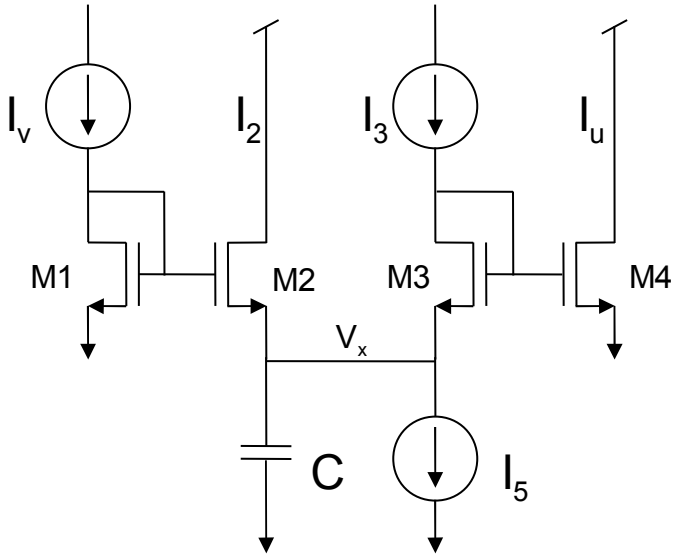

Figure 8. Circuit to implement ODE for u

To implement the relationship

$$\frac{du}{dt} = a(bv - u) \tag{29}$$

using the aforementioned translinear circuit, we must find a way to manipulate the variables of the equation describing that circuit such that its behavior closely matches that of u. We can distribute the parameter a in the u' equation to arrive at

$$\frac{du}{dt} = ab \cdot v - a \cdot u \tag{30}$$

Given that

$$\frac{dI_u}{dt} = \frac{I_1 \cdot I_3}{C} - \frac{I_u}{C}(I_5 - I_3) \tag{31}$$

governs the behaviors of the currents in our dynamic translinear circuit, we can let I_v represent v and I_u represent u, and set

$$\frac{(I_5 - I_3)}{C} = a \tag{32}$$

and

$$\frac{I_3}{C} = a \cdot b \qquad (33)$$

As long as we set the values of capacitor C and the input currents I_3 and I_5 according to these relationships, we will find that our circuit will accurately emulate the behavior of u.

3.5 Circuit Implementing v'

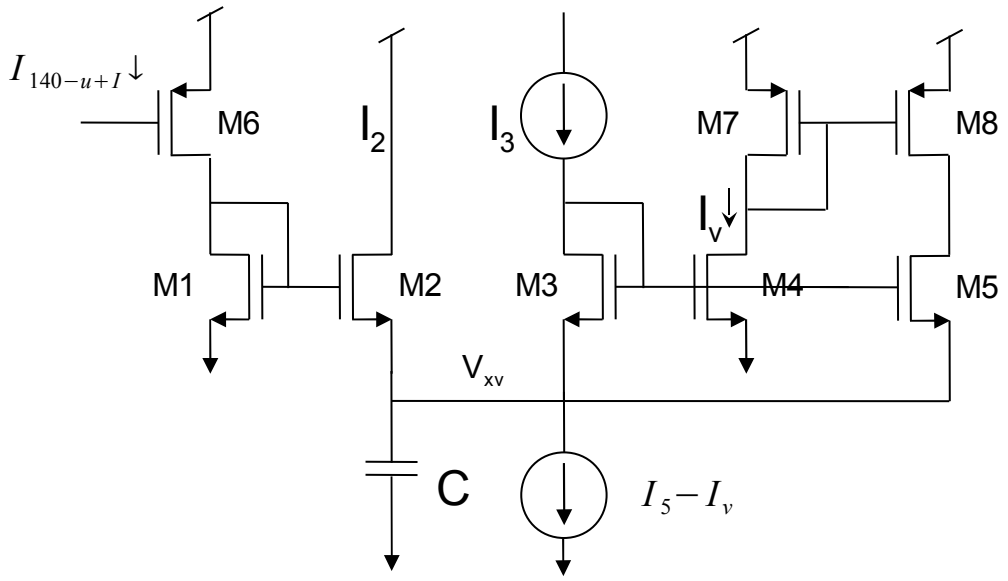

Figure 9. Circuit to implement ODE for v

To implement the relationship

$$\frac{dv}{dt} = 0.04v^2 + 5v + 140 - u + I \qquad (34)$$

with our dynamic translinear circuit, we can follow a similar methodology as we did in the case of u. We set

$$\frac{I_1}{C} = 140 - u + I \qquad (35)$$

and

$$\frac{I_3}{C} = 5 \qquad (36)$$

which will accommodate the "5v" term. We must make a small modification to our circuit to implement the v^2 term. By making I_5 a linear function of I_v, such as

$$\frac{I_5}{C} = 0.04(I_{ref} - I_v) \qquad (37)$$

we can emulate the v^2 term, where I_{ref} corresponds to an offset current. This relationship can be implemented simply by mirroring current I_v directly into the capacitor, as shown in figure.

3.6 V-Reset Circuit

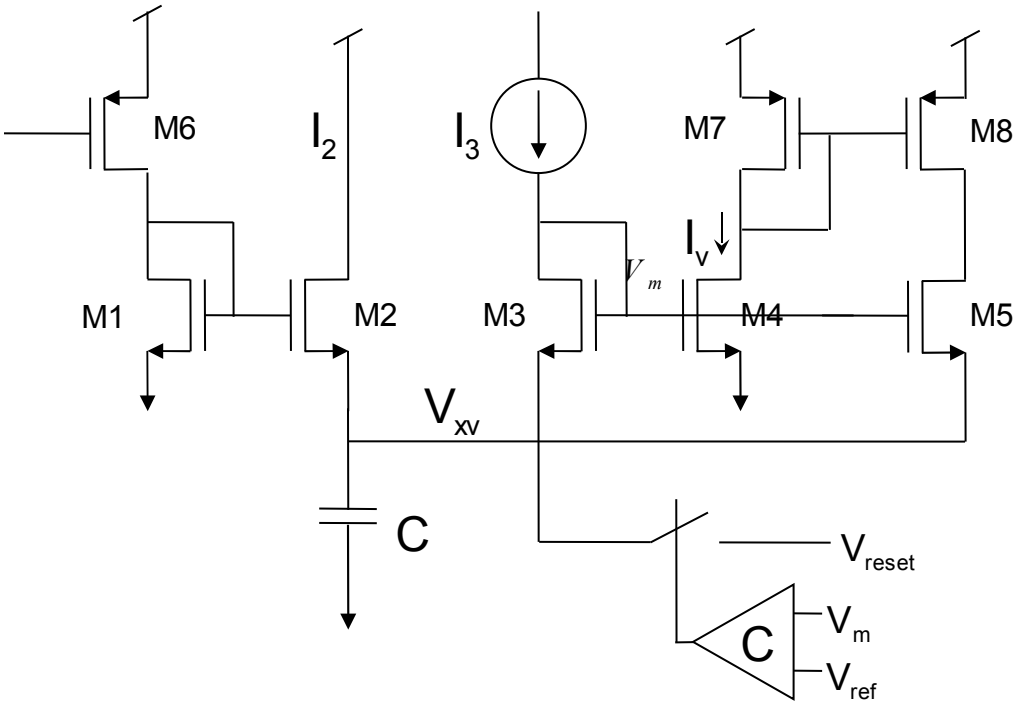

Figure 10. Circuit to reset v after it exceeds a threshold

Implementing a circuit to reset v when it reaches a certain threshold, i.e.

$$\text{if } V_m > V_{ref}, \text{ then } V_m \leftarrow V_{reset}$$

is a relatively simple task. We use a comparator circuit to detect whether current v has exceeded a certain level, and if it has, we close a switch connected between the capacitor and a reference voltage, whose specific value determines the value of parameter c. This causes the

current v to drop rapidly, settling at the value c.

3.7 U-Incrementing Circuit

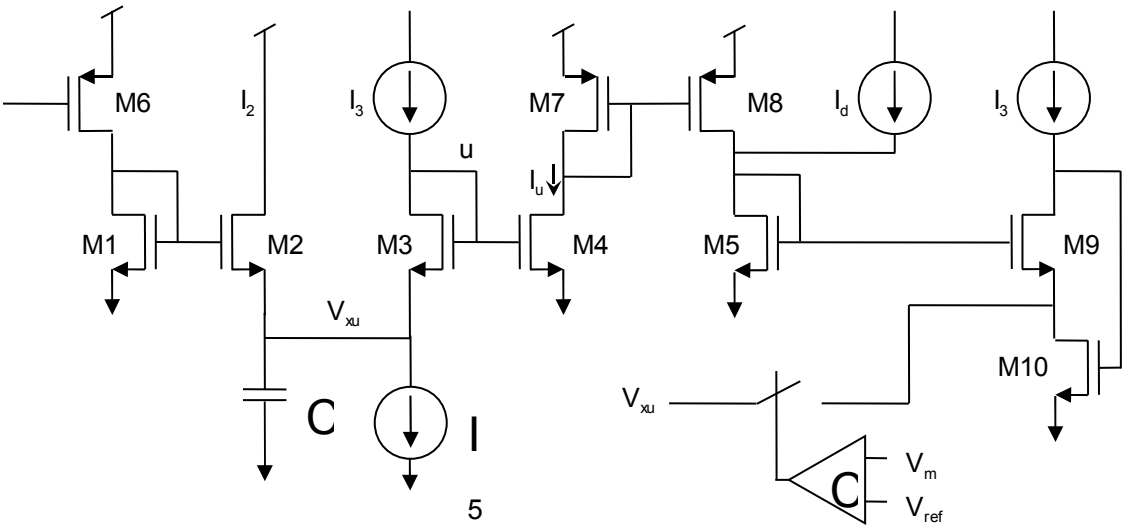

Figure 11. Circuit to increment u after v exceeds a threshold

To change the value of u, we must change the voltage across the capacitor in the translinear u-circuit. This new voltage needs to alter the current u such that it becomes the previous value of u, incremented (or decremented) by an amount d. Our basic plan is to establish a voltage elsewhere in the circuit, which, were it present on the capacitor, would produce the properly incremented value of current u. To achieve this, we mirror the current u and add to it a current d, passing this new current through a diode-connected MOS transistor, M5. This establishes a gate voltage which corresponds to the incremented current, u+d, as long as the source voltage is 0. This voltage is then connected to the gate of another MOS transistor, M9 whose drain is supplied with current I_b. (Its source is connected to a biasing transistor, M10.) With this configuration, we have essentially set up a situation equivalent to that of transistor M3, but with a different gate voltage. It follows that because the gate voltage on transistor M9 corresponds to a current of u+d, and since it is passing current I_3, that it's source

voltage should change to accommodate that current; a voltage which, were it to become present on the capacitor, would cause current u to become u+d. This could be achieved fairly easily by using a voltage buffer and a switch connected to the source of transistor M9, which would feed into capacitor C. The switch would be closed momentarily each time v was reset (when a spike occurred). The voltage buffer would need to be able to supply (and sink) enough current to be able to overcome all the other currents involved with the capacitor in order to force the voltage on that capacitor to change very rapidly and to settle precisely on the desired value.

Although the concept of this circuit seems to be correct, we encountered trouble when trying to simulate it. We found that there was always a significant error present in the voltage on the source of transistor M9, and we are not yet sure of the cause.

3.8 Design Compromises

The two most difficult problems we faced during the design process were the precise implementation of the u-increment event, "u←u+d", and the representation of negative values using always-positive currents. Fortunately, the first problem can be partially bypassed, as there do exist some types of neurons in the Izhikevich model where the parameter d is 0. Thus, for these cases, we can ignore the u-incrementing circuit altogether, but still observe spiking and the dynamic behavior of u.

Further, in some cases where d is 0, every other parameter is positive and u and v do not have to change signs; therefore we do not have to worry about enabling any of the variables to represent both positive and negative values.

3.9 Results

After verifying that all of the previously mentioned circuits function as they should, we constructed a circuit to emulate the entire neuron, combining the u', v', and reset circuits.

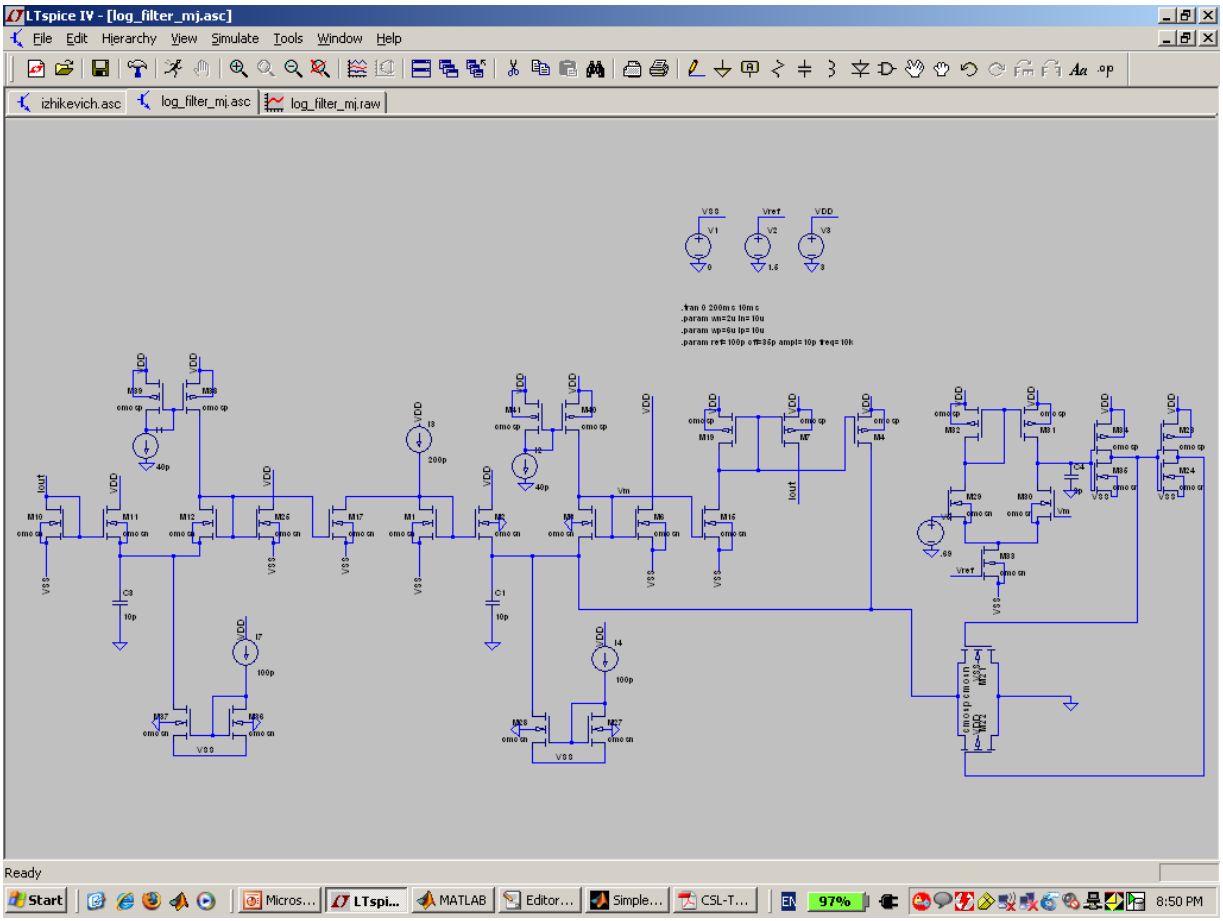

Figure 12. Entire neuron circuit, implemented in LTSpice

Taking our design compromises into consideration, we aimed at emulating a Class-2 type neuron. This type of neuron, modelled using the Izhikevich model in Matlab, produces the following behaviors of u and v:

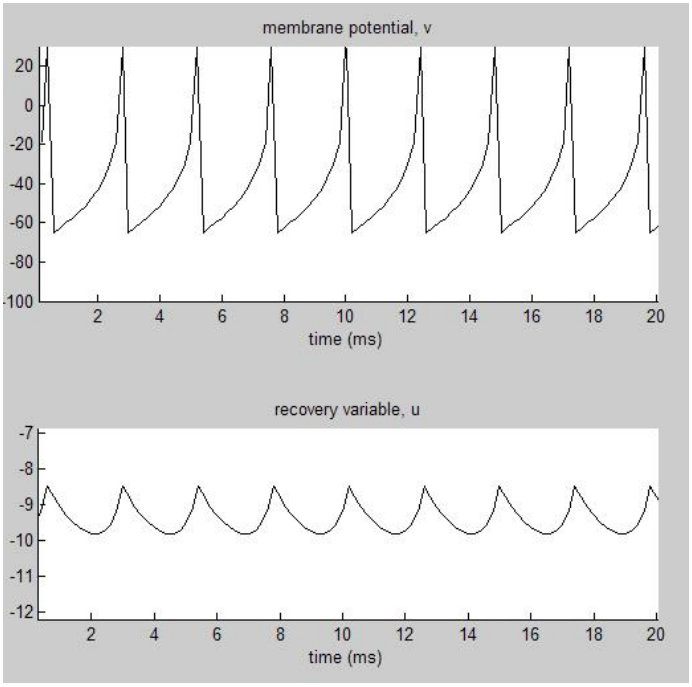

Figure 13. Matlab simulation of Class-2 neuron, using the Izhikevich model

After simulating our circuit in LTSpice, we were happy to find that our results closely matched those of the Matlab simulation:

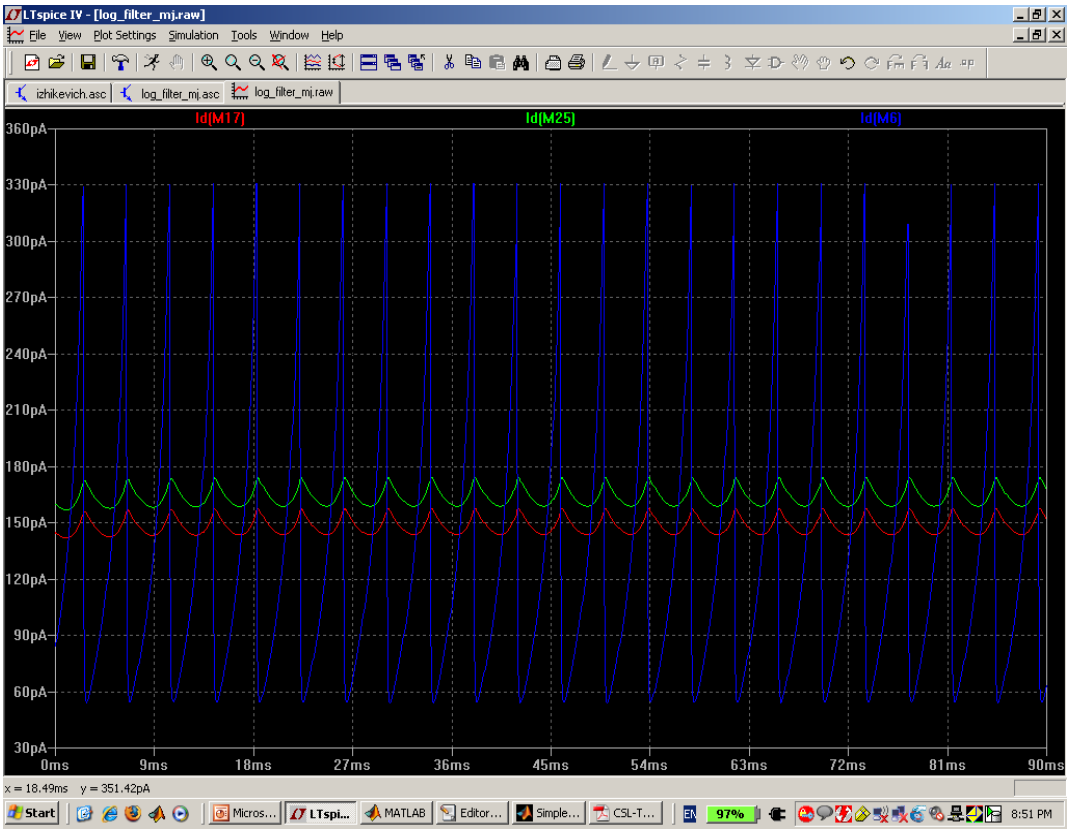

Figure 14. LTSpice simulation of Class-2 neuron, using circuit in fig. 12

Here, the blue trace represents the v current, and the green trace represents the u current. (The red trace is the actual u current that is being injected into the v' translinear circuit. The offset is not of large importance here.) The exponential shape of each spike in v is quite apparent; likewise, our circuit's u curve has nearly exactly the same shape as the curve produced by the Matlab simulation. These results demonstrate that the translinear circuits we have used do indeed implement the u' and v' equations quite accurately.

4. Future Work

In future designs, one of the most critical problems will be to design a circuit to effectively implement the u-incrementing event, "u←u+d". This is necessary if we desire a neuron circuit which is capable of emulating all the types of neurons which the Izhikevich model is capable of emulating. One solution may be to simply tweak the aforementioned circuit until it works effectively. Whether or not this is a practical scheme, we do not yet know.

Another way to increment u could be to use a precise charge-injecting circuit, which would quickly inject a constant amount of charge into the u-circuit capacitor every time v is reset. The specific amount of charge injected at each reset event would be proportional to the parameter d. Although this would be relatively simple to implement and may work for many types of neurons, it would not give us a completely accurate emulation of the " u←u+d" event, because of the exponential relationship between the gate voltage and current in a MOS transistor. If we were to test that circuit, we would notice that d would appear increase exponentially as u becomes larger. However, it is important to note that this may not be an undesirable effect – the original Izhikevich model was designed to be implemented on a computer, on which the "u←u+d" event requires very little time and computational resources. A u-increment with an exponential term (such as, in our case, $u \leftarrow u+d \cdot e^{u}$) requires far more time to compute, but might produce an even more useful model overall. This exponentially adjusted u-increment would be very simple to implement in our circuits, so it could be the case that analog VLSI is an even more ideal medium in which to implement the (slightly modified) Izhikevich model than are digital electronics. (Of course, this is only speculation – whether or not an exponential u-increment term would improve the dynamics of the Izhikevich model is a question which would need to be answered through further studies.)

Another crucial addition to our design will be a way to allow all the variables to take both positive and negative values. Because all of the variables and parameters in our circuit are represented by currents which cannot be negative, one possible solution is to use offset currents to establish a positive current value which represents the value “0”. Although we investigated this scheme during our design process, we found it to be surprisingly difficult to implement. We were unable to find, analytically, values of offset currents which would allow us to efficiently emulate all types of neurons. This problem could be the subject of further investigation. (See Minchn paper on translinear circuits)

There exist other schemes for representing positive and negative values using all-positive currents, but as of yet we have not deeply investigated any of those circuits.

As our stability analysis shows, precise control of all of the coefficients in the u' and v' equations is crucial in order to keep the model working within acceptable levels of variation. The coefficient of the v^2 term, “0.04”, is especially sensitive to variation. The problem of controlling currents and voltages precisely is inherent to analog electronic design, as manufacturing variation between individual components, changes in temperature, and electrical noise are all unavoidable external factors which cause unwanted circuit behavior. Using larger transistors or larger current levels would cause the effects of device imperfections and noise to become less pronounced, but would lower the number of neuron circuits that could fit on a single chip, and would cause the chip to consume more power. These trade-offs would have to be investigated experimentally in order to come to an optimal design. However, it could also be argued that some degree of noise is desired, as systems of biological neurons do exhibit some natural noise as well.

It should be noted that one method of minimizing the effects of noise in the v^2 coefficient is to offset all the variables so that v is reset to a value close to 0, rather than a negative number such as -70. This would cause v^2 to be small while the neuron is not spiking, so small fluctuations in the coefficient “0.04” would produce much less pronounced effects on the neuron's behavior. Of course, the error would soon become large as v rises, but this may not be much of a problem, because once v becomes large enough, the neuron will usually spike and reset so quickly that variations in the coefficient “0.04” will have very little time to produce significant adverse effects on the dynamics of the system.

A last addition to our circuit could be a system by which multiple chips could be connected together, thus creating a highly customizable device to simulate large networks of a wide variety of types of neurons with interconnecting synapses. This system would be necessary to realize the full potential of the Izhikevich model in simulating nearly any system of biological neurons. It would require the addition of spike-detecting external circuitry which would also govern all synaptic events and control time and activity-dependent phenomena such as long-term potentiation or depression.

5. Reference

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