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Beyond address-event communication: dynamically-reconfigurable spiking neural systems

Large-scale artificial sensory information-processing systems that emulate biological intelligence when interfacing with their surroundings have been the holy grail of neuromorphic engineering. The effort of our community has concentrated on modeling neural structures and adaptive mechanisms in biology as much as it has on efficient implementation in real-time micropower hardware.

However, despite steady advances in the scaling of VLSI technology, which promises to deliver more transistors on a single chip than neurons in our brain, it is neither feasible nor advisable to integrate the full functionality of a complete nervous system on a single chip. Early experimentation with neuromorphic systems revealed the need for a multi-chip approach and a communication protocol between chips to implement large systems in a modular and scalable fashion. Thus, the address-event representation (AER) protocol was developed over a decade ago and quickly became a universal 'language' for neuro-morphic engineering systems to communicate neural spikes between chips.[1-7] However, AER is now used for functions in addition to inter-chip communication. The *Silicon Cortex* project proposed using AER to connect detailed compartmental models of neurons and synapses on multiple chips,[8,9] and a few different groups have used AER to implement synaptic connectivity.[4-7]

Here we will concentrate on our integrate-and-fire array transceiver (IFAT) chips, which can be used to implement large-scale neural networks in silicon with both synaptic connectivity and synaptic plasticity in the address-domain.[10,11] The newest IFAT chip[12] implements 2,400 silicon neurons, each with a single dynamically-programmable conductance-like synapse: both the synaptic 'conductance' and the synaptic driving potential can vary for each incoming event. Rather than hardwiring connections between cells, the network architecture and synaptic parameters are stored off-chip in a RAM-based look-up table (LUT). An external digital micro-controller (MCU) provides the appropriate signals to configure synapses and route spikes to their respective targets via an asynchronous AER bus. A block diagram of the system is shown in Figure 1.

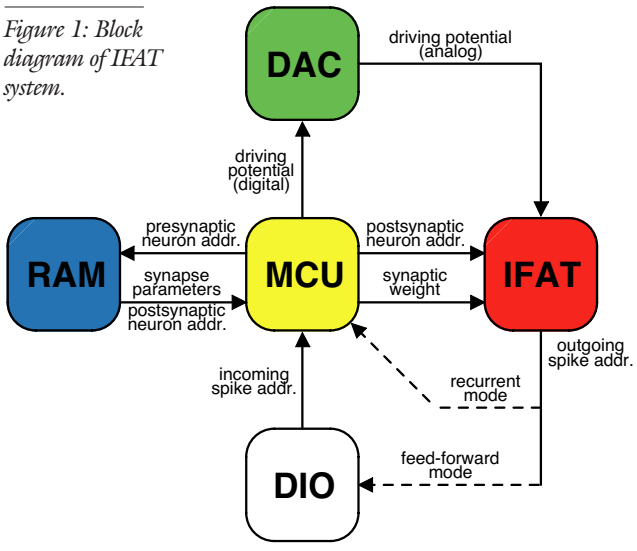

Figure 1: Block diagram of IFAT system.

During normal operation, the event-driven microcontroller is activated when a presynaptic neuron generates a spike. The cell's address is used as an index into the LUT and the data stored at that location in RAM specifies one or more postsynaptic targets with their associated synaptic weights and driving potentials. The MCU then provides signals to the IFAT to configure each synapse and sends the events serially. Any postsynaptic spikes generated by this process can either be sent back to the IFAT (in recurrent mode) or sent off-chip (in feed-forward mode), depending on the data stored in RAM. Additionally, updates to the network can be implemented by modifying the LUT according to a spike-based learning rule computed by the MCU.[11]

A printed circuit board (Figure 2) integrates the components of the IFAT system, including 9,600 neurons on four IFAT chips, 128MB of non-volatile SRAM, a high-speed 8bit voltage DAC, a 200MHz FPGA, and a 32bit digital I/O (DIO) interface. The DAC is used to control synaptic driving potentials, while synaptic weights are specified by three separate fields in the LUT: one each for the size of the postsynaptic potential, the number of events to send, and the probability of event transmission. External AER-compliant hardware or a peripheral computer interface

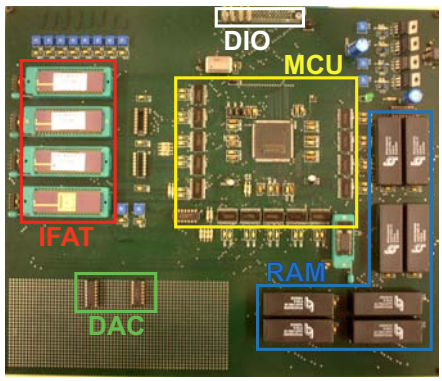

Figure 2. *Printed circuit board integrating all components of the IEAT system.*

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can communicate with the IFAT through the DIO. The system is capable of implementing over four million synapses.

Previous generations of the IFAT system[10] have served a variety of applications. For instance, Laplacian filters were implemented to isolate vertical edges on static images:[10] a task that ran two orders of magnitude faster in hardware than in simulation. Similar network architectures can be employed to compute arbitrary filter kernels by varying the pattern of lateral connections between neurons. Even more interesting applications arise by extending address-event synaptic connectivity to address-domain synaptic plasticity. We implemented spike-based learning rules by monitoring the AER bus and dynamically updating the LUT.[11] Using this strategy with a form of spike-timing dependent plasticity (STDP), we constructed a network that could detect correlated inputs and group them together. Subsequent work by other groups has demonstrated that the resulting networks are capable of preserving spike synchrony across multiple levels of neural processing.[13] Finally, we recently built rudimentary neural spatio-temporal filters and used them to process a spike train produced by an AER retina.[14] By constructing an array of similar elements and combining the appropriate outputs, it is possible to construct velocity-selective cells similar to those found in the medial-temporal cortical area (MT) of the human brain.[15]

We believe that by combining analog VLSI hardware with a digital microcontroller and RAM, reconfigurable hardware neural networks provide the 'best of both worlds': analog cells efficiently model sophisticated neural dynamics in real-time, while network architectures can be reconfigured and adapted in-site. The newest of these systems provide a number of advantages over previous designs, including more neurons, a richer parameter space, more biologically plausible dynamics, and a higher degree of inter-connectivity and plasticity. We expect them to serve as useful tools for future investigations of learning in large-scale neural networks. We invite the readers to contact us for collaborative opportunities on modeling of large-scale biological neural circuits.

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a nuisance, is certainly not common among electronic engineers. This view, inspired by emerging neurophysiological coding models, can definitely give new impulse to circuit designs.

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