Wireless Multichannel Acquisition of Neuropotentials

Mohsen Mollazadeh, Kartikeya Murari,
Helen Schwerdt, Xing Wang and Nitish Thakor
Department of Biomedical Engineering
Johns Hopkins University
Email: mohsenm@jhu.edu

Gert Cauwenberghs
Division of Biological Sciences
University of California San Diego
Email: gert@ucsd.edu

***Abstract*—Implantable brain-machine interfaces for disease diagnosis and motor prostheses control require low-power acquisition of neuropotentials spanning a wide range of amplitudes and frequencies. Here, we present a 16-channel VLSI neuropotential acquisition system with tunable gain and bandwidth, and variable rate digital transmission over an inductive link which further supplies power. The neuropotential interface chip is composed of an amplifier, incremental ADC and bit-serial readout circuitry. The front-end amplifier has a midband gain of 40 dB and offers NEF of less than 3 for all bandwidth settings. It also features adjustable low-frequency cut-off from 0.2 to 94 Hz, and independent high-frequency cut-off from 140 Hz to 8.2 kHz. The Gm-C incremental $\Delta\Sigma$ ADC offers digital gain up to 4096 and 8-12 bits resolution. The interface circuit is powered by a telemetry chip which harvests power through inductive coupling from a 4 MHz link, provides a 1 MHz clock for ADC operation and transmits the bit-serial data of the neurpotential interface across 4 cm at up to 32 kbps with a BER less than 10^{-5}. Experimental EEG recordings using the neuropotential interface and wireless module are presented.**

I. INTRODUCTION

Recent advances in the field of neural prosthesis have enabled decoding the multitude of electrical activity in the brain to understand neural mechanisms underlying movement [1], [2]. Neural signals occupy a wide range of signal frequencies and amplitudes, from Hz to kHz and from μV to mV. Action potentials, the electrical activity of a single neuron, occupy a bandwidth of 8 kHz and have an amplitude of 500 μV. Recording spike activity from a population of neurons offer basic understanding underlying brain mechanism such as motor movements. However, microelectrodes need to be implanted in the brain to acquire these signals adding to the complexity associated with these recordings. On the other side of neural spectrum, electroencephalogram (EEG) is a representation of the electrical activity of the brain as recorded on the scalp. EEG signals are much weaker and slower than their spike counterparts, typically 50 μV in amplitude and up to 100 Hz in frequency. EEG does not represent the exclusive activity of cortical regions below the electrodes because of volume conduction in the brain, which non-linearly adds single neuron activities. Inspite of their poor spatial resolution, a number of signal processing techniques have been developed to decode brain intent from EEG signals. These efforts demonstrate the possibility of control of a high degree of freedom prosthetic device using EEG signals.

Due to the noise, power, cost and footprint advantages of integrated systems, several VLSI systems have been developed for wired/wireless acquisition of neural signals [3]–[5]. For example, A wireless 100 channel system for recording single unit activity was reported by Harrison *et al.* [6]. The system uses a 2.64 MHz inductive link to receive power and commands and telemeters the digitized data over a 433 MHz FSK link. The amplifier has an input-referred noise of 5.1 μV_{rms} while consuming 13.5 mW of power. Denison *et al.* [7] reported a neural amplifier for extraction of biomarkers which uses chopper stabilization to reduce input-referred noise of the amplifier. A 200 μW, 8 channel ASIC for ambulatory EEG monitoring was presented by Yazicioglu *et al.* [8]. Chae *et al.* [9] also reported a system with real time spike detection and an Ultra Wide Band (UWB) transmitter for acquisition of neural signals.

Here, we present a 16-channel integrated neuropotential interface chip with adjustable filtering, amplification and digitization covering the entire spectrum of neural signals. The system was powered by a telemetry chip previously designed in our lab [10] which harvests power from a 4 MHz inductive link. The telemetry module was also used to transmit low frequency neural data (EEG, ECoG) over the same link back to the base station. The two chips were fabricated in a 0.5 μm 2 poly, 3 metal CMOS process and the system maintained low-noise and low-power performance during wireless operation. Characterization results and *in-vivo* data are presented.

II. SYSTEM ARCHITECTURE

The functional block diagram of the wireless neural acquisition system is shown in Fig. 1. The interface chip has 16 parallel channels each comprising of a fully differential band-pass filtering two-stage voltage amplifier, a Gm-C incremental $\Delta\Sigma$ ADC, a decimating counter, and a daisy-chained parallel-to-serial output register. The wireless chip supplies power and clock to and transmits data from the neuropotential interface chip using inductive coupling via a 4 MHz link. The chip consists of a rectifier, two voltage regulators and circuits for clock recovery and data modulation [10]. The base station transmission coil voltage is driven by a high efficiency class-E transmitter. On the receiving side, an off-chip coil feeds into a full wave rectifier, followed by a low pass filter and two separate regulators, to generate two 3.3 V supplies for the chip operation. Two supplies were used to decouple digital noise from the analog circuits. A clock recovery block extracts a 4 MHz clock that is stepped down to 1 MHz for the ADC operation. The NRZ format digitized data is transmitted back

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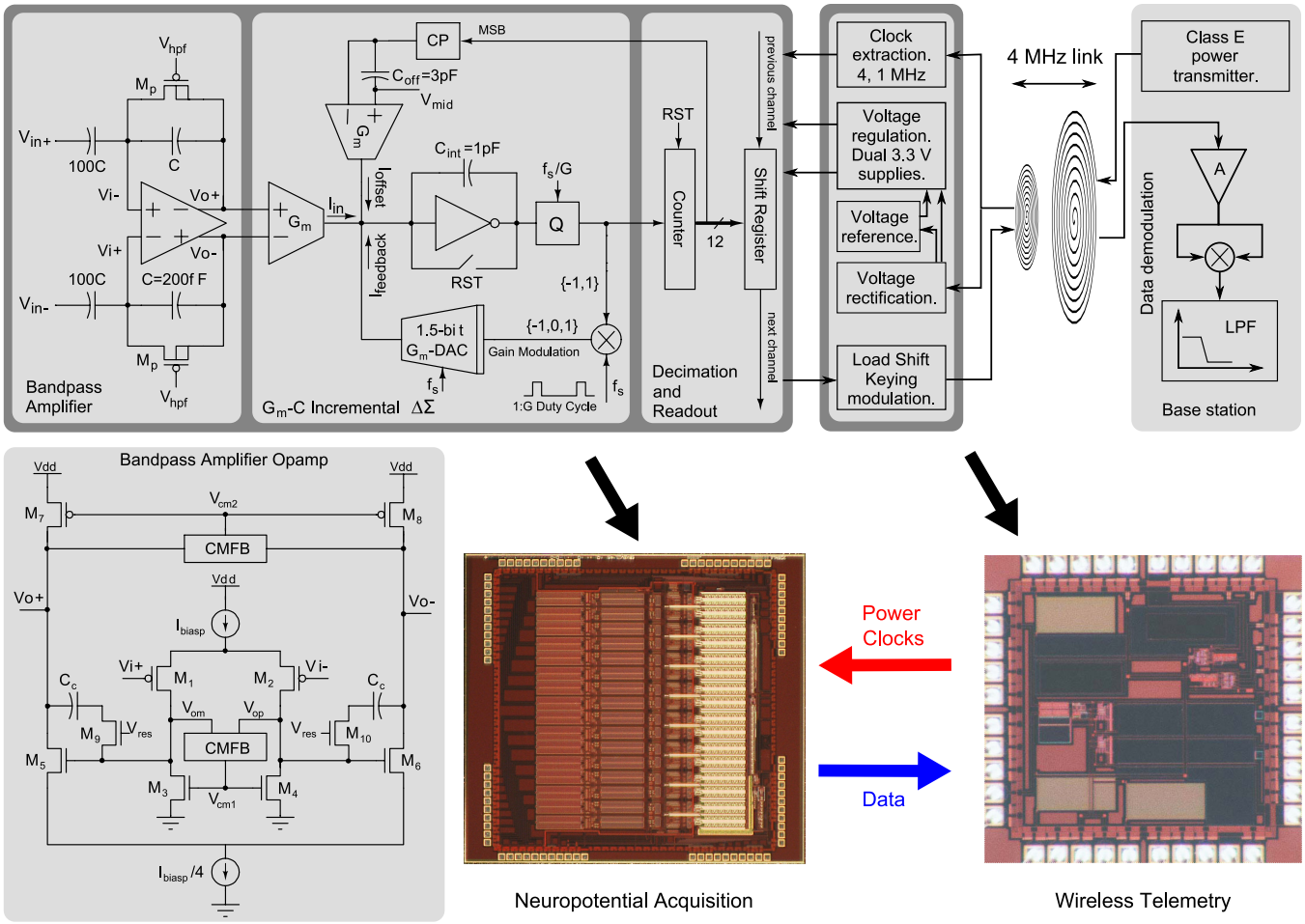

Fig. 1. Block diagram of wireless neuropotential acquisition system and the micrographs of the fabricated neuropotential acquisition and wireless telemetry chips. Circuit diagram of the bandpass amplifier in the interface chip is shown in the bottom left of the figure.

through the same link via Load Shift Key (LSK) modulation. At the base station, the received data is buffered, squared and low pass filtered to perform coherent demodulation.

In the interface chip, the amplifier midband gain is set to 40 dB by ratioed poly1/poly2 capacitors ($100C$=20 pF and C=200 fF). The PMOS transistors M_p in the feedback loop provide a large resistance in the TΩ range for sub-Hz cutoff highpass filtering [4]. Tuning their gate bias, V_{hpf}, changes their resistance, which in turn adjusts the sub-hertz cutoff high pass filtering and AC coupling of the input. The low pass filter cutoff frequency can be tuned for various modalities of neural signals by changing the g_m of the front-end amplifier which results in a change in its unity gain frequency.

The circuit implementing the fully differential two-stage voltage amplifier in the frontend amplifier is detailed in Fig. 1. Very wide (W/L = 216μ/1.8μ) input PMOS transistors M_1 and M_2 permit weak inversion operation over a range of bias currents I_{biasp} to maximize transconductance and hence minimize thermal noise. Large gate area sizing of M_1 and M_2 also partially mitigate the 1/f flicker noise. Likewise, second stage input transistors M_5 and M_6 were sized (W/L = 18μ/1.8μ) for weak inversion to minimize thermal noise, but at significantly lower bias currents. The attenuation of second stage input-referred noise by the first stage gain affords this lower current, and leads to significant savings in power consumption. The first and second stage bias currents are set in a constant ratio of 4:1 for an overall single-pole lowpass response of the two-stage amplifier. The unity gain frequency of the amplifier $g_m/2\pi C_c$ is set by the transconductance of the first stage g_m proportional to the bias current I_{biasp}, and by C_c = 15 pF. Active resistors M_9 and M_{10} were inserted to null the zero and non-dominant pole in the second-order response. Both stages have independent common mode feedback circuitry, CMFB (Fig. 1). The advantage over previous two-stage amplifier designs is superior noise efficiency approaching that of a single-stage single-ended amplifier, with reduced input-referred noise and lower power contributed by the second stage and common-mode feedback.

The ADC was implemented using a continuous time Gm-C, incremental ΔΣ (Fig. 1). Each channel has a dedicated ADC for low clock speed operation reducing the power consumption. The ADC is configured in current-mode to in-

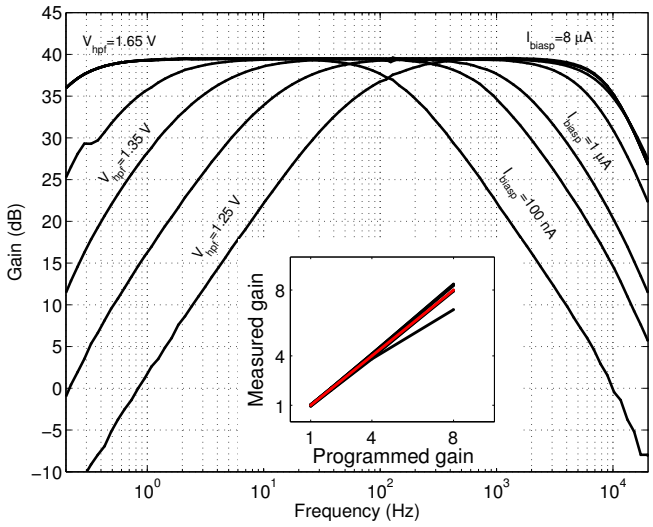

Fig. 2. Bandpass amplifier responses for lowpass current bias I_{biasp} between 100 nA and 8 μA, and for highpass voltage bias V_{hpf} between 1.25 V and 1.65 V. The inset shows the normalized measured gain versus programmed gain for multiple channels. The red trace is the ideal unity slope line.

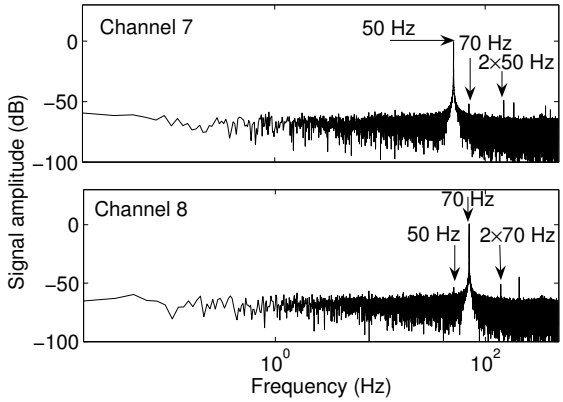

Fig. 3. Normalized power spectra of the recorded digital output for two adjacent channels. 1 mV 50 Hz and 70 Hz sine waves were presented to the channel 7 and 8 of the interface respectively.

corporate a time modulation feedback which allows a digitally programmable gain between 1 and 4096. The structure also allows configuration of the ADC resolution [11]. In order to remove any offset in the digitized output caused by mismatch in the ADCs, a charge pump based circuit adaptively adds or subtracts a small current from the OTA based on the output of the ADC. The digital output is decimated using a first order comb filter and read out from a parallel-in serial-out shift register.

III. EXPERIMENTAL RESULTS

The neural interface and wireless power harvesting and data telemetry blocks were fabricated separately in a 0.5 μm 3M2P CMOS process through the MOSIS foundry service. The 16 channels of neural interface occupy 3 mm $\times$ 3 mm of silicon area and consume 1.8 mW of power at the maximum bandwidth and speed (8.2 kHz and 16 kS/s). Each block of the system was characterized independently. For characterizing the system and *in vivo* recordings, the digital output (or demodulated data) of the chip was acquired using a DAQ card (National Instruments, Austin, TX) and read into a computer.

A. Neuropotential Interface

Measured gain and bandwidth of the closed-loop bandpass amplifier are shown in Fig. 2. The midband gain was 39.6 dB. The lower cutoff frequency could be varied between 0.2 Hz to 94 Hz by tuning V_{hpf} from 3.3 to 1.25 V. The higher cutoff frequency was adjustible from 140 Hz to 8.2 kHz by tuning I_{biasp} from 0.1 to 8 μA. The inset figure plots measured vs programmed gain of all channels showing mismatch in the system channels and the deviation from the digitally programmed gain in the ADC stage. The gain was set to 1, 2, 4 and 8 and the input sine wave amplitude was halved each time. The ADC resolution was changed from 12 to 9 bits to maintain the sampling rate. The red trace is the ideal unity slope line.

The amplifier's CMRR and PSRR were larger than 76 dB for inputs between 1 Hz and 10 kHz at an electrode offset of 50 mV. The amplifier THD was below 1% for inputs within 9.4 mV_{p-p}. For the 8.2 kHz bandwidth (I_{biasp} = 8 μA and V_{hpf} = 3.3 V), the amplifier had a thermal noise level of 18 nV/$\sqrt{Hz}$ and a 1/f noise corner at 1 kHz. Integration of the PSD for this bandwidth yielded an input-referred noise of 1.94 μV_{rms} and a noise efficiency factor (NEF) of 2.9. Decreasing the amplifier bias to the lowest level (I_{biasp} = 100 nA) resulted in higher thermal noise level but lower 1/f corner frequency, with an input-referred noise of 1.65 μV_{rms} and an NEF of 3.2.

Fig. 3 shows the power spectra of the recorded digital output of two adjacent channels. The data indicate a THD of 0.5%, and a digital output noise of 1.1 LSB and more than 55 dB crosstalk suppression. Lower quantization noise levels can be attained by higher gain setting for smaller signal amplitudes.

B. Wireless Power Harvesting and Telemetry

A transponder coil of 1 cm radius was used to receive power and clock using inductive coupling at 4 MHz from a reader coil of diameter 2.5 cm. Fig. 4 shows the 3.3 V generated supply, 32 kHz data clock (generated from 1 MHz recovered clock), transmitted neural data and demodulated neural data at the base station. Stable operation of the circuit was achieved with up to 4 cm separation between the coils. Data transmission was also tested up to 32 kbps resulting in a bit error rate (BER) less than 10^{-5}. With wireless operation of the system, the channel noise increased to 2.1 LSB due to increased noise on the power supplies.

C. In-vivo Recordings

Although the neuropotential interface chip is capable of recording spike signals (8.2 kHz), the telemetry system limits the data transfer rate since the same link is used for transmitting data as well as power. For the purpose of this report,

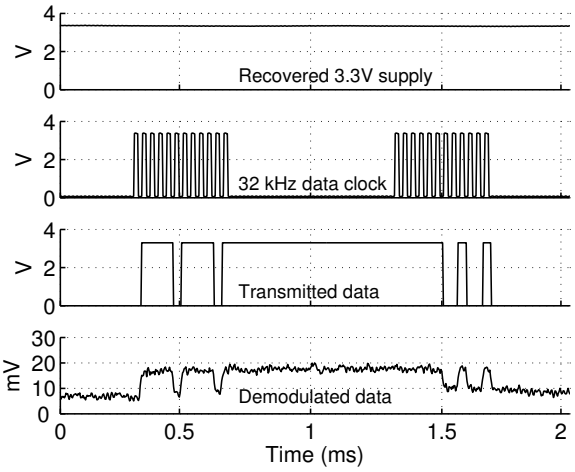

Fig. 4. RF operation: 3.3 V generated supply, 32 kHz data clock (generated from the 1 MHz recovered clock), transmitted data and demodulated data at the base station.

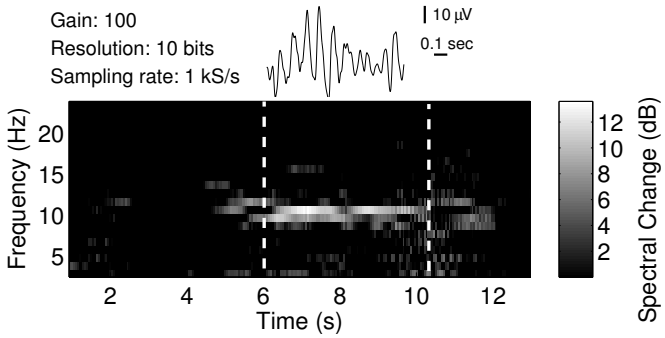

Fig. 5. Time frequency plot of the recorded EEG waveform from occipital lobe of a human subject. Dotted line shows closing and opening of the eye. The recorded EEG waveform when the eyes are closed is shown on top.

we will present EEG recordings with wireless powering and telemetry. EEG recordings were performed on a male human subject fitted with a 20-electrode cap with gel-based electrodes (Electro-Cap, Eaton, OH). The O1 electrode located above the occipital lobe was connected to the interface circuit and the subject was asked to periodically open and close his eyes for 4 s intervals. Fig. 5 shows the time frequency plot of the recorded waveform under wireless operation. Dotted lines denote the closing and opening of eye. As it can be seen, the power in the 11 Hz band (α activity) increases during eye closure.

IV. CONCLUSIONS

We have presented an integrated multichannel acquisition system for recording neural signals. Tunable filters were embedded in the amplifier front-end stage in order to selectively amplify the signal of interest. The amplifier's input-referred noise was below 2 μV_{rms}, consistently providing low-noise performance. The configurable gain and resolution setting in the ADC stage allows the optimum quantization based on the dynamic range and frequency content of the acquired signal.

TABLE I
PERFORMANCE SUMMARY OF THE SYSTEM

Amplifier	Gain	39.6	dB
	Lowpass cutoff	0.140 - 8.2	kHz
	Highpass cutoff	0.2 - 94	Hz
	THD, $v_{in} \leq 9.4mV_{pp}$	$< 1\%$	
	Noise Efficiency Factor	< 3	
Channel	Programmable gain	1-4096	
	Sampling rate	< 16	kS/s
	Noise	< 1.1	LSB
	Current draw	< 34	μA
RF operation over 4 cm & 32 kbps	Harvested power (dual supplies)	3.3	V
	Channel noise	< 2.1	LSB
	Bit error rate	$< 10^{-5}$	
Chip	Power (maximum BW & speed)	1.8	mW
	Gain mismatch	$< 5\%$	
	Crosstalk suppression	< -55	dB

The wireless power harvesting module was able to provide the power and clock for interface operation at distances up to 4 cm and transmit data up to 32 kbps rate with negligible BER. RF operation increased the input-referred noise of the system from 1.1 to 2.1 LSB. The system was used to wirelessly acquire EEG from a human subject. The performance of the system is summarized in Table I.

ACKNOWLEDGEMENT

This work was supported by NIH MH062444-065296 and NIH/NIA 1R01AG029681 grants.

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