

16-Channel Integrated Potentiostat for Distributed Neurochemical Sensing

Roman Genov, *Member, IEEE*, Milutin Stanacevic, *Member, IEEE*, Mihir Naware, Gert Cauwenberghs, *Senior Member, IEEE*, and Nitish V. Thakor, *Fellow, IEEE*

Abstract—We present the architecture and VLSI circuit implementation of a BiCMOS potentiostat bank for monitoring neurotransmitter concentration on a screen-printed carbon electrode array. The potentiostat performs simultaneous acquisition of bidirectional reduction-oxidation currents proportional to neurotransmitter concentration on 16 independent channels at controlled redox potentials. Programmable current gain control yields over 100-dB cross-scale dynamic range with 46-pA input-referred rms noise over 12-kHz bandwidth. The cutoff frequency of a second-order log-domain anti-aliasing filter ranges from 50 Hz to 400 kHz. Track-and-hold current integration is triggered at the sampling rate between dc and 200 kHz. A 2.25-mm × 2.25-mm prototype was fabricated in a 1.2- μ m VLSI technology and dissipates 12.5 mW. Chronoamperometry dopamine concentration measurements results are given. Other types of neurotransmitters can be selected by adjusting the redox potential on the electrodes and the surface properties of the sensor coating.

Index Terms—Analog VLSI, biomedical instrumentation, current-mode circuits, dopamine sensor arrays, log-domain signal processing, neurotransmitters, potentiostat.

I. INTRODUCTION

IMPLANTABLE integrated technologies that enable simultaneous monitoring of chemical neural activity at different locations in the brain could have far reaching impact in understanding the neurophysiology of sensory-motor systems, encoding in auditory nerve and visual cortex among others, and could lead to breakthroughs in areas such as neural prostheses, artificial tissue engineering, and automated neural disorders diagnostics and therapy. A number of integrated potentiostats suitable for on-chip voltammetry or amperometry have been recently reported. Single-channel implementations include [1]–[4]. For distributed electrochemical neural recording, we recently reported an 8-channel integrated potentiostat [5], [6]

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R. Genov is with the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON M5S 3G4, Canada (e-mail: roman@ecg.toronto.edu).

M. Stanacevic is with the Department of Electrical and Computer Engineering, State University of New York at Stony Brook, Stony Brook, NY 11794-2350 USA.

M. Naware and N. V. Thakor are with the Department of Biomedical Engineering, The Johns Hopkins University School of Medicine, Baltimore, MD 21205 USA.

G. Cauwenberghs is with the Division of Biological Sciences, University of California San Diego, La Jolla, CA 92093 USA.

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and a 16-channel integrated potentiostat [7]–[9]. The electrochemical current output from a neurochemical sensor is usually on the order of picoamperes, but can reach the microampere range during transients or catastrophic events such as stroke [10]. The potentiostat in [9] employs oversampling data conversion techniques to achieve the high dynamic range, from picoamperes to milliamperes over nine programmable scales of current, at the cost of reduced sampling rate of less than 30 samples per second for the smallest current scale.

In this work, we present a 16-channel integrated potentiostat microsystem for simultaneous monitoring of chemical neural activity at different locations in the brain at sampling rates ranging from dc to 200 kps while maintaining over 100-dB cross-scale dynamic range. Such sampling rate is important as the spectrum of electrochemical neural activity often remains significant at higher frequencies (i.e., up to 10 kHz). A current-mode BiCMOS design yields high dynamic range in track-and-hold current acquisition [11]. The integrated potentiostat records bidirectional reduction-oxidation (redox) currents at controlled redox potentials from a 16-electrode array of screen-printed carbon-based chemical sensors [12]. The acquired currents are proportional to the concentration of neurotransmitter dopamine near the electrodes. Various types of neurotransmitters can be selected by adjusting the redox potential on the electrodes and the surface properties of the sensor coating [13], [14]. The rest of the paper is organized as follows. Section II presents the architecture of the 16-channel integrated potentiostat. Section III details its VLSI implementation. Section IV contains experimental results of *in vitro* neurotransmitter concentration measurements in real time.

II. ARCHITECTURE

To simultaneously transduce the neurotransmitter activity at multiple locations of brain tissue in close proximity to the neurochemical sensor array, a multichannel potentiostat amplifier has been developed. Each channel of the integrated system simultaneously acquires the oxidation-reduction current generated at the surface of each electrode, amplifies it and converts it to a differential voltage.

The block diagram of one channel of the 16-channel integrated potentiostat is presented in Fig. 1. Each channel is connected to one working electrode with the redox potential, the necessary voltage for driving the redox reactions, set by the voltage V_{red} on its virtual “ground” node. The channels are organized in groups of four with one independent redox voltage per group. An additional reference electrode, common for all working electrodes, is also placed in the bath. Each of the 16 data channels is independently programmed to have a current

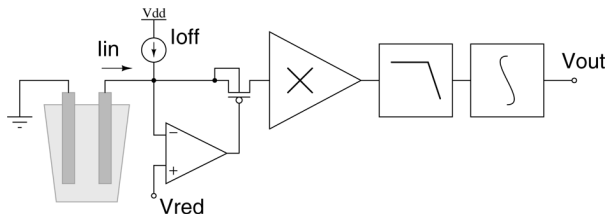


Fig. 1. Simplified block diagram of one channel of the integrated potentiostat.

gain covering four orders of magnitude allowing to acquire bidirectional currents up to $50 \mu\text{A}$, at a redox voltage ranging from 0 to 5 V. An additional bias channel (not shown) supplies all bias and reference signals as well digital control signals. In each data channel, the bidirectional input redox current is summed with an appropriately scaled offset current I_{off} in order to obtain a unidirectional current. The pMOS transistor in the negative feedback of the input transconductance amplifier conveys the current at the supplied redox voltage. The pMOS transistor has the well connected to the source to minimize the back-gate effect, as needed for a 5-V range of the redox voltage.

The acquired input current is subsequently fed into the normalizing circuit. The circuit is programmed to normalize the unidirectional current to a fixed range of $1 \mu\text{A}$. This range is chosen appropriately as a trade-off between signal-to-noise ratio and integration time constant further in the channel. The normalized current is fed into the anti-aliasing low-pass filter. The integrator at the end of the signal path includes a track-and-hold circuit. It provides a differential output voltage buffered in a pipelined fashion.

III. VLSI IMPLEMENTATION

A track-and-hold potentiostat integrated prototype was designed and fabricated in a $1.2\text{-}\mu\text{m}$ double-poly BiCMOS process, which includes a p-Base layer to implement vertical n-p-n bipolars. Vertical n-p-n and lateral p-n-p transistors are used in the design with the goal of improving device matching beyond that attainable with MOS transistors [15]. The chip micrograph is shown in Fig. 2. The sections below focus on particular circuit design solutions and their experimentally measured performance.

A. Transconductance Amplifier

For accurate acquisition of small-amplitude currents, a transconductance amplifier depicted in Fig. 3 is employed in the input current conveyor. It provides a low input impedance virtual node at a user-selectable redox voltage. The amplifier is a wide output range single stage differential amplifier with a pMOS input differential pair and cascoded BiCMOS current mirrors. The differential pair transistors are laid out in a centroid configuration to lower input offset voltage. Higher accuracy current replication is obtained by using current mirrors base current compensation with MOS source followers. The choice of 7-V and -2-V supply voltage rails allows the redox voltage to range from 0 to 5 V (typical values for carbon-based sensors).

The measured input offset voltages are in the range between 5 and 10 mV (for single ended input), for the minimum and maximum input current scales respectively, with the input impedance of 125Ω . From our experience these offset figures

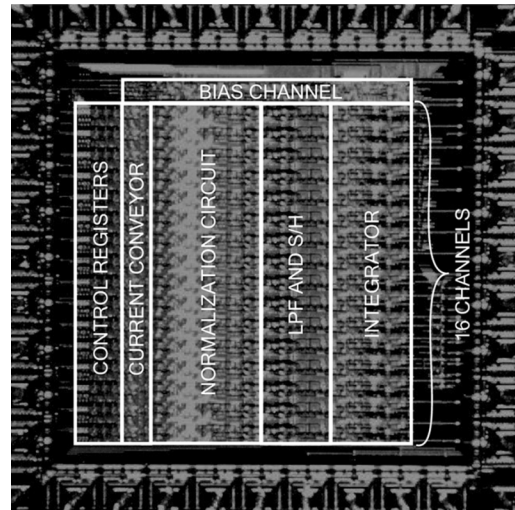


Fig. 2. Chip micrograph of the 16-channel integrated track-and-hold potentiostat. The die size is $2.25 \times 2.25 \text{ mm}^2$ in a $1.2\text{-}\mu\text{m}$ BiCMOS technology.

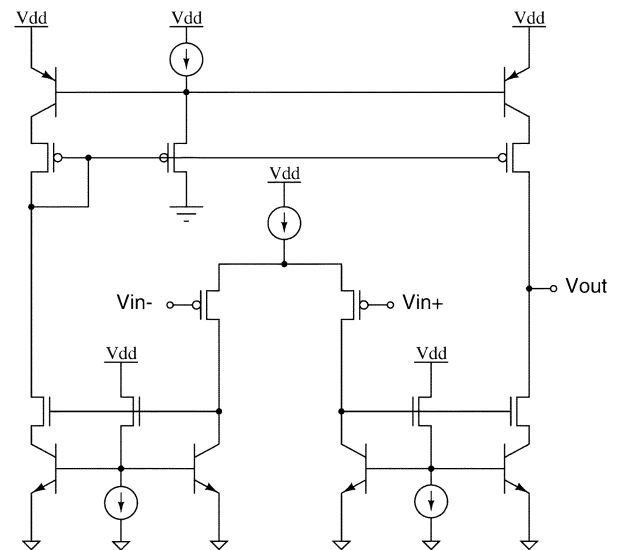


Fig. 3. Input transconductance amplifier with the input differential pair in a centroid layout configuration.

are typical for the technology used, even for a centroid configuration, due to poor control of fabrication process parameters.

B. Current Normalization Circuit

The acquired input current of each data channel is normalized to a fixed range suitable for further processing. Normalization circuitry shown in Fig. 4 performs this task. The programmable scaling selects between four input ranges of current, 100 nA , $1 \mu\text{A}$, $10 \mu\text{A}$, and $100 \mu\text{A}$, independently for every data channel. This scaling function provides for a floating point representation and drastically increased dynamic range. While each channel is designed to provide at least 40-dB dynamic range for any given current range, the cross-scale dynamic range representing the union of the dynamic ranges at all current scales exceeds 100 dB. Channel gains are changed dynamically when an overflow is detected. The value of the input offset current I_{off} is programmed on-chip simultaneously with programming the current gain of a channel. Thus, dynamic re-programming of

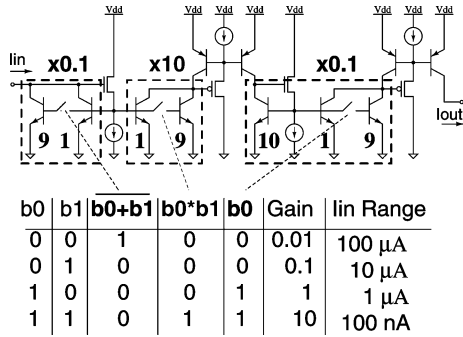


Fig. 4. Current normalization circuitry of a data channel. Normalization is performed over four orders of magnitude of the input current to a fixed output range of 0–1 μ A. The lowest input current scale is 0–100 nA, the highest is 0–100 μ A.

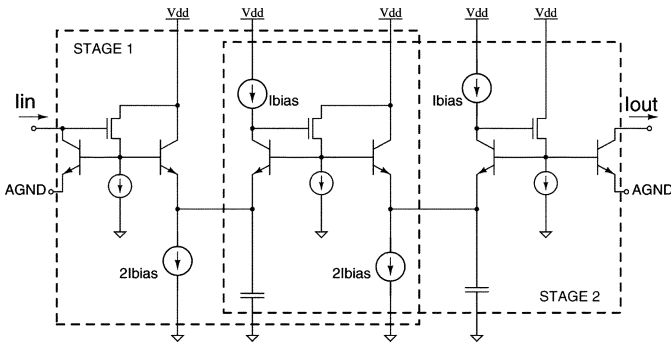


Fig. 5. Anti-aliasing two-stage log-domain LPF.

input current range is possible as no manual tuning of the offset current is required.

The four BiCMOS current mirrors can be configured to attenuate the input signal with a gain of 0.01, 0.1, 1, or 10 by switching bipolar transistors bases controlled by bits b_0 and b_1 . Amplification of currents with gains other than one is performed using n-p-n vertical transistors, as the gain control by scaling of the emitter area is more precise and reproducible. The output current is a replica of the input current normalized to a range 0–1 μ A. Any nonlinear effects in the normalization, and in subsequent processing stages, can easily be accounted for by a look-up table type calibration in software.

C. Anti-Aliasing Filter

To allow aliasing-free sampling of the normalized currents, a second-order low-pass (log-domain) filter (LPF) [16]–[18] with a selectable cutoff frequency shown in Fig. 5 is incorporated into the channel. Each stage constitutes a single pole linear time-invariant (LTI) system with unity dc gain if the bias currents are supplied as shown in Fig. 5. Two single-stage log-domain filters are combined in such a way that the output common-base configuration n-p-n transistors of the first stage serve as the input transistor pair of the second stage. The cutoff frequency set by the current I_{bias} can be programmed in the range from 50 Hz to 400 kHz [17].

The filter prevents aliasing and eliminates high-frequency noise and interference introduced prior to sampling, and additionally allows to bypass the subsequent current-mode sample-and-hold circuit, not shown, before the integration stage, by selecting a time constant sufficiently larger than the integration time interval. Fig. 6 depicts measured channel

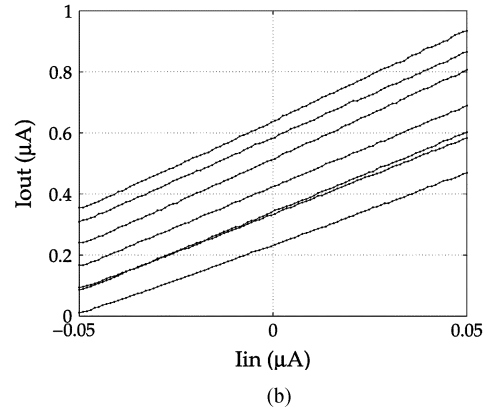
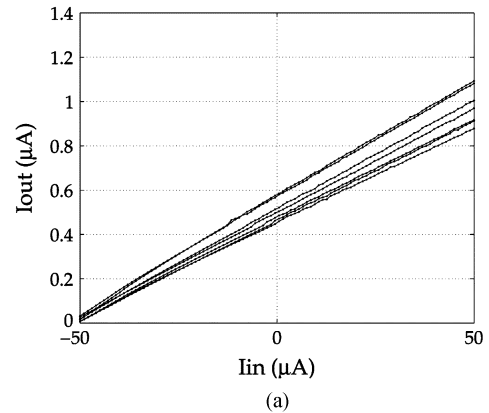


Fig. 6. Measured current transfer characteristics of eight adjacent channels: (a) at the largest (100 μ A) input current scale and (b) at the smallest (100 nA) input current scale.

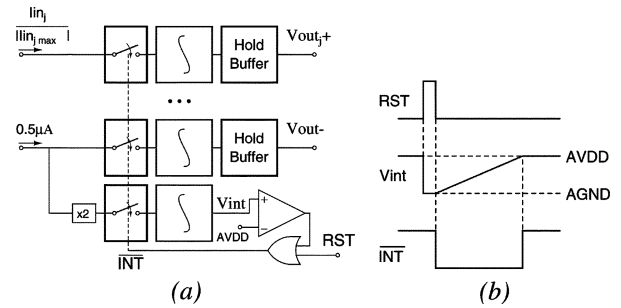


Fig. 7. (a) Integrator and hold buffer multichannel architecture. (b) Timing diagram.

current transfer characteristics for the largest and the smallest current scale for eight adjacent channels. As expected, channel matching improves at larger currents. The observed current spread is attributed to poor control of fabrication process parameters.

D. Integrator and Hold Buffer

Integration circuitry described in this section performs conversion of normalized currents into a differential voltage and produces a continuously available output signal. As depicted in Fig. 7(a), the integration circuit is employed once in each j th data channel, and separately twice in the bias channel.

Integration of the 0.5- μ A dc reference current in the bias channel generates the midpoint voltage, V_{out-} , used as a “zero-level” of the output signal. The differential output format reduces sensitivity to noise and power supply variations. A 16-to-1

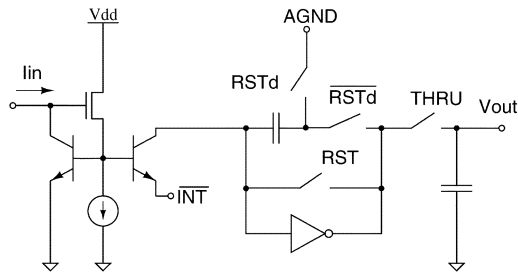


Fig. 8. Switched-capacitor integrator and hold buffer circuit diagram.

multiplexer selects the integrated signal of one of the 16 channels at the output.

Integration of the $1 \mu\text{A}$ dc reference current by the second integrator in the bias channel determines the integration time of all 16 channels. This is achieved by generating the upper-bound voltage, V_{int} , with respect to analog ground AGND and comparing it with the analog supply voltage AVDD. Once the upper-bound voltage reaches AVDD, a control signal $\overline{\text{INT}}$ is set as shown in Fig. 7(b), which completes integration in all channels (including the two bias channel integrators themselves). This corresponds to a $5 \mu\text{s}$ integration time, or 200-kHz maximum sustained sampling frequency.

The circuit diagram of a single integrator is given in Fig. 8. It employs a single-ended nMOS common-source cascoded amplifier. The mirrored input current is integrated on the feedback capacitor of the amplifier. The external digital signal RST is a narrow pulse resetting the integrating capacitor on the rising edge, and also resetting the $\overline{\text{INT}}$ signal on the falling edge. The signal RSTd is a delayed version of RST. The input current is integrated while $\overline{\text{INT}}$ is low.

In order to produce continuously available output voltage, the output voltage is sampled on a capacitor by the digital signal THRU and held while a subsequent current is integrated in a pipelined fashion. Fig. 9(a) depicts measured channel transfer characteristics (integrator output voltage) for eight adjacent channels at the largest current scale. Channel-wise calibration is performed in software in order to remove mismatch-induced offset and gain errors, as well as higher order errors.

The maximum integral non-linearity of -40 dB at the smallest current scale of ± 50 nA was measured as shown in Fig. 9(b). This establishes a 40-dB dynamic range at the smallest current scale and the cross-scale dynamic range of the system at 100 dB. The nonlinearities are calibrated using look-up tables extending the calibrated dynamic range to that limited only by the noise floor. The experimentally measured input-referred current noise of a channel is 46 pA (for a current gain of 10) at a 12-kHz bandwidth. This yields a cross-scale calibrated dynamic range of the system of 120 dB.

The measured characteristics of the integrated track-and-hold potentiostat system are summarized in Table I.

IV. REAL-TIME MEASUREMENT OF NEUROTRANSMITTER CONCENTRATION

The integrated potentiostat has been experimentally demonstrated in real-time measurements of neurotransmitter concentration. The integrated system was interfaced with carbon

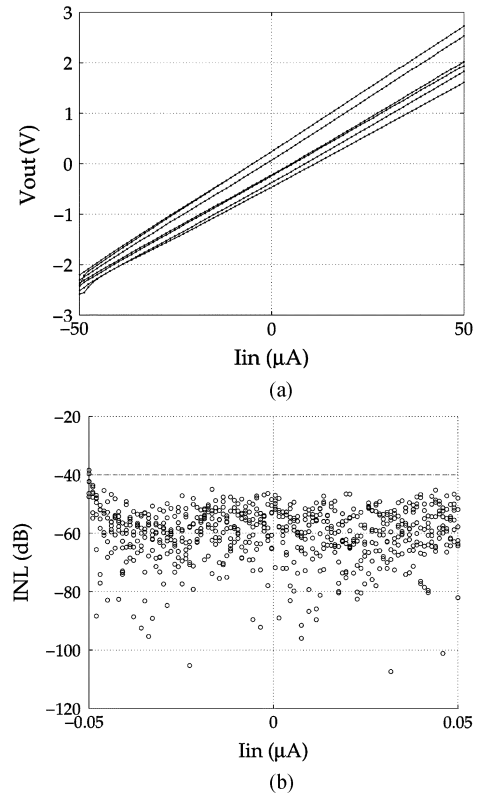


Fig. 9. (a) Measured integrator output voltage for eight adjacent channels at the largest input current scale ($100 \mu\text{A}$). (b) Measured integral nonlinearity of eight adjacent channels at the smallest current scale (100nA).

TABLE I
MEASURED CHIP CHARACTERISTICS

Channels	16			
Max Sampling Rate	200ksps			
Input Current Range	-50nA- +50nA	-500nA- +500nA	-5μA- +5μA	-50μA- 50μA
Input-Referred RMS Current Noise	46pA	1nA	8nA	25nA
Input Impedance	125Ω			
DC Offset	+/-5mV	+/-5mV	+/-5mV	+/-10mV
Power Dissipation	12.5mW			
Analog Volt. Range	0-5V			
LPF Cut-off Freq.	50Hz - 400kHz			
Power Suppl. Volt.	-2V; +7V			
Technology	1.2μm, BiCMOS (vertical NPN)			
Die Size	2.25 mm x 2.25 mm			

micro-fiber electrodes [12] to monitor temporal variations in dopamine concentration in vitro.

A two-electrode system was employed, in contrast with the more traditional three-electrode configuration. This is because the current produced by the oxidation of neurotransmitter species at physiological concentrations is typically in the nano/pico ampere level, and as such, is not expected to affect the reference electrode. Each test was conducted in 25 ml of degassed phosphate-buffered saline (PBS) solution (without

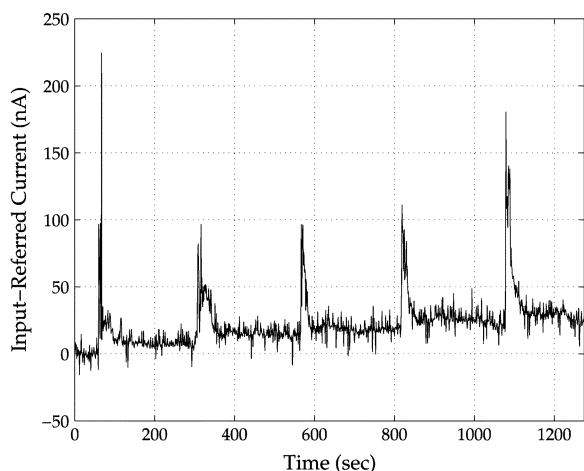


Fig. 10. Measured input-referred chronoamperometry sensors output current.

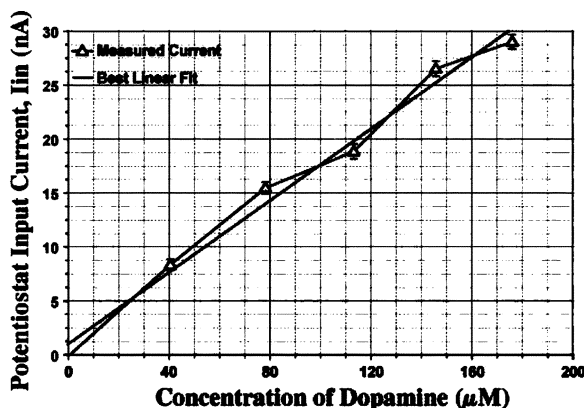


Fig. 11. Sensor calibration plot: time-averaged carbon electrode output current as a function of the concentration of the analyte dopamine in a solution. The best linear fit is also shown.

Mg⁺⁺ or Ca⁺⁺) at a pH of 7.4. Standard chronoamperometry was employed to measure the current, in which the working carbon electrode was held at 900 mV with respect to the Ag/AgCl reference electrode. The current was recorded as a function of time as shown in Fig. 10. Controlled amounts of dopamine solution were introduced into degassed phosphate-buffered saline solution every four minutes and briefly stirred. The current spikes correspond to recordings during the manual stirring and are thus not relevant. The pedestals correspond to the steady state concentration measurements and are monotonically increasing, consistent with the amounts of dopamine added. The calibration curve of the sensor-chip system depicted in Fig. 11 was obtained by calculating average currents for discrete concentration levels.

V. CONCLUSION

A 16-channel integrated potentiostat for simultaneous parallel recording of neurochemical activity has been interfaced with a 16-electrode array of carbon-coated neurotransmitter sensor. The microsystem has been tested to operate with an input cross-scale dynamic range of over 100 dB and allows to resolve bidirectional redox currents with input-referred rms noise of 46 pA. The system features programmable current gain

control, configurable anti-aliasing circuitry, triggered current integration and provides differential voltage-mode output ready for asynchronous external analog-to-digital conversion over a compressed dynamic range. The neurochemical interface has been demonstrated in real-time *in vitro* measurements of dopamine concentration.

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Roman Genov (S'96–M'02) received the Ph.D. degree from The Johns Hopkins University, Baltimore, MD in 2003.

He is presently an Assistant Professor in the Department of Electrical and Computer Engineering, University of Toronto, Toronto, ON, Canada. His research interests include analog and digital VLSI circuits, systems and algorithms for energy-efficient signal processing with applications to electrical, chemical and photonic sensory information acquisition, biosensor arrays, neural interfaces, parallel

signal processing, adaptive computing for pattern recognition, and implantable and wearable biomedical electronics.



Milutin Stanačević (S'00–M'05) received the B.S. degree in electrical engineering from the University of Belgrade, Belgrade, Serbia, in 1999, and the Ph.D. degree in electrical and computer engineering from The Johns Hopkins University, Baltimore, MD, in 2005.

He is currently an Assistant Professor of Electrical and Computer Engineering at Stony Brook University, Stony Brook, NY. His research interests include mixed-signal VLSI circuits, systems, and algorithms for parallel multichannel sensory information processing with emphasis on real-time acoustic source localization and separation, and micropower implantable biomedical instrumentation and telemetry.



Mihir Naware was born in Mysore, India, in 1979. He received the B.Tech. degree in instrumentation engineering from the Indian Institute of Technology (IIT), Kharagpur, India, and the M.S. degree in biomedical engineering from The Johns Hopkins University, Baltimore in 2001 and 2003, respectively.

In 2004, he joined St. Jude Medical, CRMD, Sunnyvale CA, as a Hardware Design Engineer. His interests include biomedical sensors, and associated development of hardware and algorithms, specifically for implantable medical devices. For his M.S. thesis,

he worked on microfabricated sensors for neurotransmitters, primarily based on different forms of carbon as an electrode.



Gert Cauwenberghs (S'89–M'94–SM'04) received the Ph.D. degree in electrical engineering from California Institute of Technology, Pasadena, in 1994.

Previously Professor of Electrical and Computer Engineering at The Johns Hopkins University, Baltimore MD, he joined University of California San Diego, La Jolla, as Professor of Neurobiology in 2005. His research aims at advancing silicon adaptive microsystems to understanding of biological neural systems, and to development of sensory and neural prostheses and brain-machine interfaces.

Dr. Cauwenberghs received the National Science Foundation Career Award in 1997, the Office of Naval Research Young Investigator Award in 1999, and Presidential Early Career Award for Scientists and Engineers in 2000. He is Associate Editor of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS I—REGULAR PAPERS, the IEEE TRANSACTIONS ON NEURAL SYSTEMS AND REHABILITATION ENGINEERING, and the IEEE SENSORS JOURNAL.



Nitish V. Thakor (S'78–M'81–SM'89–F'97) received B.Tech. degree in electrical engineering from Indian Institute of Technology (IIT), Bombay, India, in 1974 and the Ph.D. degree in electrical and computer engineering from the University of Wisconsin, Madison, in 1981.

He served on the faculty of Electrical Engineering and Computer Science of the Northwestern University between 1981 and 1983, and since then he has been with the School of Medicine, The Johns Hopkins University, Baltimore, MD, where he is currently serving as a Professor of Biomedical Engineering. He conducts research on neurological instrumentation, biomedical signal processing, micro and nanotechnologies, neural prosthesis, and clinical applications of neural and rehabilitation technologies. He has authored more than 160 peer-reviewed publications on these subjects. Currently he directs the Laboratory for Neuroengineering and is also the Director of the National Institute of Health (NIH) Training Grant on Neuroengineering. One of his current research projects, in collaboration with a multi-University consortium, funded by the Defense Advanced Research Projects Agency (DARPA), is to develop a next generation neurally controlled upper limb prosthesis. He is actively interested in developing international scientific programs, collaborative exchanges, tutorials and conferences on Neuroengineering and Medical Microsystems.

Dr. Thakor is the Editor-in-Chief of IEEE TRANSACTIONS ON NEURAL AND REHABILITATION ENGINEERING. He is a recipient of a Research Career Development Award from the National Institutes of Health and a Presidential Young Investigator Award from the National Science Foundation. He is a Fellow of the American Institute of Medical and Biological Engineering, IEEE and Founding Fellow of the Biomedical Engineering Society. He is also a recipient of the Centennial Medal from the University of Wisconsin School of Engineering, Honorary Membership from Alpha Eta Mu Beta Biomedical Engineering student Honor Society and Distinguished Service Award from IIT Bombay.