VLSI POTENTIOSTAT ARRAY FOR DISTRIBUTED ELECTROCHEMICAL NEURAL RECORDING

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ABSTRACT

A neurochemical sensor system is being developed to spatially sense and process neurotransmitters. This paper reports the design and VLSI implementation of a multi-channel potentiostat that interfaces to a nitric-oxide (NO) sensor array. Picoampere to microampere input currents are range-normalized with programmable gain, and digitized by a bank of current-mode delta-sigma analog-to-digital (A/D) converters. First-order noise shaping and 4,096-fold oversampling provide high signal-to-noise ratio for the low-frequency NO transients. A shift register scans the buffered decimated delta-sigma outputs in bit-serial format providing asynchronous sequential readout. An 8-channel potentiostat in 0.5 μm CMOS measures 1.5mm $\times$ 1.5mm, and consumes 0.5 mW power. The device is expected to serve as a valuable tool for neurophysiological research and implantable neural prostheses.

1. INTRODUCTION

Electrophysiology of populations of neurons has so far relied primarily on electrical sensing. Neurochemical sensing will enable real-time, continuous monitoring of neurotransmitter activity accompanying both electrophysiological processes and the response of the nervous system to neural stimulation and prosthesis. The basic aim of this project is to design a fully programmable multi-channel potentiostat chip to interface with a multi-electrode array. Previously, George reported the fabrication process for the interfacing sensor array [1], illustrated in Figure 1. The sensor system will be used to measure the concentration of nitric-oxide (NO), a diffusible neurotransmitter. Electrodes are coated with polymers to make them selective to NO. Each potentiostat channel employs one working electrode, maintained at virtual ground, with a redox potential, $-E_{red}$, applied to the reference electrode. Thus the working electrode is biased at E_{red} with respect to the reference electrode [3]. The redox potential required for NO is 900 mV. NO is metabolized by oxygen and blood and has a half life of about 5 seconds. The electrochemical current output from the electrode is usually on the order of picoamperes, but can reach the microampere range during transients or catastrophic events such as stroke [2].

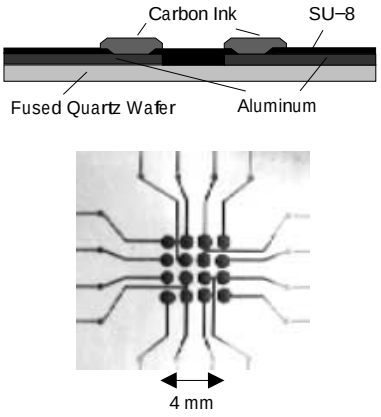

Fig. 1. *Nitric-oxide (NO) sensor array for electrochemical neural recording (George et al. [1]). Top: cross section using carbon screen printing fabrication process. Bottom: 4 $\times$ 4 array.*

Turner et al. [4] previously reported a basic CMOS integrated potentiostat capable of measuring currents from 0.1 to 3.5 μA, with a nonlinearity of 2%, and total power consumption less than 2 mW. Additionally, Kakerow et al. [5] reported on the development of a monolithic potentiostat capable of making 2-3 current measurements in the range of 0.1 nanoamperes to 0.5 microamperes.

The primary difference between the strategy adopted in our design and those of the aforementioned designs is that the analog path of the chip operates entirely in the current domain. Current-mode signal processing, as compared to conventional voltage-mode techniques, seemed a natural choice for a potentiostat as the input is a current over several orders of magnitude. Current mode techniques intrinsically offer large dynamic range, spanning 6 orders of magnitude in the subthreshold region [6, 7], and avoid the need for highly linear current-to-voltage conversion.

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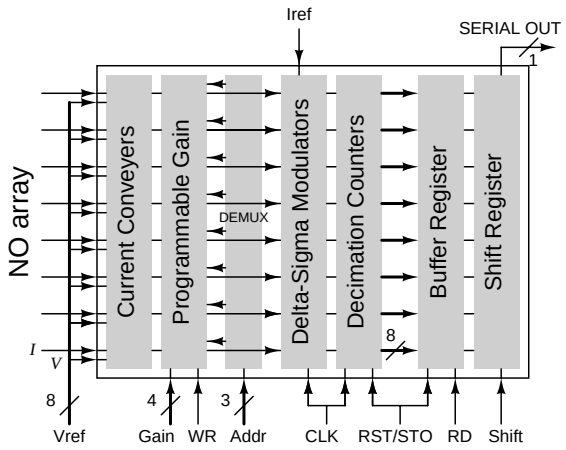

Fig. 2. *Potentiostat chip architecture.*

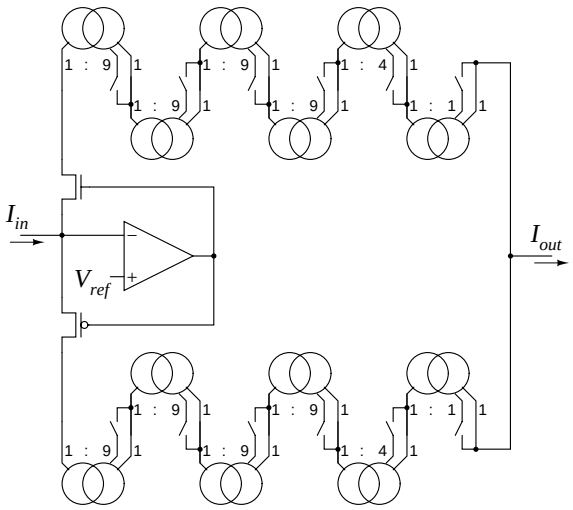

Fig. 3. *Simplified schematic of input stage: current conveyer and programmable gain amplifier.*

2. ARCHITECTURE

Each potentiostat channel consists of a current amplification stage, with input current conveyor and programmable gain current mirrors, and a current-mode delta-sigma A/D converter, with counting decimator. A register buffer and shift register provide an asynchronous bit-serial output. The system diagram is shown in Figure 2.

Input current in each channel is amplified to the microampere range and passed to a delta-sigma A/D converter to digitize the signal. The oversampled binary output of the delta-sigma modulator is decimated using a binary counter. The decimated signals for all channels are then scanned by an output shift register, and the sequence is fed off-chip through an asynchronous bit-serial interface for external processing.

A 1MHz clock CLK serves as the system clock for the delta-sigma modulators and decimation counters. One sample of conversion takes 4,096 cycles of the system clock, for 12-bit resolution at 250 Hz conversion rate. Upon completion of the conversion cycle, all 8 channels' 12 bits are stored in a buffer register, and the counters are reset for the next conversion cycle. Resolution can be traded for bandwidth by adapting the conversion cycle length, through control of the buffer store and counter reset (RST/STO) signal.

Pipelined operation allows a new conversion to start while previous outputs are read off-chip. Furthermore, the buffer register allows for asynchronous read-out, using a different clock (Shift) to scan out the digital outputs in sequential, bit-serial fashion. The scanning is initiated by the RD clock signal, which loads the content of the buffer into the output shift register. This allows to read data at a different rate than set by the delta-sigma clock and oversampling ratio.

3. VLSI IMPLEMENTATION

The chip operates in the subthreshold region to provide high sensitivity matching the wide range of input currents, and decrease power consumption. The different stages are described below.

3.1. Current-mode input stage and amplifier

Input currents from the NO array are usually on the order of picoamperes, but can reach several decades larger [2]. A current conveyor and two cascades of current mirrors, shown in Figure 3, acquire and amplify the signal to the microampere range.

The active current conveyor [8] establishes a virtual ground at the input node while acquiring the current for proper potentiostat operation. A (standard) single-stage cascoded differential voltage amplifier is used to provide high gain for low voltage offset at the input. Remaining offset resulting from component mismatch in the differential amplifier can be calibrated for accurate control of the reference voltage V_{ref} (redox potential E_{red}) of the potentiostat.

A pair of nMOS and pMOS transistors in the feedback path of the amplifier conveys the current in two branches, each exclusively serving one polarity of the input. The current is amplified separately in either branch, containing a cascade of current mirrors with programmable gain. Gain mismatch between polarities is not an issue as the polarity is easily detected for sign-based gain correction after decimation.

Current mirrors in the cascade alternate source and sink types, as shown schematically in Figure 3. A low-voltage, subthreshold cascode configuration [9] is used for the al-

ternating nMOS and pMOS current mirrors, improving dynamic range and lowering power consumption.

Programmable gain is implemented in 6 mirroring amplification stages. Each stage has one of two amplification values, selected by the state of a control bit through a current switch. Unity gain is established when the switch is open. A second mirroring path is selected when the switch is closed, contributing additional gain given by the mirror ratio of the second path. The first four stages each provide one decade of amplification, and the remaining stages offer fine tuning with selectable gains 5 and 2. A total of 16 different gain values over 5 decades (1-10^5) are thus available.

Each channel gain is individually programmable, using a 4-bit register and a decoder. Programming for a particular channel is achieved with the demultiplexer (DEMUX) in Figure 2 by selecting the channel address (Addr) and asserting a write signal (WR) while the 4-bit gain setting (Gain) is valid. All gain values are statically latched in their registers.

The outputs of the two cascaded mirroring branches are joined, and subsequently digitized.

3.2. Delta-sigma A/D converter

Neurotransmitter activity operates at low frequency, with time constants ranging from milliseconds to seconds. Interference from other sources in the currents acquired from the NO sensor make the received signal susceptible to high-frequency noise. Oversampling analog-to-digital (A/D) conversion allows to eliminate some of this noise, along with the shaped quantization noise, in the digital domain. This alleviates the need for accurate low-pass filtering in the input stage. With very large ($> 1,000$) oversampling, first-order noise shaping is adequate for high signal-to-noise ratio. A first-order architecture also supports simple VLSI implementation of the modulator and decimator.

The A/D converter employs a first-order delta-sigma modulator, comprised of a continuous-time integrator, a voltage comparator, and a switched reference current in the feedback loop, shown in Figure 4. The decimator is implemented using a binary counter, avoiding problems with spurious tones that arise under certain steady inputs when using sharper cut-off decimation filters [10].

The continuous-time current integrator is implemented with a capacitor placed between the output and inverting input terminals of a differential transconductance amplifier. The cascoded single-stage transconductance amplifier operates nominally in the subthreshold region. A mid-range fixed voltage (shown as signal ground in Figure 4) is placed at the non-inverting terminal of the opamp, and the reference to the comparator. The output of the comparator is passed through a static shift register, controlled by a non-overlapping clock (ϕ_1, ϕ_2) derived from the system clock CLK. The digital output Q is valid at each rising edge of CLK.

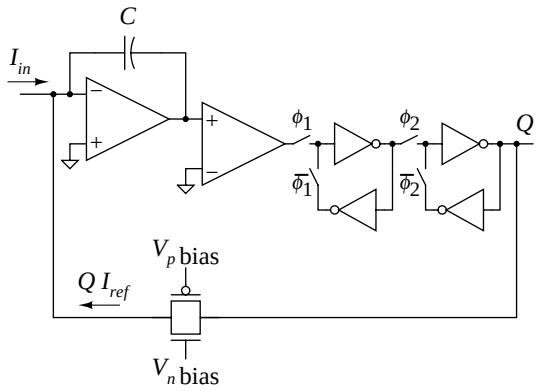

Fig. 4. *Simplified schematic of current-mode delta-sigma A/D converter.*

Current feedback from the quantized output in the delta-sigma loop is achieved using a pair of nMOS and pMOS transistors. Bias voltages $V_{n\ \mathrm{bias}}$ and $V_{p\ \mathrm{bias}}$ are established from an externally supplied reference current I_{ref} to provide switched currents $\pm I_{ref}$, controlled by the state of the delta-sigma output Q. By switching these transistors from the source rather than gate terminals, and retaining constant bias voltages on the gates, clock feedthrough switch injection noise is minimized [11].

3.3. Decimator and asynchronous bit-serial output

The decimator implements a rectangular FIR window for the low-pass digital filter, of the accumulate-and-dump type. This stage consists of a series of counters and registers. The circuit counts the number of digital ones returned by the delta-sigma modulator during a time span of 4,096 clock cycles.

The counter is constructed of a series of dynamic registers cascaded in a ripple-counter configuration. Upon reset (RST), the output of each of the 12-bit registers is set to 0. The delta-sigma output is gated with the system clock CLK as clock input to the counter.

After 4,096 clock cycles, data is stored (STO) onto eight adjacent buffer registers. Data is loaded in the output shift-register with the RD clock, independent of STO. The 12 bits of each channel are then shifted bit-serially to the output pin, over 96 cycles of the Shift clock, independent of CLK. The pipelining allows a new A/D conversion cycle to start as soon as bits are stored in the buffer register.

4. RESULTS AND DISCUSSION

The chip was fabricated in 0.5 μm technology, with an active area of 1.1mm $\times$ 1.1mm. Power consumption is 0.5 mW at 5 V supply. Figure 5 shows the micrograph of the fabricated chip.

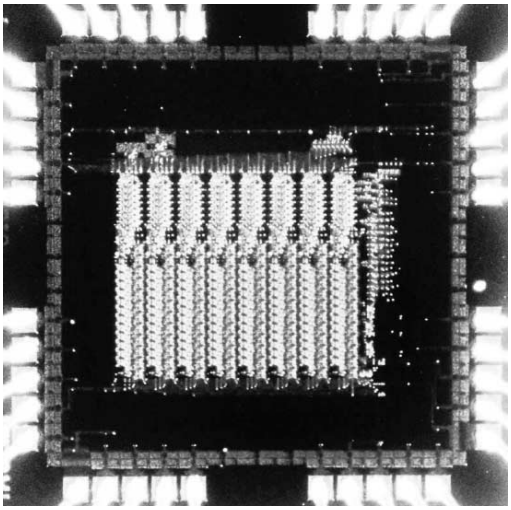

Fig. 5. *Micrograph of 8-channel potentiostat chip. Dimensions are 1.5mm × 1.5mm in 0.5 μm CMOS technology.*

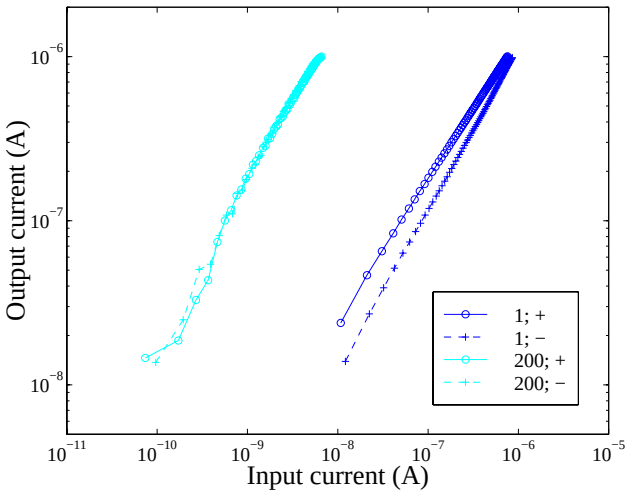

Fig. 6. *Current amplification in the input stage of one channel of the potentiostat chip, measured for two settings of the digitally programmable gain (1; 200) and both polarities (+; −) of the input current.*

The chip was tested and characterized for different current inputs, simulating the actual current levels expected from microelectrode recordings. For verification purposes, multiple test points have been made accessible in the chip design. Tests have been conducted for different amplification settings in the input stage, and oversampling ratios in the digitization stage. Measured data for the input amplification stage are shown in Figure 6. Gain mismatch for different amplification settings and both polarities of the input can easily be accounted for by calibration. Similarly, mismatch in the delta-sigma reference current contributes a channel-dependent gain, uniform across scales and polarities of the input, that can be digitally corrected.

The integrated NO sensor array and VLSI interface constitute a complete system for in vitro neurochemical measurements. An integrated sensor plus potentiostat opens up new uses in measuring electrochemical reactions from a variety of neurotransmitters, including NO and dopamine. The sensitivity of pA to μA level currents in a potentiostat array make it possible to differentiate currents from single membrane channels and monitor neurotransmitter activity at the synaptic level. In the long term we envisage applications of the device integrated in implantable neural prostheses.

5. REFERENCES

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