520.492 Mixed-Signal VLSI Systems

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Week 1

VLSI Technology and Device Characterization

References

1. Geiger, Allen and Strader: pp 33-235.
2. Tsividis, *Operation and Modeling of the MOS Transistor*.
3. Sze, *VLSI Technology*.
4. Beynon & Lamb, “Charge Coupled Devices”, in *Topics in Applied Physics* vol. 38.

SILICON VLSI TECHNOLOGY

INGREDIENTS

- Silicon
- Polysilicon (POLY)
- Oxide (SiO_2)
- Impurities (diffusion, implants)
- Metal (Al, Au)

DEVICES

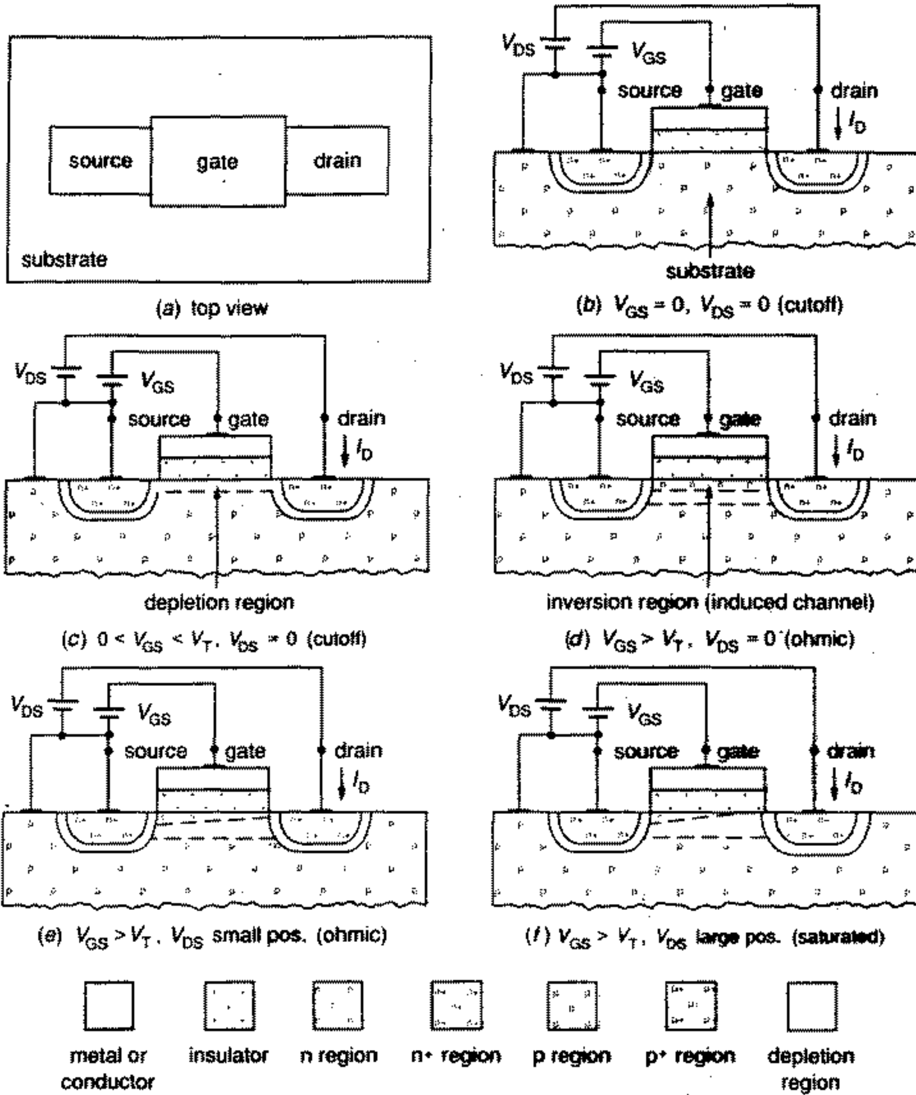
- MOSFETS (nMOS, pMOS)
- JFETS
- bipolars (npn, pnp)
- diodes
- capacitors
- resistors
  - + derivates: phototransistors, floating gates, CCD's, ...

LAYERS (typical MOSIS)

- diffusion (n and p; masked with "Select")
- well
- poly (poly 1, poly 2)
- metal (metal 1, metal 2, ...)
- p-base (npn vertical BJT in n-well process)
- buried channel
- + contacts; via(s)

MOS TRANSISTORS

(Geiger & al.: pp 32-236)



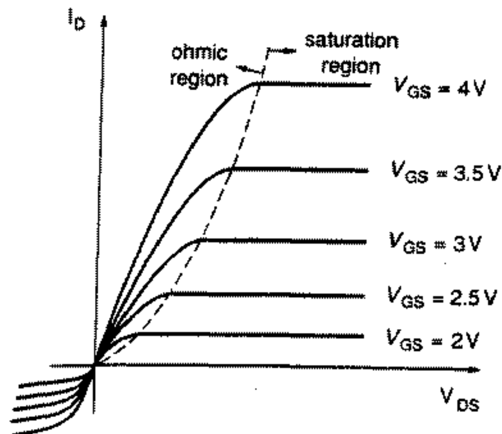


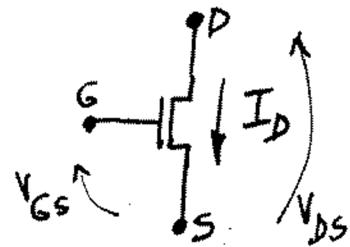
FIGURE 2.2-3
Typical output characteristics for an n-channel MOSFET.

MOS MODELS

Above threshold: (Shichman - Hodges)

$$I_D = \begin{cases} 0 & \text{CUTOFF} \\ \frac{1}{2} K' \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS}) & \text{SATURATION} \\ K' \frac{W}{L} \left(V_{GS} - V_T - \frac{V_{DS}}{2}\right) V_{DS} (1 + \lambda V_{DS}) & \text{OHMIC (TRIODE)} \end{cases}$$

$$V_T = V_{T0} + \gamma \left(\sqrt{\phi - V_{BS}} - \sqrt{\phi} \right)$$

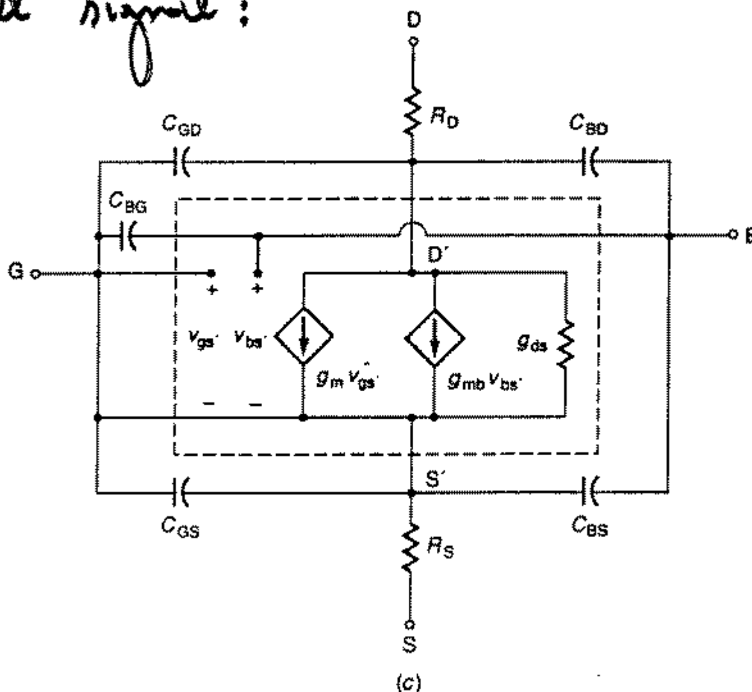


Below threshold:

$$I_D = I_0' \frac{W}{L} e^{\frac{\kappa V_{GB} - V_{SB}}{V_{th}}} \left(1 - e^{-\frac{V_{DS}}{V_{th}}}\right)(1 + \lambda V_{DS})$$

V_{th} = thermal voltage, $\frac{kT}{q}$ ($\approx$ 25mV)
κ = back gate effect

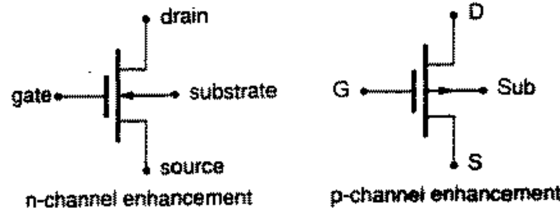
AC, small signal:



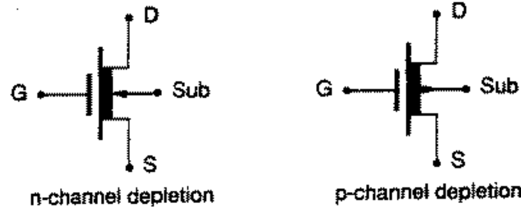
(c)

FIGURE 3.1-19

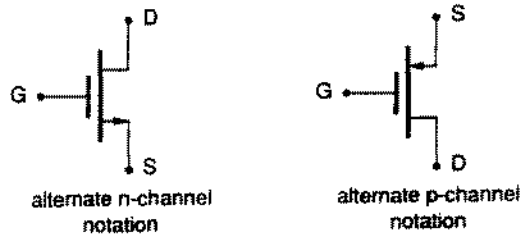
MOS symbols:



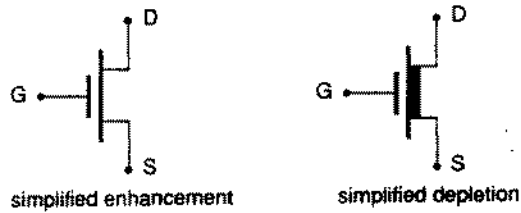
n-channel enhancement p-channel enhancement



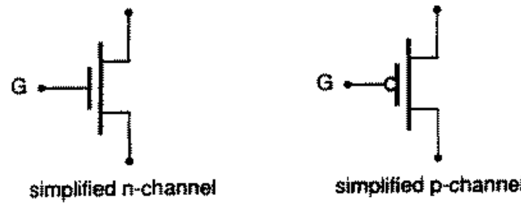
n-channel depletion p-channel depletion



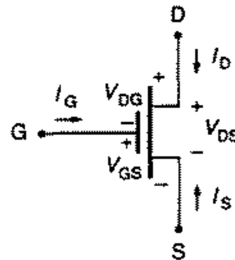
alternate n-channel notation alternate p-channel notation



simplified enhancement simplified depletion



simplified n-channel simplified p-channel

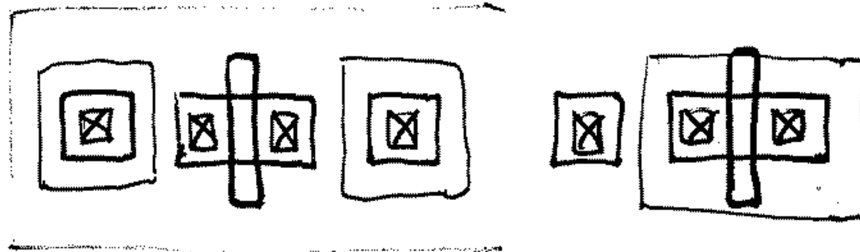


electric variable convention (n- or p-channel, enhancement or depletion)

FIGURE 2.2-4
Symbols for MOS transistors.

PHYSICAL LAYOUT / PARASITICS:

CIF:



Cross section:

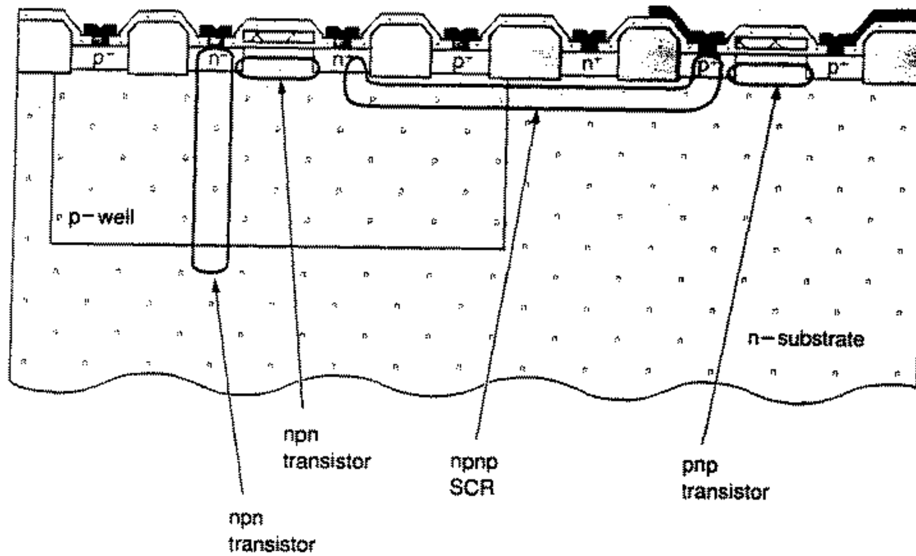
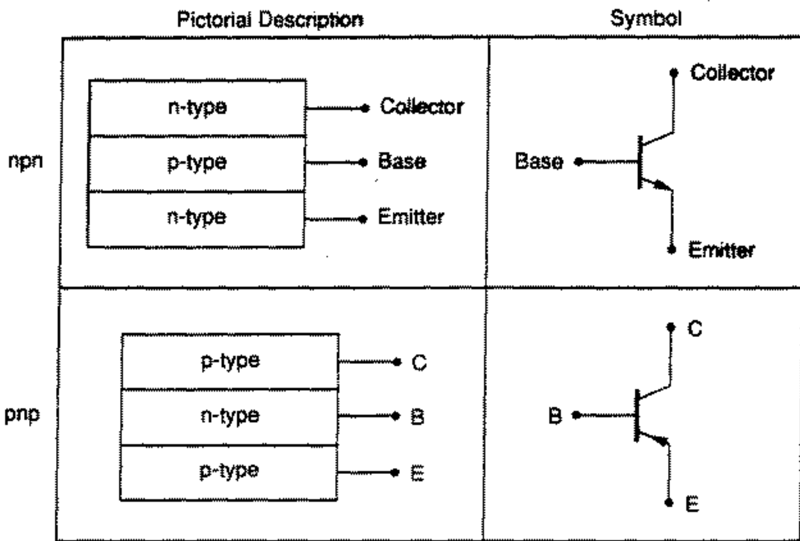


FIGURE 2.2-7
Parasitic transistors in a p-well CMOS process.

BIPOLAR JUNCTION TRANSISTORS (BJT's)



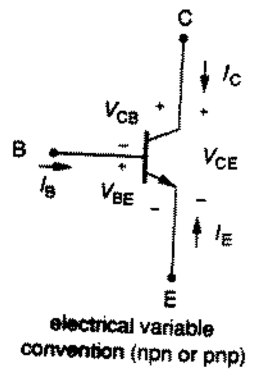


FIGURE 2.2-8
Bipolar transistors.

DC:

$$I_C = J_s A\, e^{V_{BE}/V_t} \left(1 + V_{CE}/V_{AF}\right)$$

$$I_B = \frac{1}{\beta_F} J_s A\, e^{V_{BE}/V_t}$$

AC:

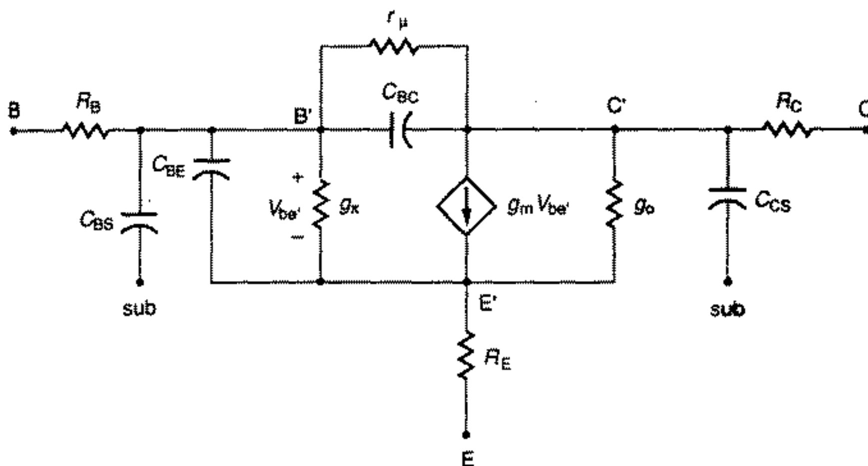


FIGURE 3.3-12
High-frequency small signal equivalent circuit of BJT.

PHYSICAL LAYOUT / FABRICATION STRUCTURE

Bipolar process (w/ epi layers)

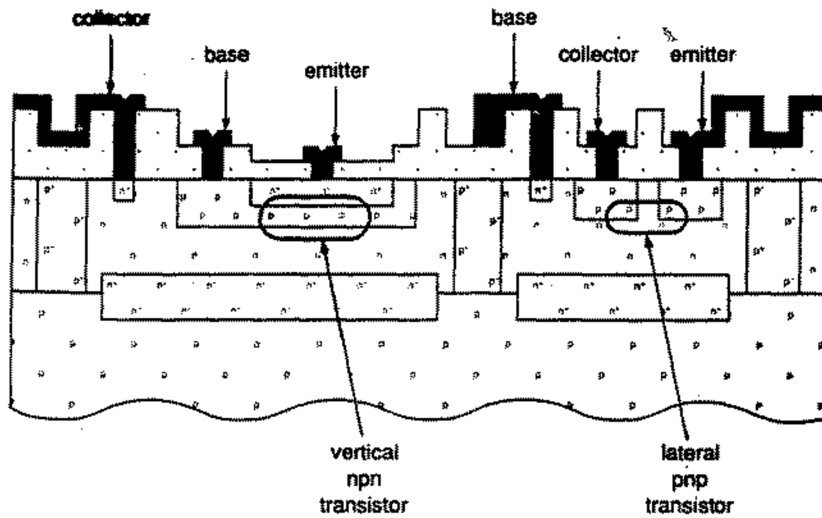
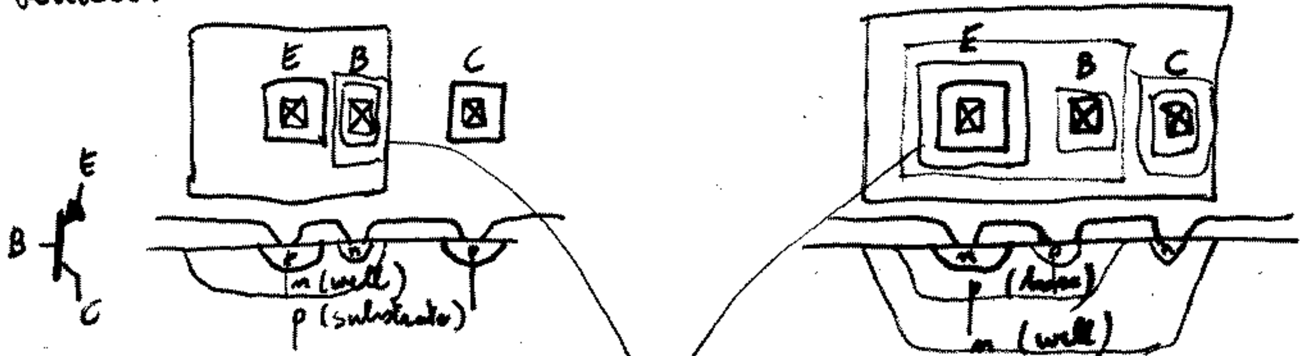


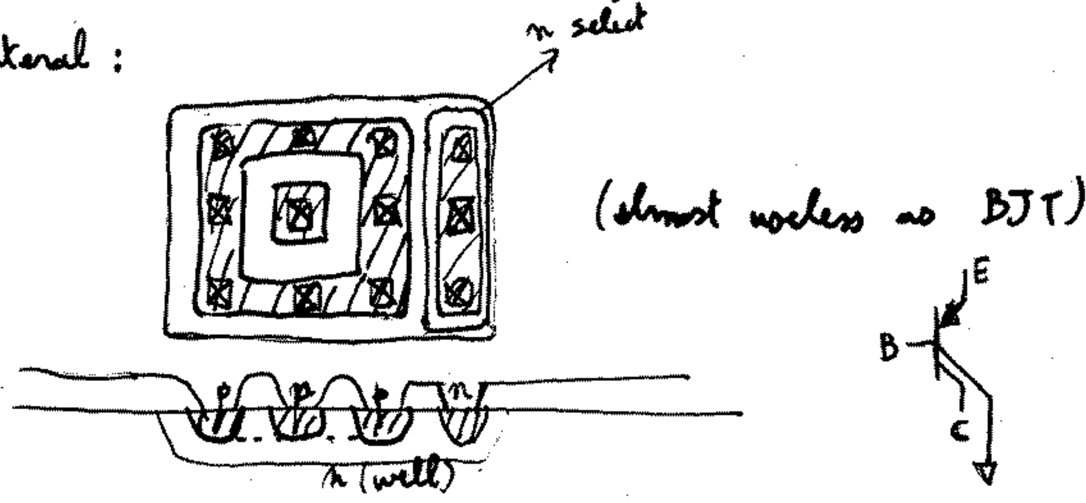
FIGURE 2.2-9
Vertical and lateral transistors in a bipolar process.

Through MOSIS (BiCMOS):

- vertical:



- lateral:



(almost useless as BJT)

B E C

NOTE: SCR (thyristor; npnp or pnpn)

$I \downarrow$, V

E_1, B_1, C_1 — p, n, p, n — C_2, B_2, E_2

$I = I_{E_1}$, V_1, I_{B_1}, V_{p_2}, β_1, I_{C_2}, C_{p_2}, I_{C_1}, V_{p_1}, C_{p_1}, I_{B_2}, β_2, $I = I_{E_2}$, V_2

$(V = V_1 - V_2)$

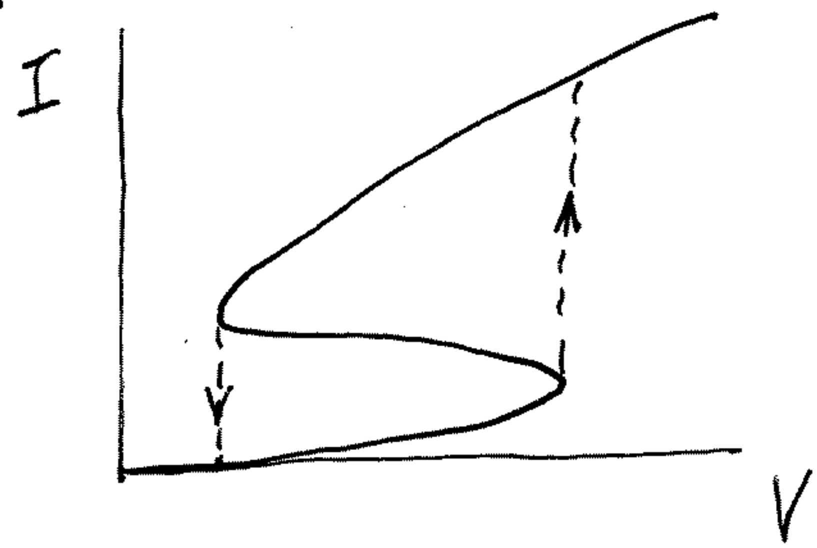
$$I_{C_1} = \beta_1 I_{B_1} = \beta_1 \left(I_{C_2} + C_{p_2} \frac{d}{dt} V_{p_2} \right)$$

$$\Rightarrow$$

$$I_{C_2} = \beta_2 I_{B_2} = \beta_2 \left(I_{C_1} - C_{p_1} \frac{d}{dt} V_{p_1} \right)$$

$$\beta_1 \beta_2 \gg 1 \Rightarrow I_{C|B,\,1|2} \rightarrow \infty \text{ or } 0$$

BISTABLE

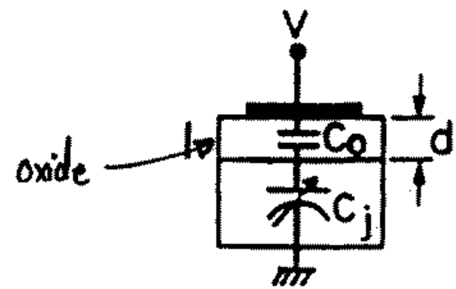


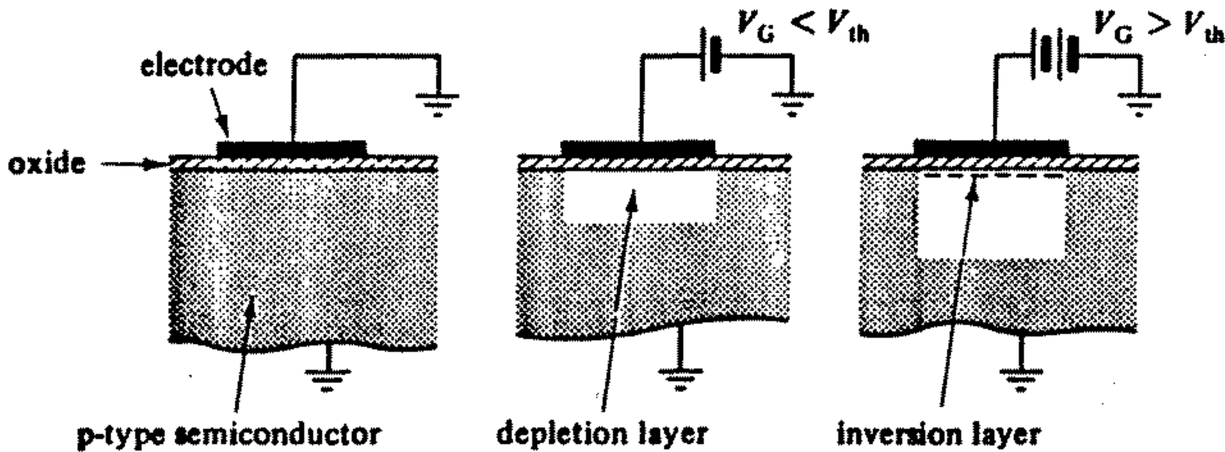
COMPARISON

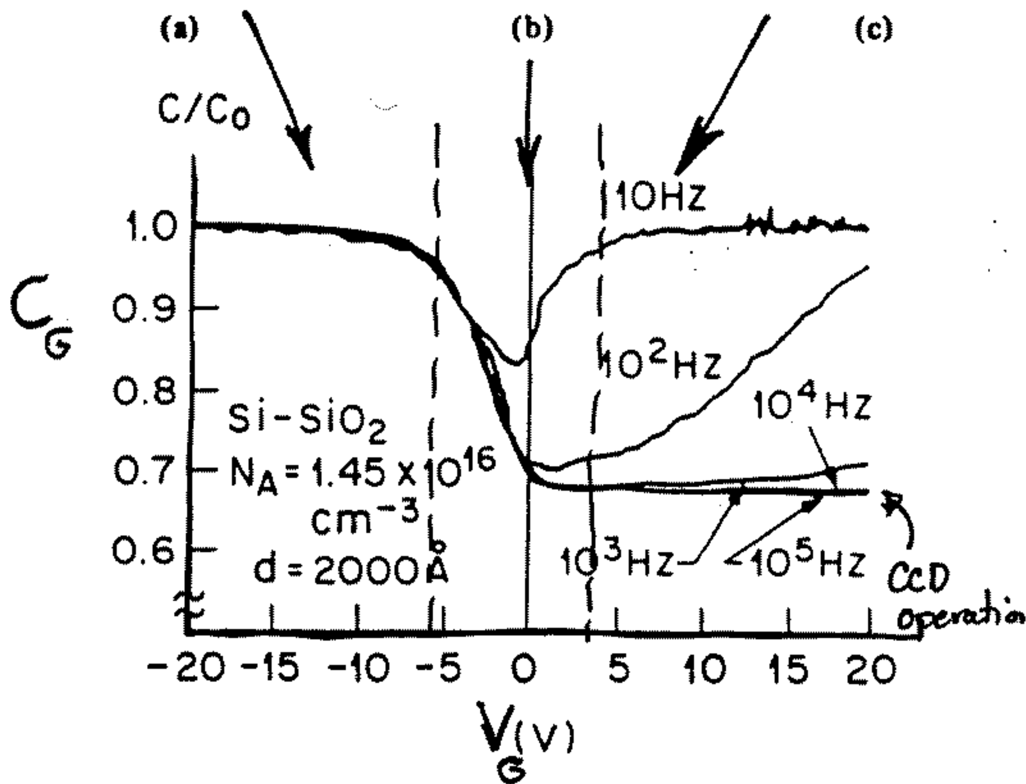
MOS	Bipolar
voltage-driven current source	current-driven current source
$Z_{in} = \infty$	Z_{in} = small
Z_{out} = large	Z_{out} = large
ohmic insulation	low-noise
compact	precise matching
thermally stable	fast
logic / memory (no static power)	high speed interfacing (ECL, ...)
switched capacitors	linear analog

↘ BiCMOS VLSI ↙

THE MOS CAPACITOR

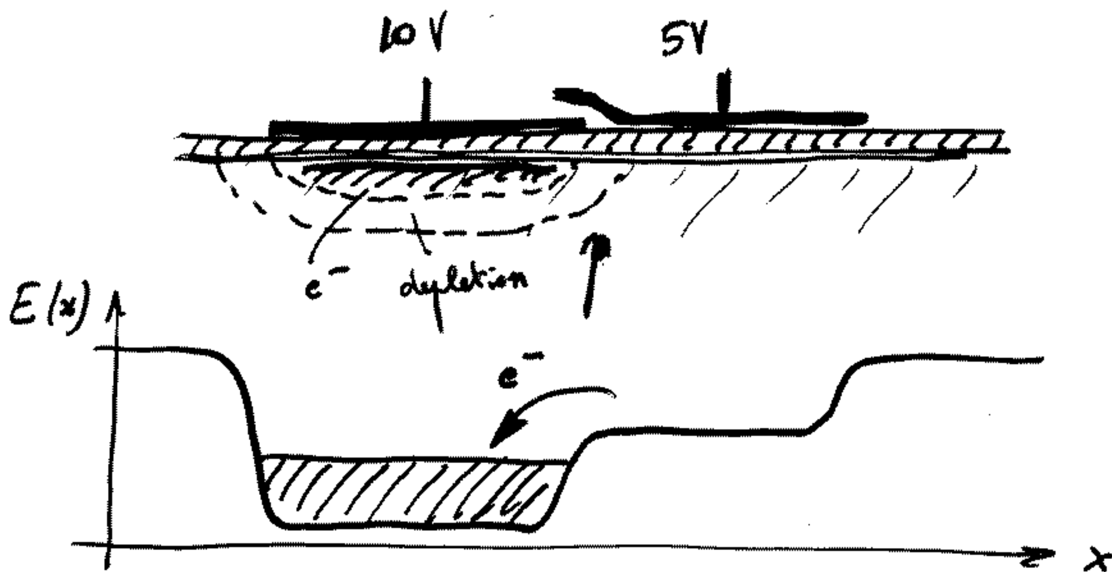


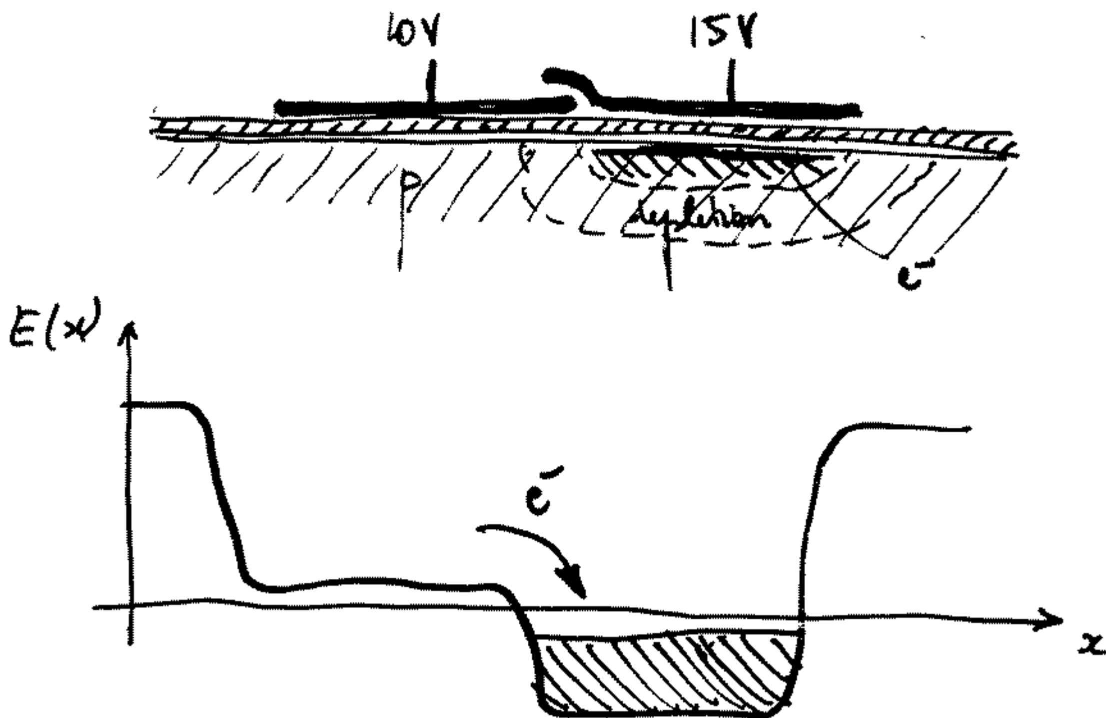




Slow recovery of inversion channel, unless there are drain or source diffusions in contact with the channel to provide carriers fast.

CCD's (and CID's)





Basic CCD Shift Register Operation

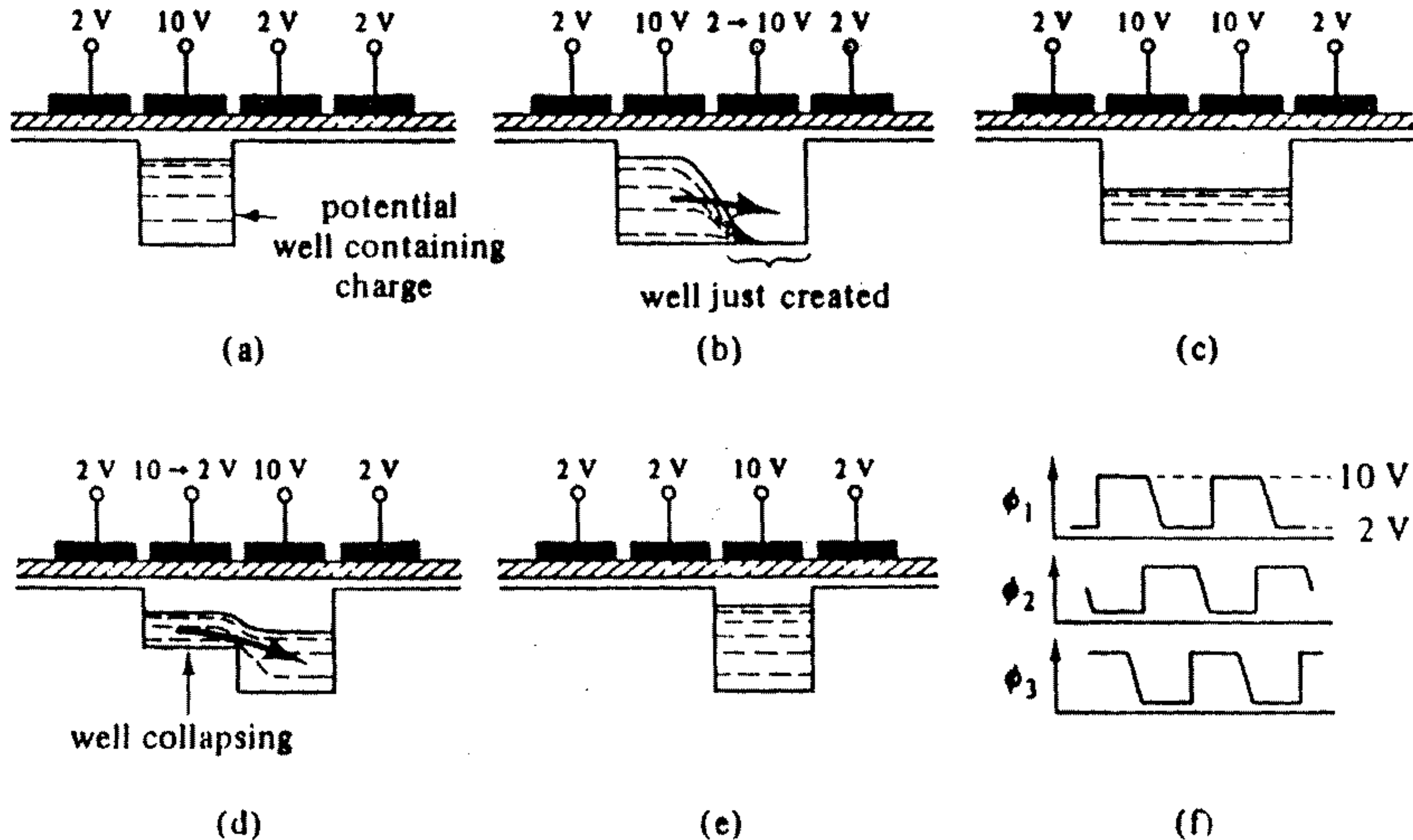
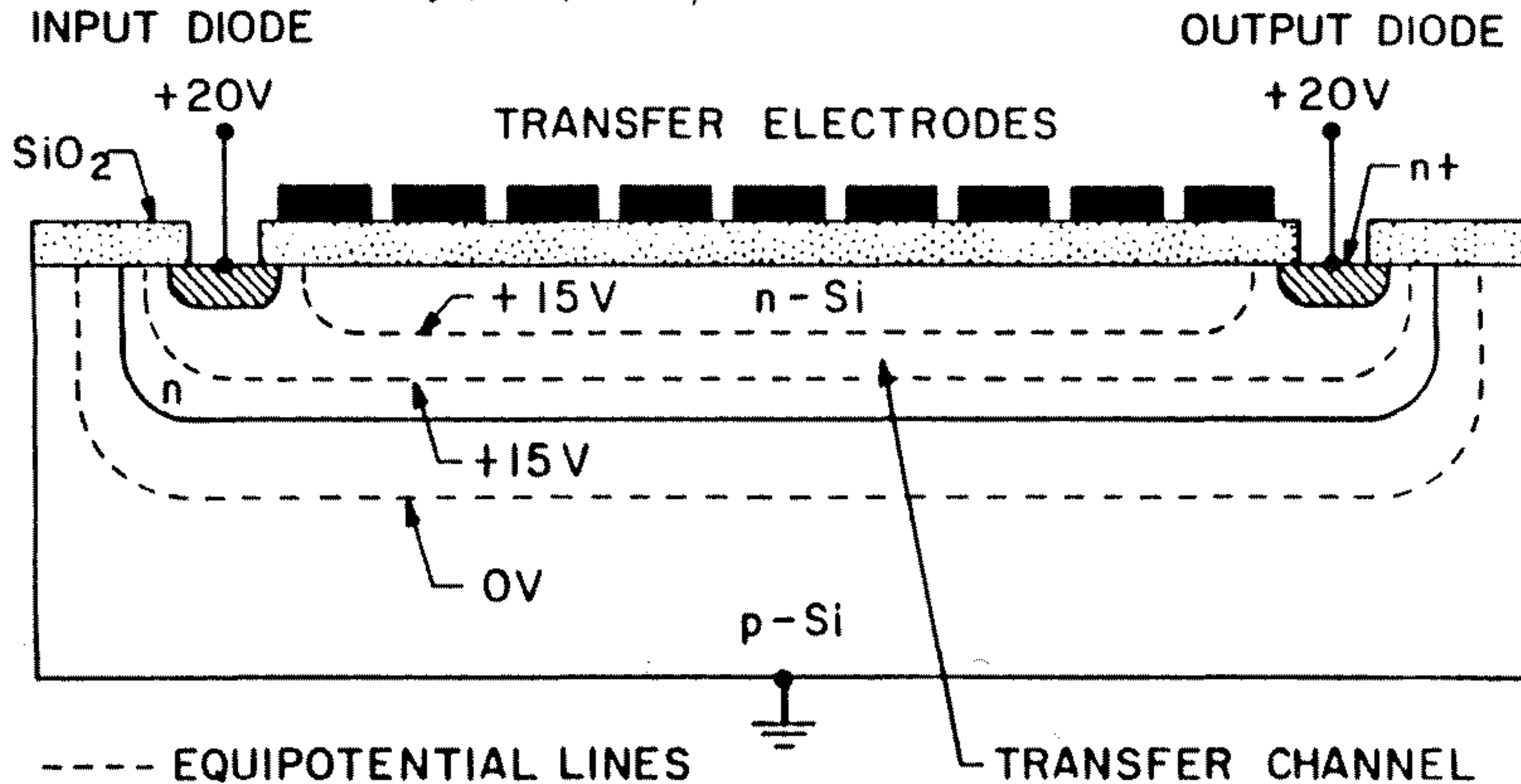


Fig. 1.7 (a)-(e) Movement of potential well and associated charge packet by clocking of electrode voltages; (f) clocking waveforms for a three-phase CCD.

Buried Channel CCD

→ TO REDUCE EFFECTS OF INTERFACE TRAPS BY PUSHING THE CARRIERS FURTHER BELOW THE OXIDE



Same as surface channel CCD except for a weak n implant underneath the CCD gates.

Equivalent Capacitance of CCD's

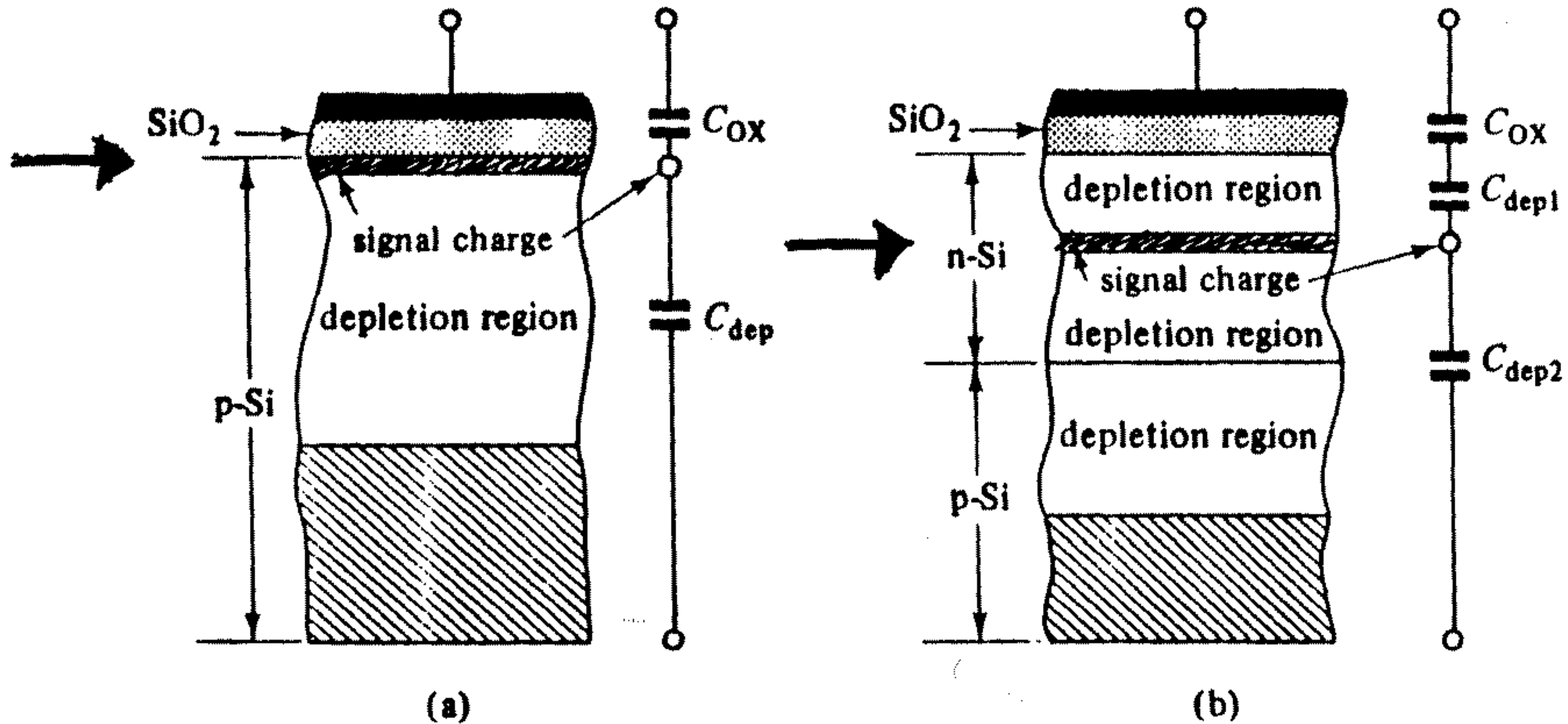


Fig. 2.12 Capacitor equivalent circuits for (a) surface-channel and (b) buried-channel CCDs.

SURFACE CHANNEL

PRO:
- STANDARD CMOS TECH.
- LINEAR Q(V)

CON:
- INTERFACE TRAPS

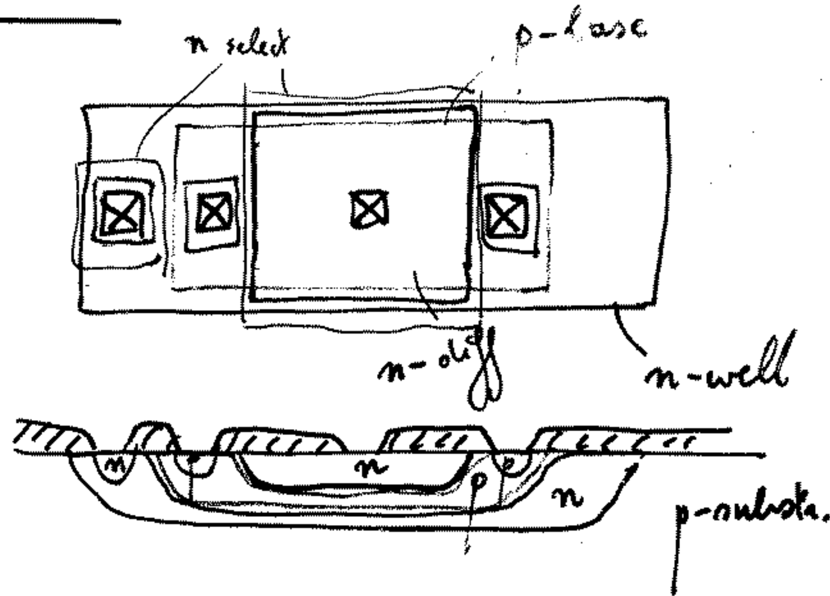
BURIED CHANNEL

PRO:
- BETTER CHARGE TRANSFER EFF.

CON:
- HIGHER VOLTAGES TO DRIVE
- NONLINEAR Q(V)
- EXTRA PROCESSING LAYER

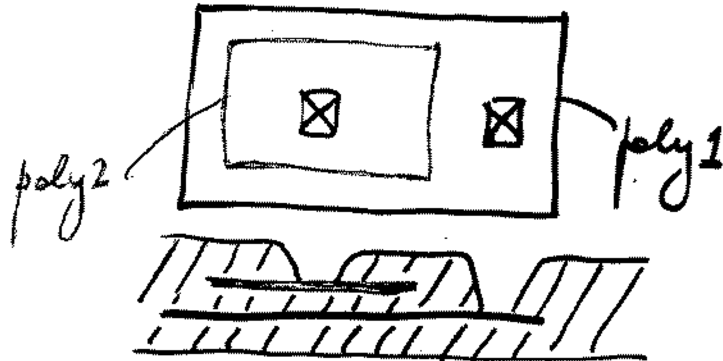
OTHER DEVICES :

- JFET :



- phototransistors, photodiodes: same as BJTs, diodes (base of the phototransistor needs to be left floating to collect photocurrent)

- linear capacitors :



- linear resistors: poly strings ($\rho_{SHEET} \approx 20\,\Omega/\square$)

HI-RES : $1000\,\Omega/\square$
(0.5μm AMIS)