520.492 Mixed-Signal VLSI Systems

Week 2

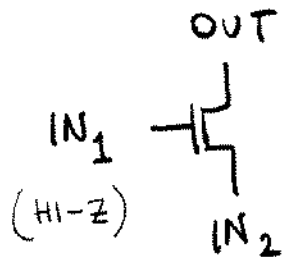
Digital and Analog CMOS Circuitry

References

1. Geiger, Allen and Strader: Chapters 5 and 6.
2. Franca and Tsividis, Chapter 2.
3. Weste and Eshraghian (2nd Ed.), pp. 1-21, 61-91, 207-243, 295-317.
4. Liu, Kramer, Indiveri, Delbruck and Douglas, *Analog VLSI* (MIT Press).

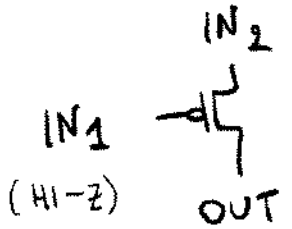
CMOS LOGIC

Weste & Eshraghian pp { 1-21, 61-71, 207-243, 295-317



GND = "0"
V_{dd} = "1"

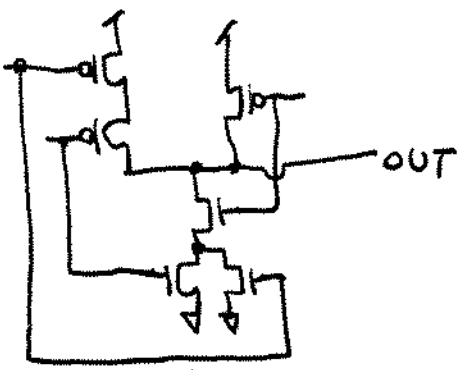
IN_1	IN_2	OUT
0	0	HI-Z
0	1	HI-Z
1	0	0
1	1	(1) ← POOR; AVOID



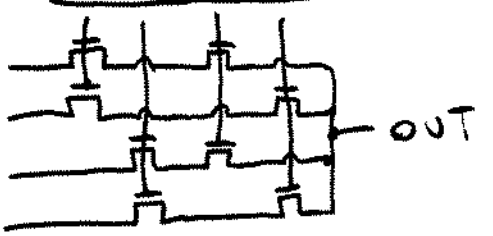
IN_1	IN_2	OUT
0	0	(0) ← POOR; AVOID
0	1	1
1	0	HI-Z
1	1	HI-Z

3 "modes" in CMOS:

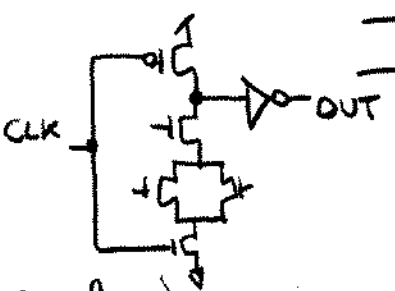
1) COMPLEMENTARY LOGIC (STATIC):



2) PASS TRANSISTOR LOGIC: (STATIC)



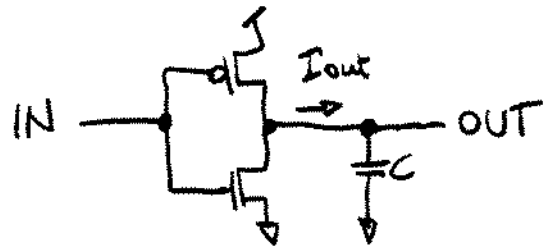
3) DYNAMIC CMOS:



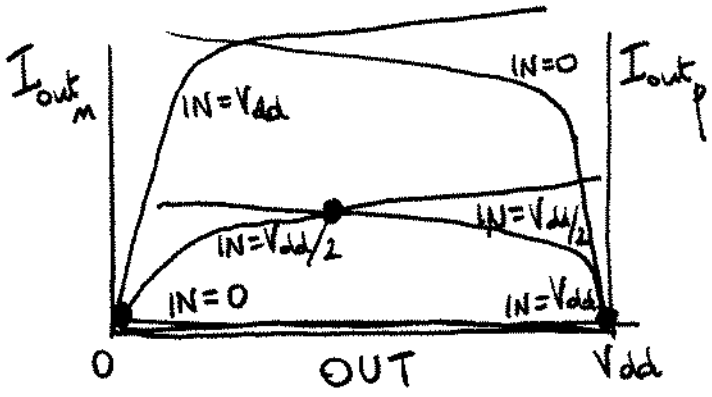
+ variants; combinations

EXAMPLES :

① CMOS INVERTER



IN	OUT
0	1
1	0



RATIOING:

$\mu_p \cong \frac{2}{5}\mu_n \Rightarrow \left(\frac{W}{L}\right)_p := \frac{5}{2}\left(\frac{W}{L}\right)_n$

POWER DISSIPATION :

static : NIL

dynamic : $P_{dyn} = f C V_{dd}^2$

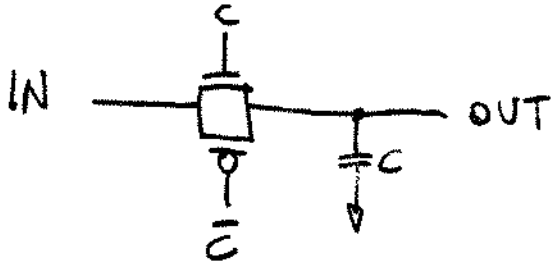
SPEED :

rise time / fall time : $\tau \div \frac{C}{\beta . V_{dd}}$

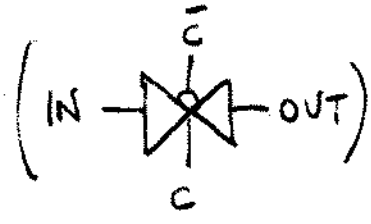
$\Big\} \quad \frac{f C^2 V_{dd}}{\beta}$

$(\beta \div C_{ox}\mu\frac{W}{L})$

② PASS GATE (TRANSMISSION GATE)



C	OUT
0	OUT
1	IN



R-C chain effects ! intermediate buffering needed

COMBINATORIAL LOGIC

$$Y = f(X)$$

a) Boolean algebra

$A \cdot \emptyset = \emptyset$
$A + \emptyset = A$
$A + \bar{A} = 1$
$A \cdot \bar{A} = \emptyset$

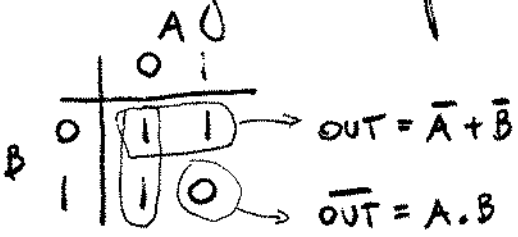
$(A + B) \cdot C = A \cdot C + B \cdot C$
$A \cdot B = B \cdot A$ $\qquad A + B = B + A$

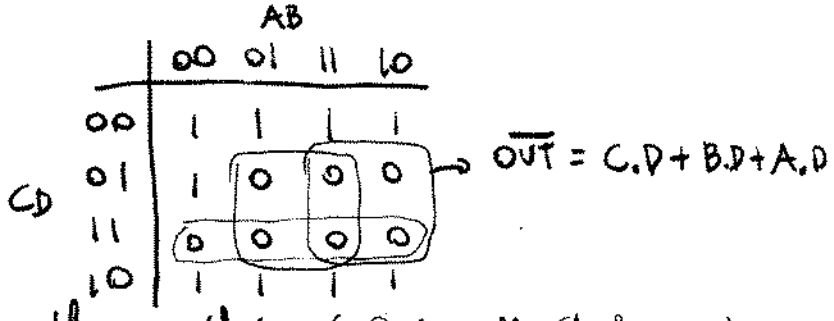
De Morgan: $\overline{A + B} = \bar{A} \cdot \bar{B}$
$\overline{A \cdot B} = \bar{A} + \bar{B}$

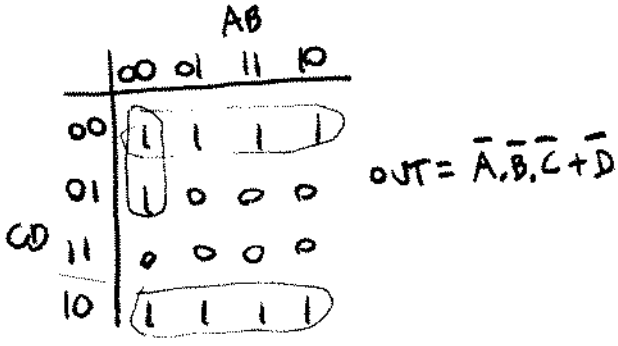
b) Synthesis

- KARNAUGH: Expansion of the boolean variable (or its complement) in a minimal sum of product combinations of the input operands

example:



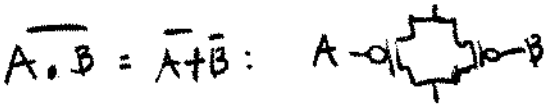


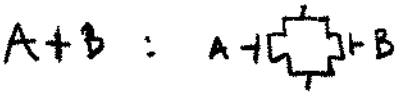


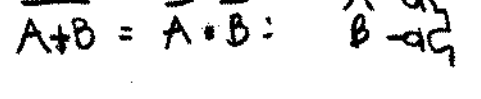
- other methods (Quine - Mc Cluskey, ...)

c) CMOS realization:

$A \cdot B$: 

$\overline{A \cdot B} = \bar{A} + \bar{B}$: 

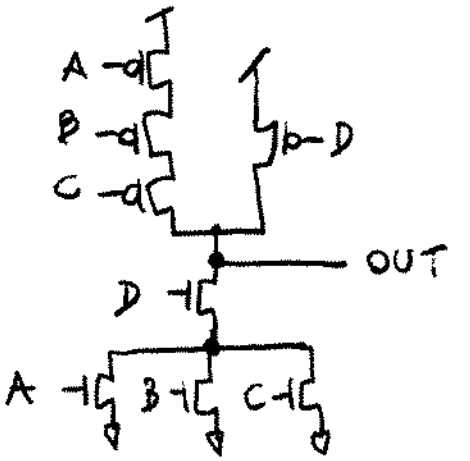
$A + B$: 

$\overline{A + B} = \bar{A} \cdot \bar{B}$: 

- COMPLEMENTARY CMOS :

$$\overline{OUT} = (A + B + C).D$$

$$OUT = \bar{A}.\bar{B}.\bar{C} + \bar{D}$$

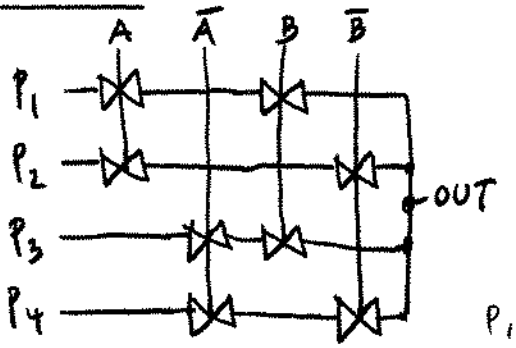


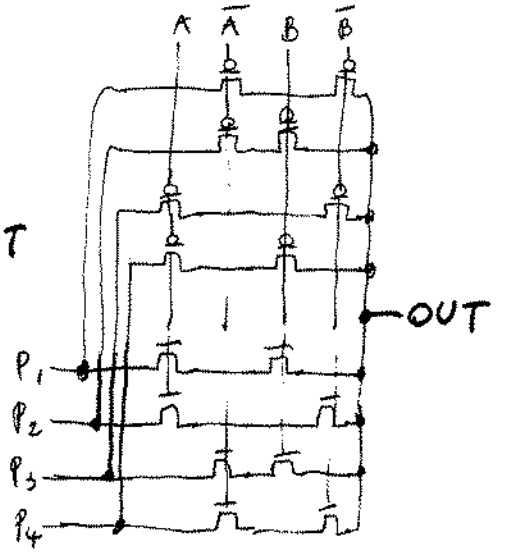
p ⟷ n permutation by series ⟷ parallel (De Morgan)

- PASS TRANSISTOR LOGIC :

e.g. : MUX

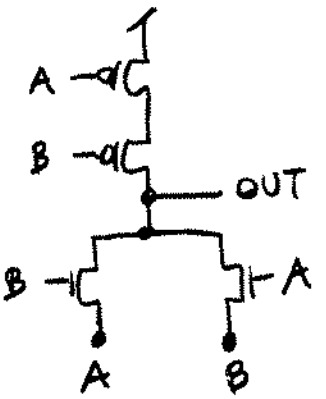
A	B	OUT
0	0	P_4
0	1	P_3
1	0	P_2
1	1	P_1

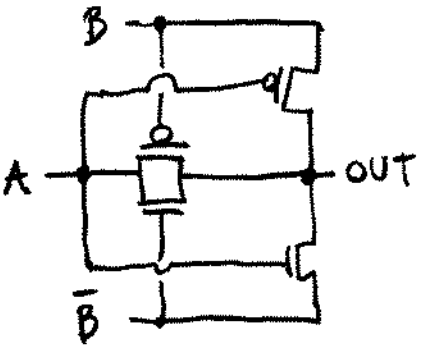




- extends to analog MUX
- disadvantage : R-C delays for long chains

- COMPOSITES :

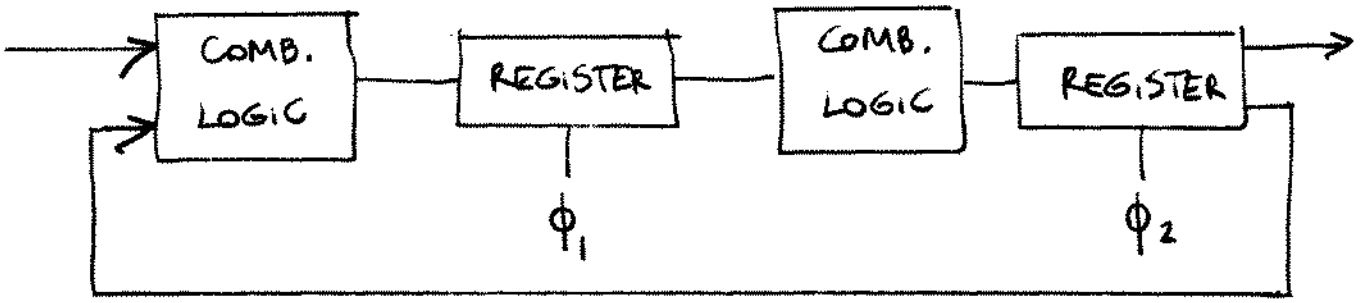


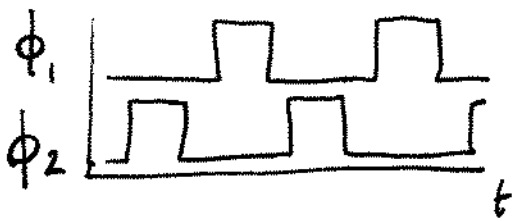


SEQUENTIAL LOGIC

$$Y_n = f(X_n, Y_{n-1})$$

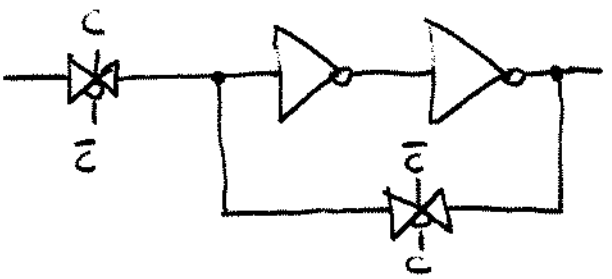
→ finite-state machines, etc...



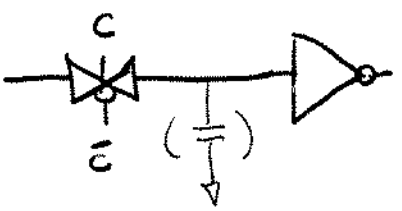


Registers :

static :



dynamic :



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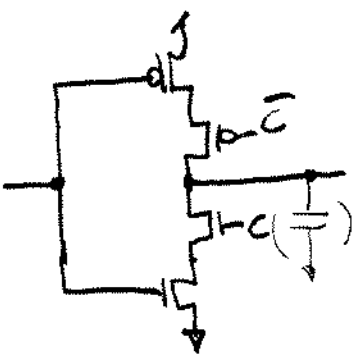
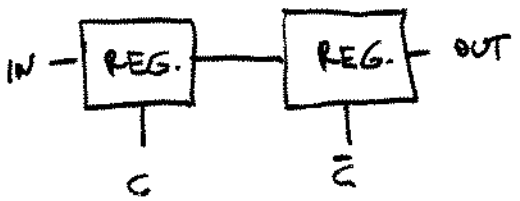
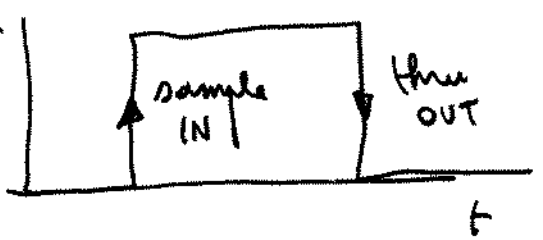
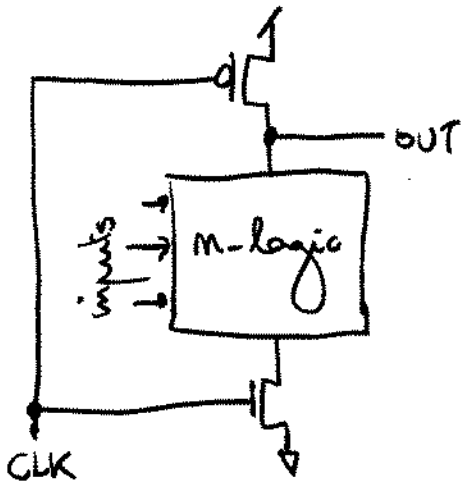


edge-triggered :

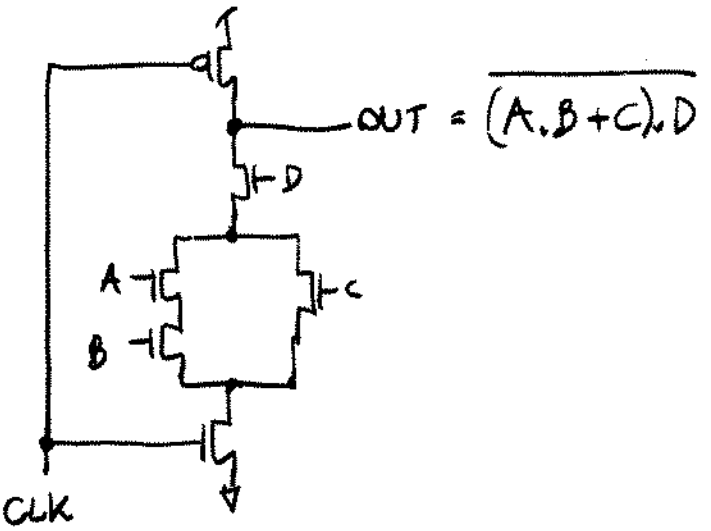


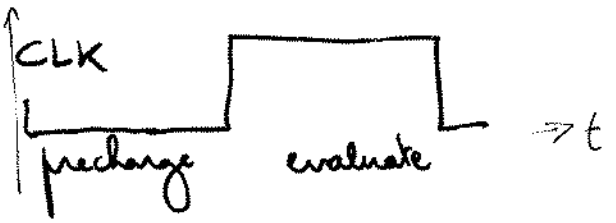


DYNAMIC CMOS LOGIC



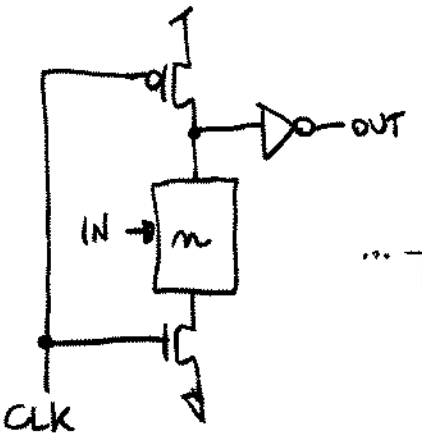
example :

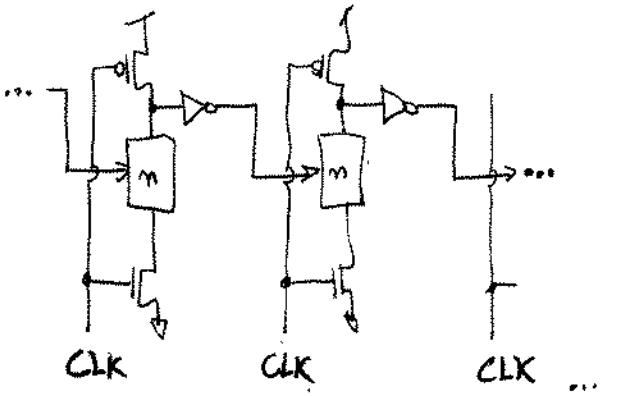




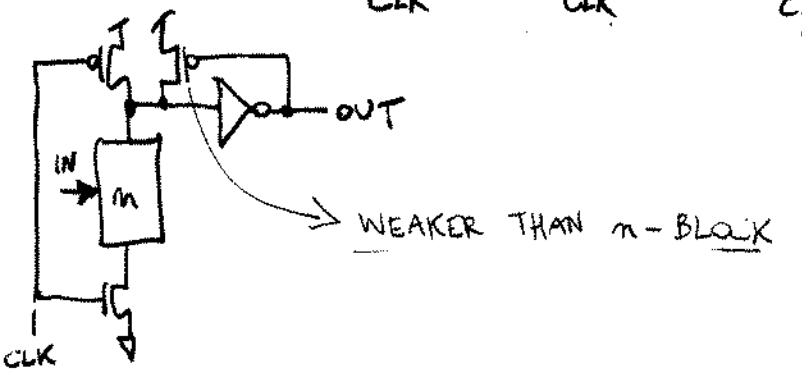
VARIANTS:

Domino Logic :





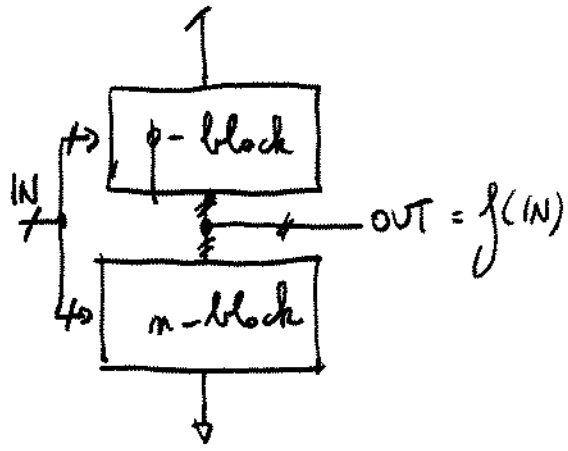
Static counterpart :

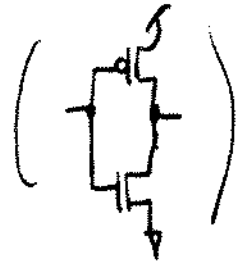


Summary of CMOS logic "families"

COMPLEMENTARY:

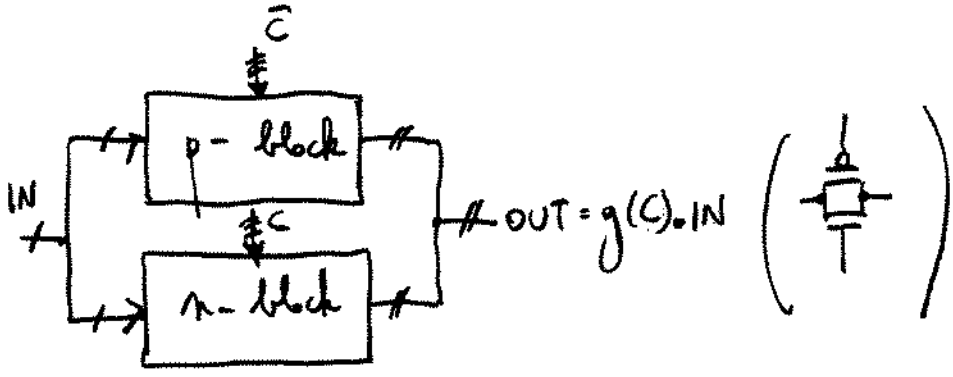
HI-Z IN
LO-Z OUT





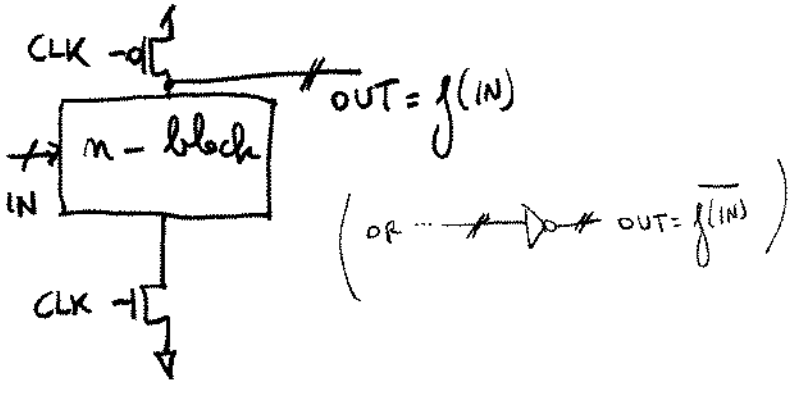
PASS TRANSISTOR:

LO-Z IN
LO-Z OUT



DYNAMIC:

HI-Z IN
HI/LO-Z OUT
"TRI"



n-block: synthesis of $f(IN)$ { "1" = short, "0" = open }, and with { "+": in parallel, ".": in series }

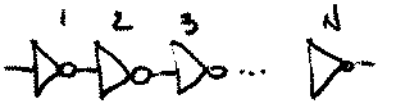
p-block: "complement" of n-block, with:

for → complementary logic: series ⟷ parallel permutation
→ pass transistor: complement the pass gate inputs (C)

Cascading of logic gates

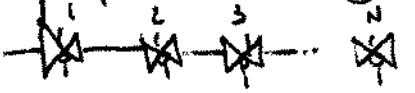
COMBINATORIAL:

Complementary logic: Hi-Z IN, Lo-Z OUT



$\tau_{prop} = N \times \tau_{stage}$

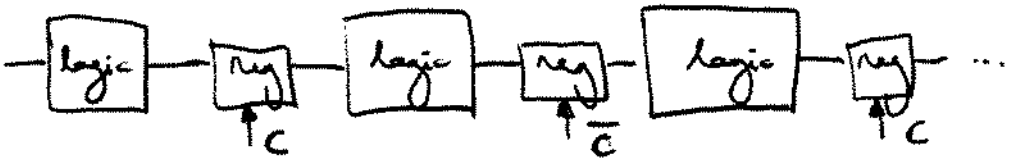
pass-transistor logic: Lo-Z IN, Lo-Z OUT



$\tau_{prop} \propto N^2 \times \tau_{stage}$ (smaller though)

optimum: include buffers (-▷o-) every 2-8 stages

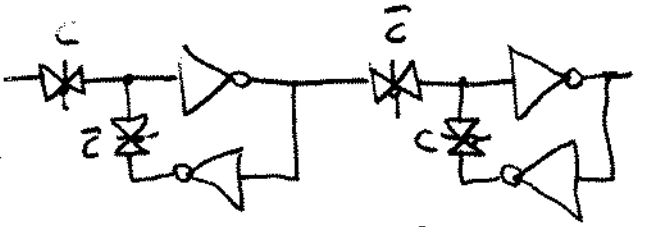
SEQUENTIAL: PIPELINING



speed ↑ as τ stage ↓ ⇒ "micro-pipelining"

caveats:

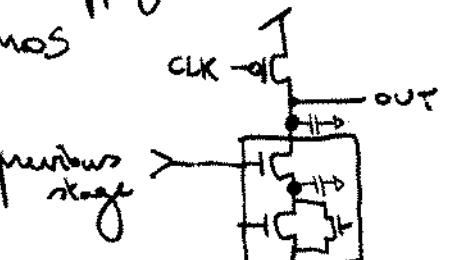
1) signal leak through:



$C = \bar{C} = 1$ transient

remedy: two-phase non-overlapping clock

2) charge redistribution in dynamic CMOS



remedy: apply a set of proper cascading rules

(e.g.: Yuan & Svensson: single-phase clock)

ANALOG CMOS

CIRCUITS

- differential pairs
- current mirrors / conveyors
- transconductance amplifiers / comparators
- source followers
- switches
- multipliers

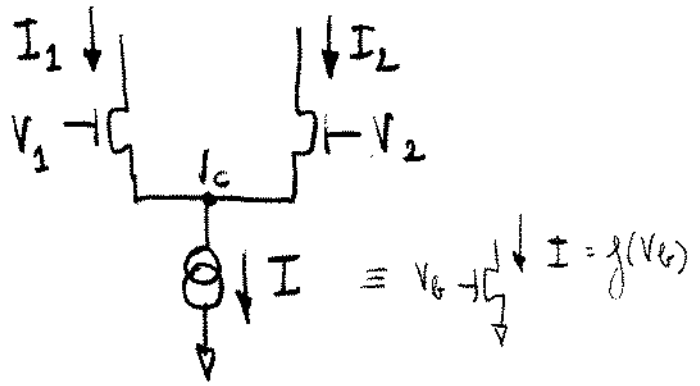
SYSTEMS

- current-mode
- transconductance mode
- charge-mode

references:

- Franca & Tsividis, Chapter 2
- Geiger, Allen & Strader, Chapter 5, 6

DIFFERENTIAL PAIR



subthreshold

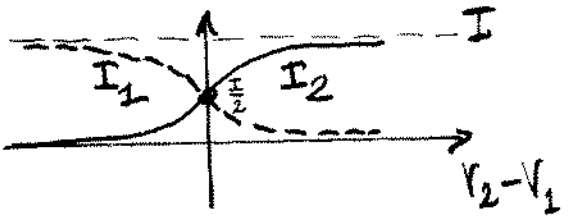
$$I_1 = I_0 \, e^{\frac{\kappa V_1 - V_c}{V_t}}$$

$$I_2 = I_0 \, e^{\frac{\kappa V_2 - V_c}{V_t}}$$

$$I = I_1 + I_2$$

$$I_1 = \frac{1}{1 + e^{\frac{\kappa(V_2 - V_1)}{V_t}}} I$$

$$I_2 = I - I_1$$

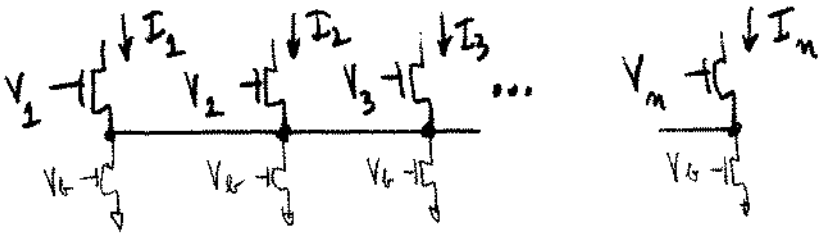


above threshold

$$I_1 = \frac{\beta}{2} (\kappa V_1 - V_c - V_T)^2 \quad \text{etc...}$$

$$I_2 = \frac{\beta}{2} (\kappa V_2 - V_c - V_T)^2$$

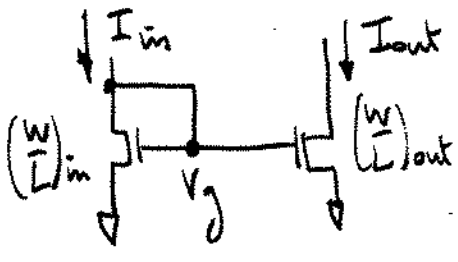
generalization :

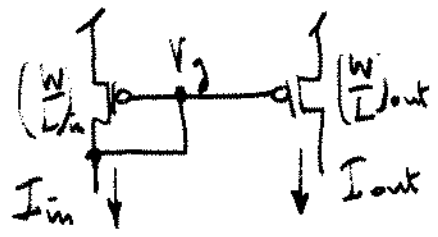


$$I_i = \frac{e^{\kappa \frac{V_i}{V_t}}}{\sum_{j=1}^{n} e^{\kappa \frac{V_j}{V_t}}} \cdot I \qquad (I = n \cdot f(V_G))$$

in subthreshold

CURRENT MIRROR





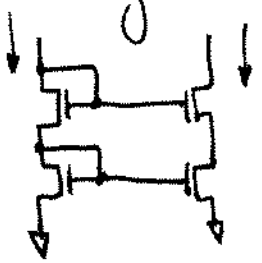
$$I_{out} \approx I_{in} \frac{\left(\frac{W}{L}\right)_{out}}{\left(\frac{W}{L}\right)_{in}}$$

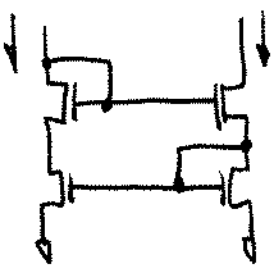
problem : drain conductance

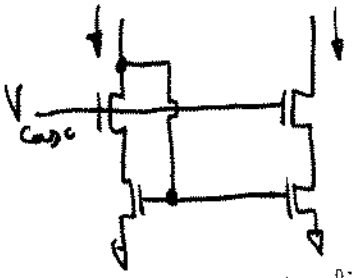
$$I_{out} = \underbrace{I_0 \, e^{\kappa \frac{V_g}{V_t}}}_{\text{or: } \frac{\beta}{2}(kV_g)^2} \left(1 + \frac{V_{out}}{V_{early}}\right)$$

V_{early} → early effect

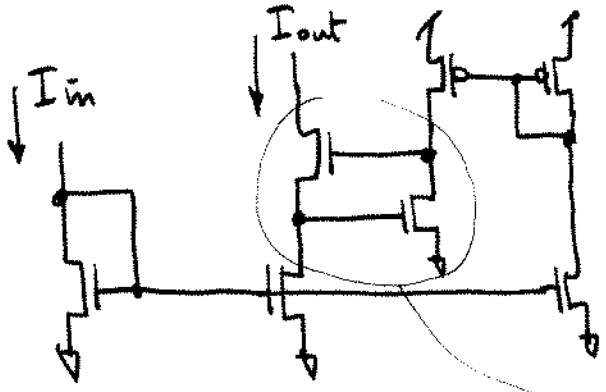
remedy : cascode :

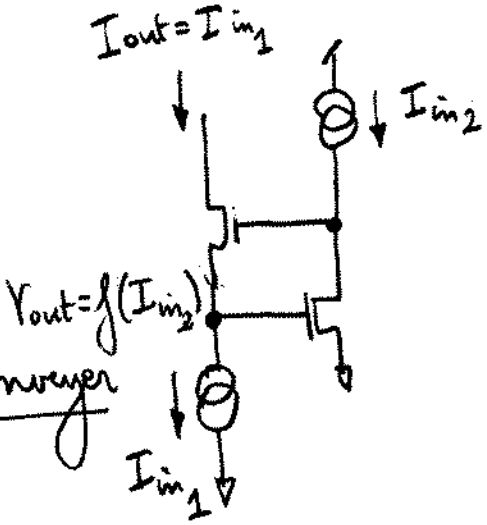






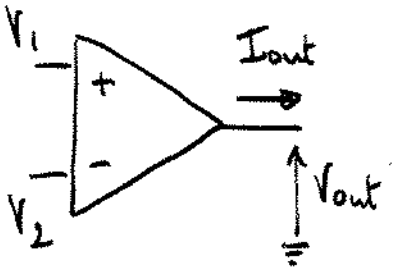
(current limited)





current conveyer

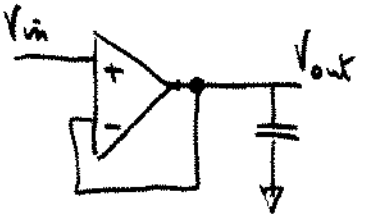
TRANSCONDUCTANCE AMPLIFIER (also, COMPARATOR)



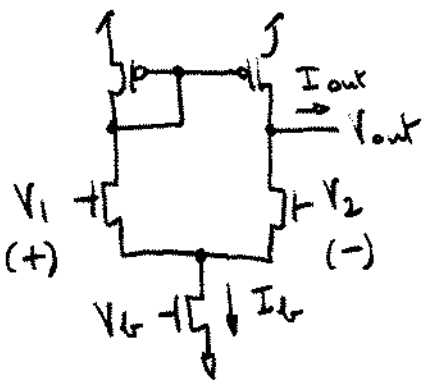
$$I_{out} = g_D(V_1 - V_2) + g_{CM}\frac{V_1+V_2}{2} + g_O V_{out}$$

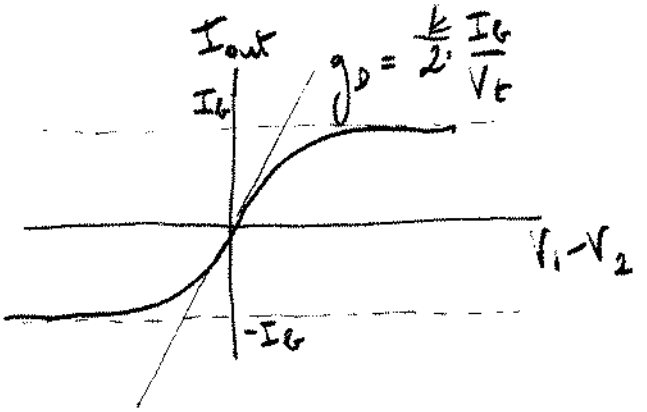
$g_{CM} \to 0$
$g_O \to 0$; g_D "high"

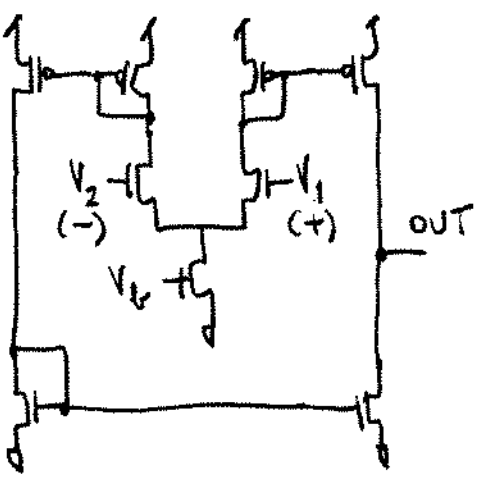
example :



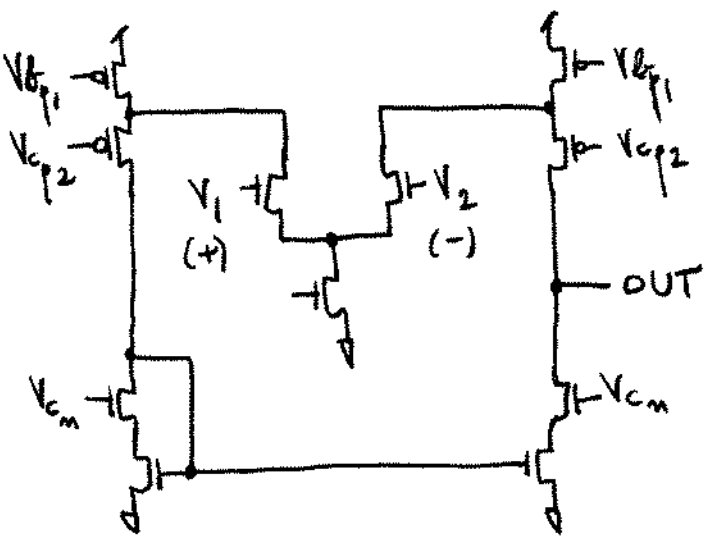
$$V_{out} = \frac{1}{1+Zs} V_{in} \quad \left(Z = \frac{C}{g_D}\right)$$





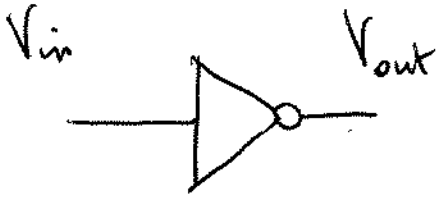


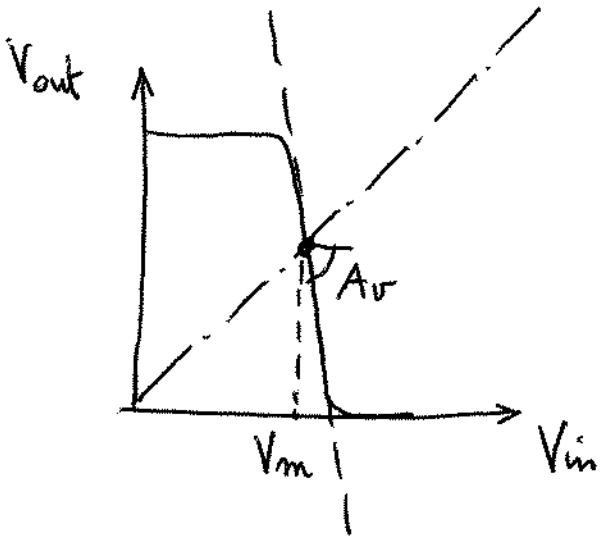
WIDE RANGE



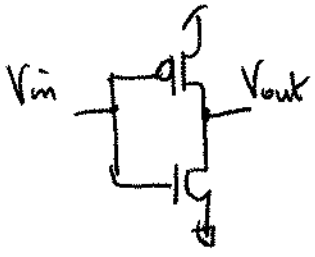
FOLDED CASCODE

INVERTING AMPLIFIER





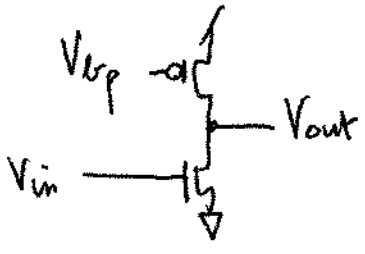
1) CMOS inverter



poor A_v ! (except at low V_{dd})

$V_m \sim$ midrange

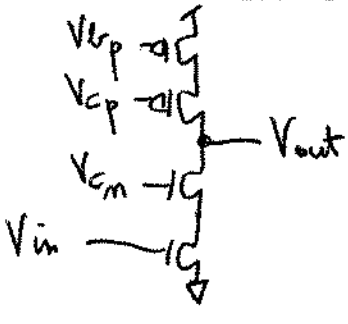
2) nMOS inverter



$$A_v \approx -\frac{g_{m_N}}{g_{ds_N} + g_{ds_P}}$$ large in subthreshold

$V_m \sim V_{T_n}$ (nMOS threshold)

3) cascoded nMOS inverter



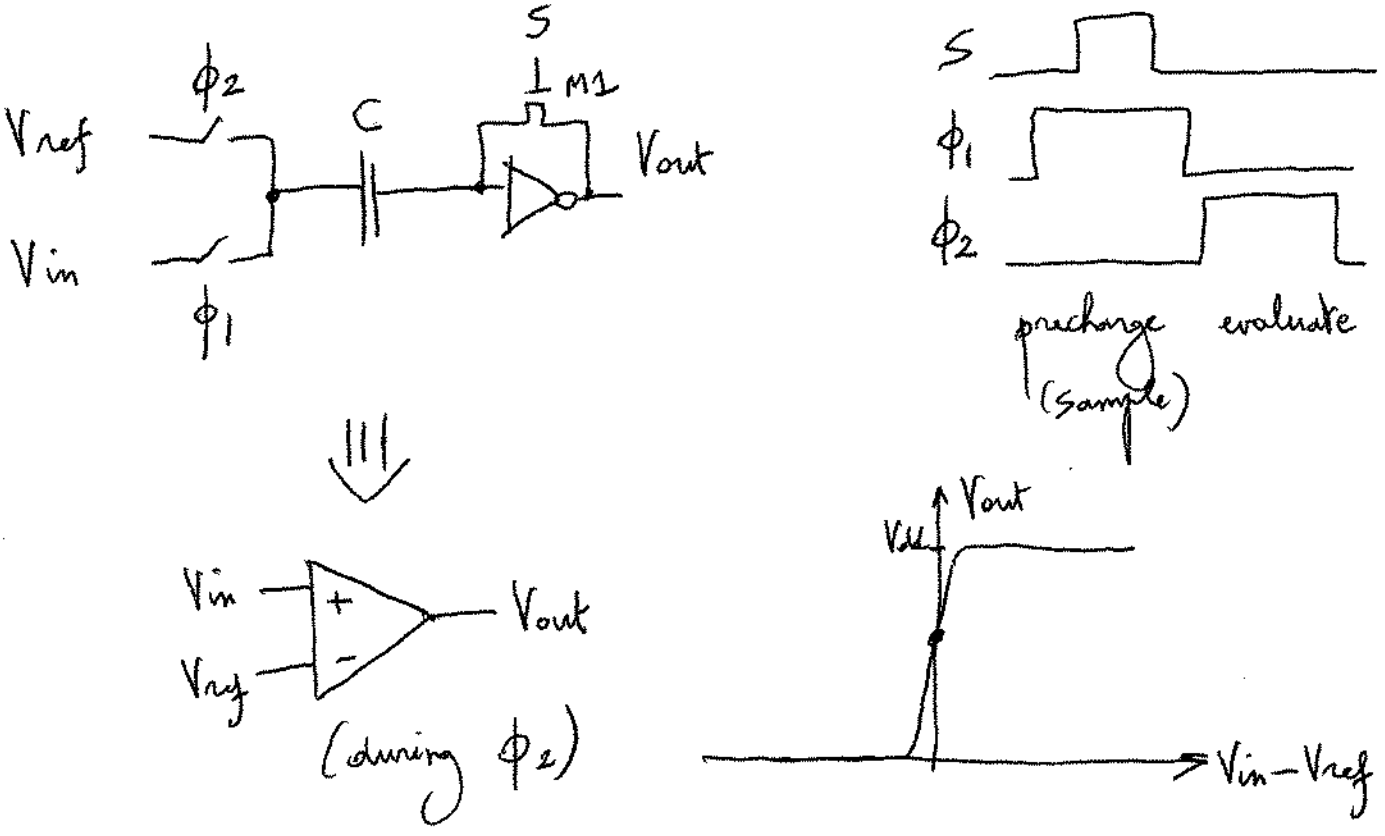
$$A_v \approx -\frac{g_{m_N}}{g_{ds_N}^2/g_{m_N} + g_{ds_P}^2/g_{m_P}}$$ very large!

high speed!

$V_m \sim V_{T_n}$

4) pMOS equivalents ($V_m \sim V_{dd} - |V_{T_p}|$)

CORRELATED DOUBLE SAMPLING ("CDS")



ϕ_1 (S): sample V_{in}, minus V_m (internal threshold of amplifier)

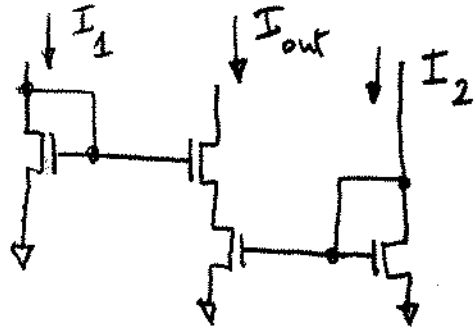
ϕ_2: evaluate difference with V_{ref}, cancelling V_m

$$\Rightarrow (V_{in} - V_m) - (V_{ref} - V_m) = V_{in} - V_{ref}$$

Residual offset is due to charge injection by M1, but is independent of V_{in} (and constant for a given process technology)

MULTIPLIERS

current mode :

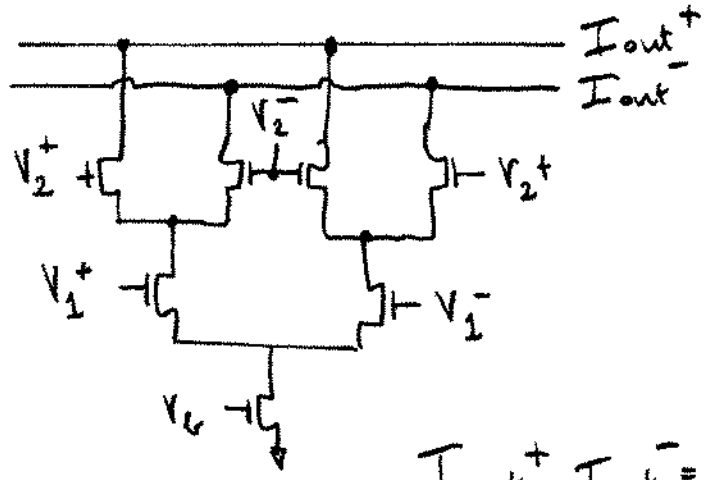


$$I_{out} = \frac{I_1 \cdot I_2}{I_1 + I_2}$$

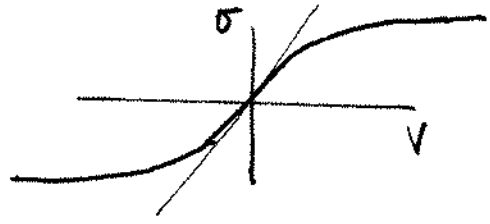
(subthreshold)

transconductance mode :

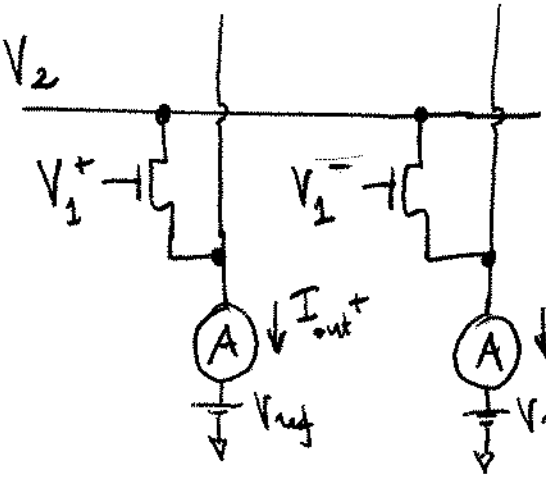
① (Hi-Z OUT)



$$I_{out}^+ - I_{out}^- = \sigma(V_1^+ - V_1^-) \cdot \sigma(V_2^+ - V_2^-)$$



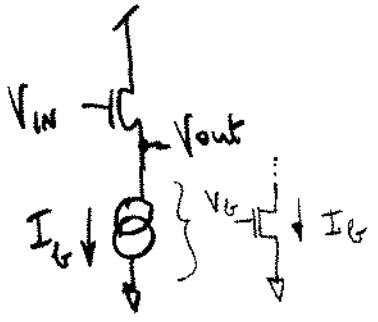
② (above threshold ; quadratic I-V law :)



$$\begin{cases} I_{out}^+ = \beta (V_1^+ - V_{ref} - V_{TN})(V_2 - V_{ref}) - \frac{\beta}{2}(V_2 - V_{ref})^2 \\ I_{out}^- = \beta (V_1^- - V_{ref} - V_{TN})(V_2 - V_{ref}) - \frac{\beta}{2}(V_2 - V_{ref})^2 \end{cases}$$

$$\Rightarrow I_{out}^+ - I_{out}^- = \beta (V_1^+ - V_1^-)(V_2 - V_{ref})$$

SOURCE FOLLOWERS

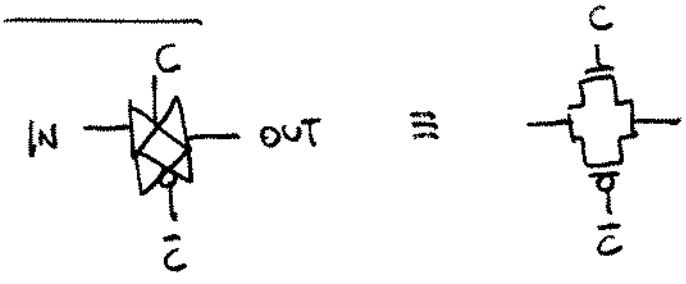


$$V_{out} \approx \kappa V_{in} - V_t \log \frac{I_b}{I_0}$$

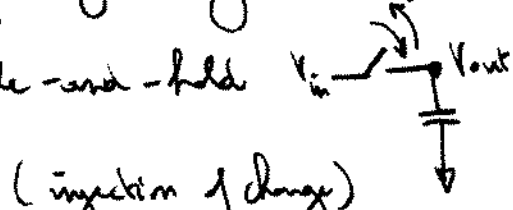
$$\left(I_b = I_0 \, e^{\frac{\kappa V_{in} - V_{out}}{V_t}} \right)$$

subthreshold

SWITCHES

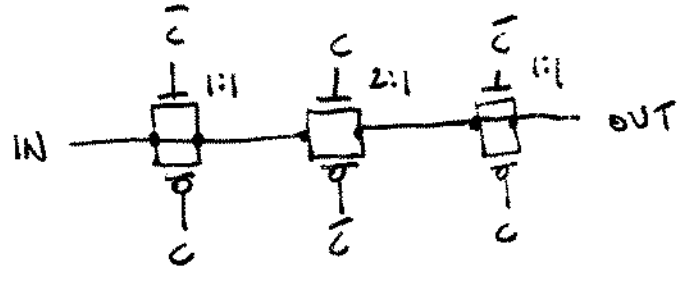


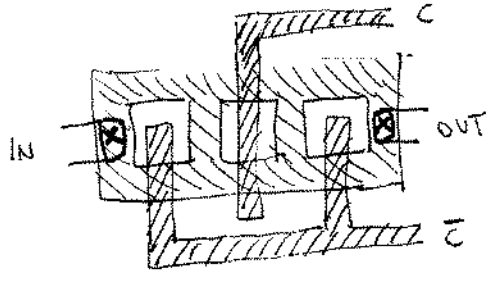
uses:
- analog MUX (same as pass-gate digital CMOS)
- switched capacitors ; sample-and-hold



problem: clock feedthrough (injection / charge)

remedy:





CIRCUIT SYNTHESIS in analog CMOS

motives : { – high density, low power
– large degree of parallelism

- distribution of variables → analog voltages
- parallel summation → currents ; charges

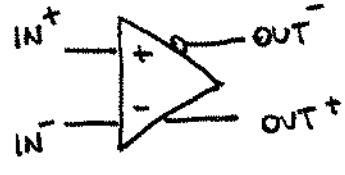
current mode : . mirrors
. current conveyors
. translinear circuits (subthreshold)

transconductance mode :

sampled filters { . transconductance amplifiers (*) } continuous-time filters
. capacitors
. switches

charge mode : . capacitor banks ; charge redistribution
. CCD's ; CID's
charge coupled devices ; charge injection devices
. charge sense amplifiers

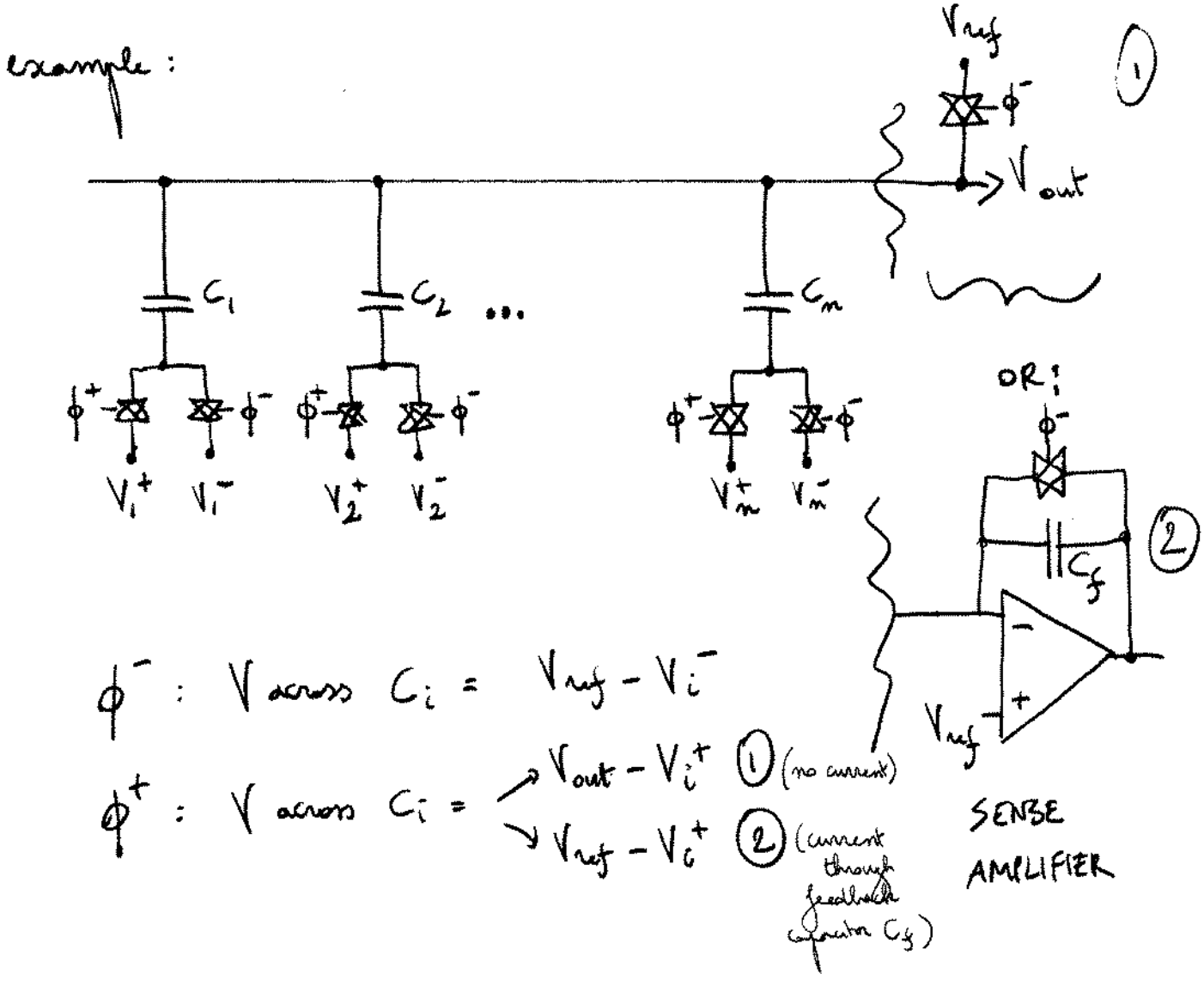
(*) + variants :



differential techniques

CHARGE MODE :

example :



ϕ^- : V across C_i = $V_{ref} - V_i^-$

ϕ^+ : V across C_i = $\nearrow V_{out} - V_i^+$ ① (no current)

$\searrow V_{ref} - V_i^+$ ② (current through feedback capacitor C_f)

$$\Rightarrow V_{out}(\phi^+) = V_{ref} + \lambda \cdot \sum_{i=1}^{n} C_i \left(V_i^+ - V_i^-\right)$$

$$\lambda = \nearrow 1 / \sum_{i=1}^{n} C_i \quad ①$$

$$\searrow -1/C_f \quad ②$$