Introduction to the SkyWater PDK

The New Age of Open Source Silicon

Tim Edwards

SVP Analog & Platform

efabless

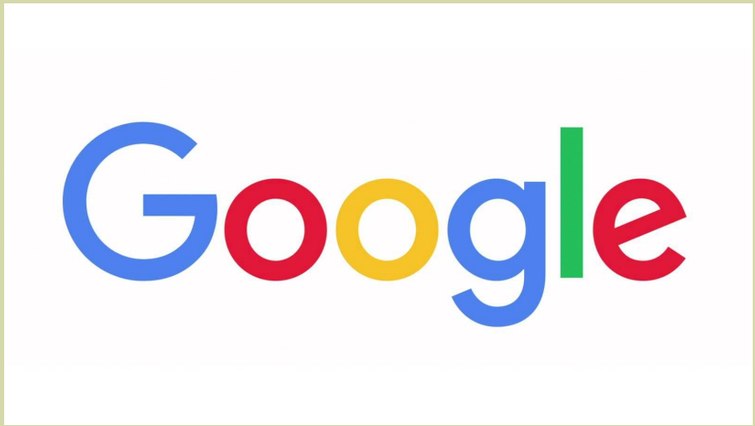
efabless.com

Open Circuit Design

opencircuitdesign.com

October 8, 2021

Introduction to the SkyWater PDK



Introduction to the SkyWater PDK

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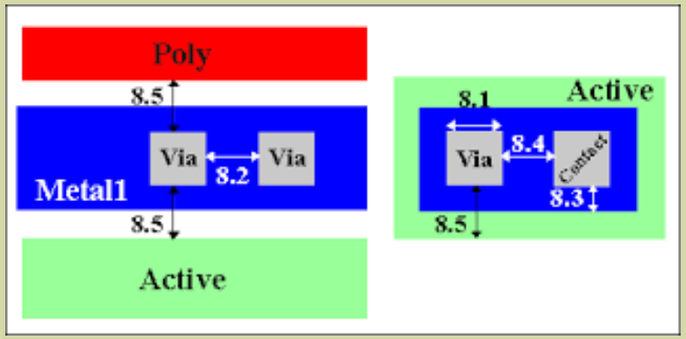
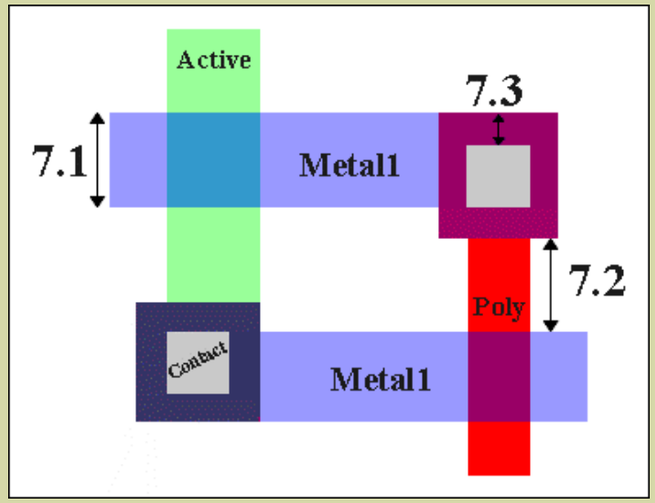




Introduction to the SkyWater PDK

130nm SCMOS

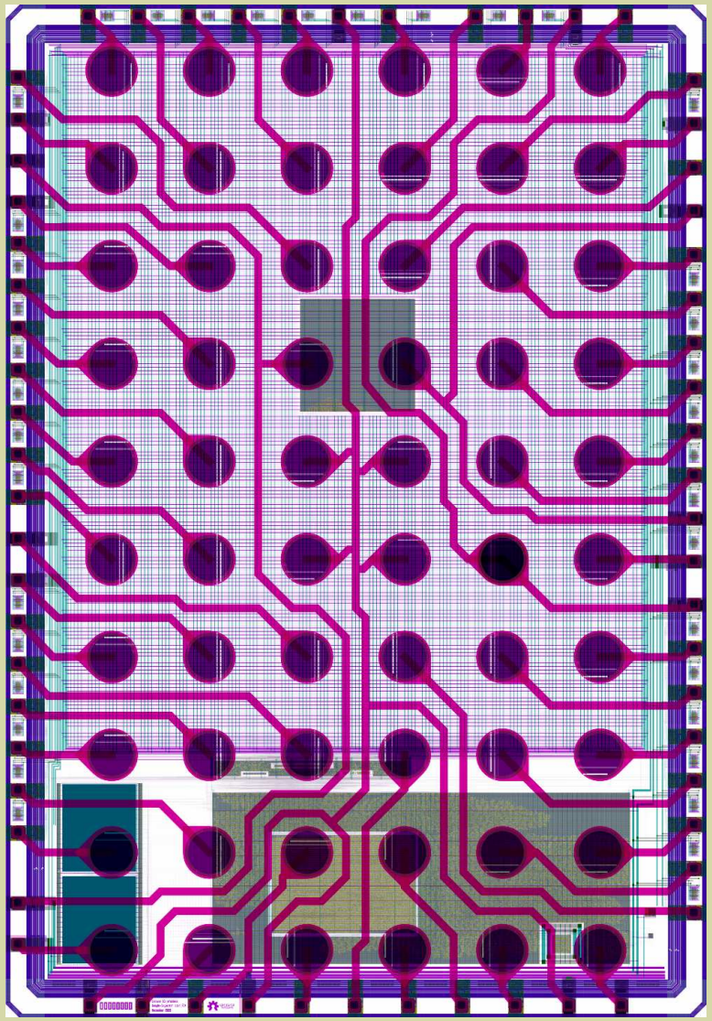
Introduction to the SkyWater PDK

130nm SCMOS

https://github.com/google/skywater-pdk

Introduction to the SkyWater PDK

Introduction to the SkyWater PDK

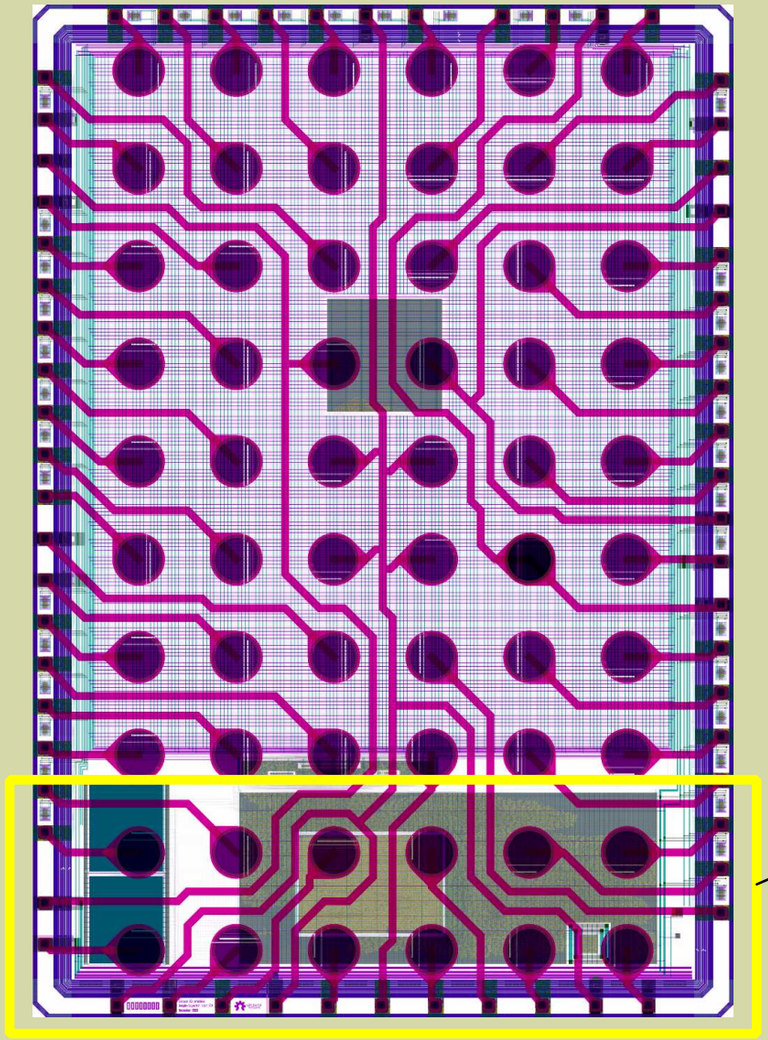


efabless.com

The "Caravel" harness chip

Introduction to the SkyWater PDK

efabless.com

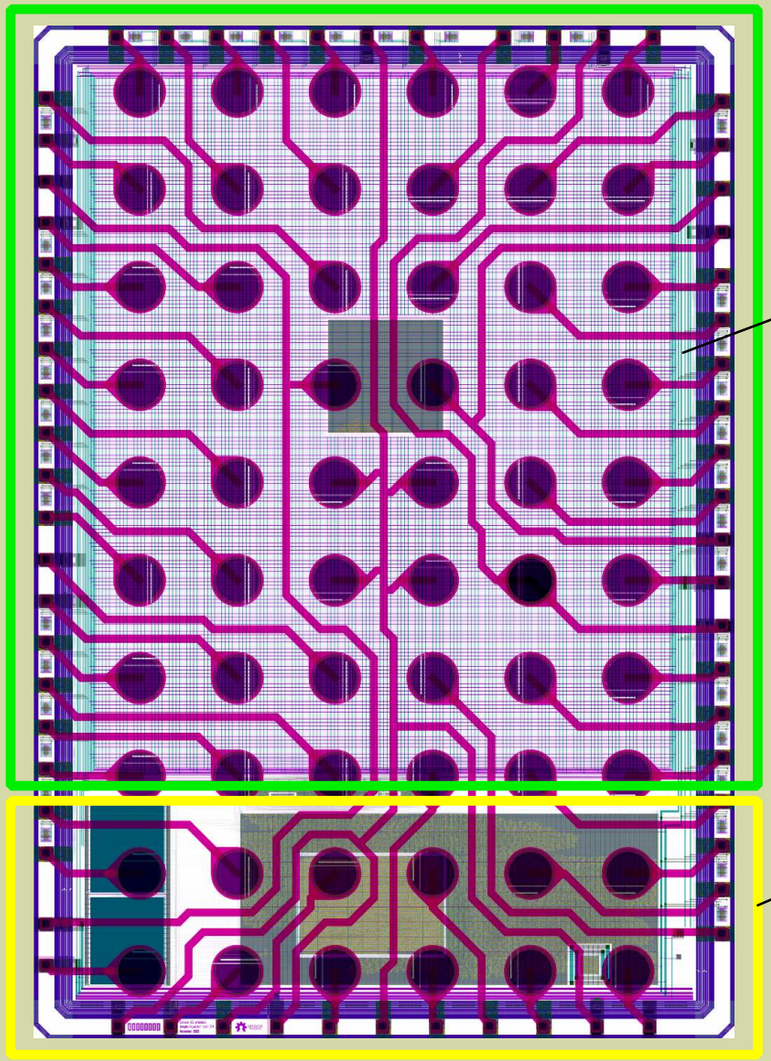


The "Caravel" harness chip

RISC-V processor

Introduction to the SkyWater PDK

efabless.com



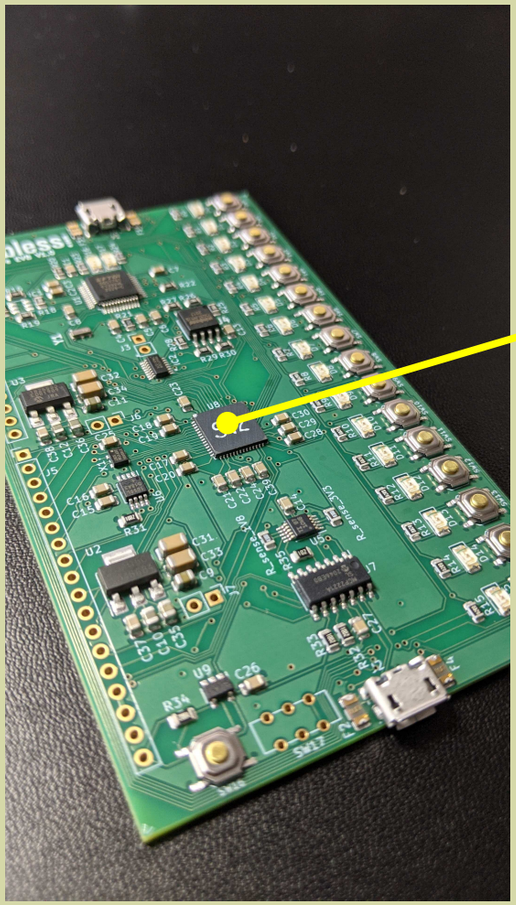
user project area

The "Caravel" harness chip

RISC-V processor

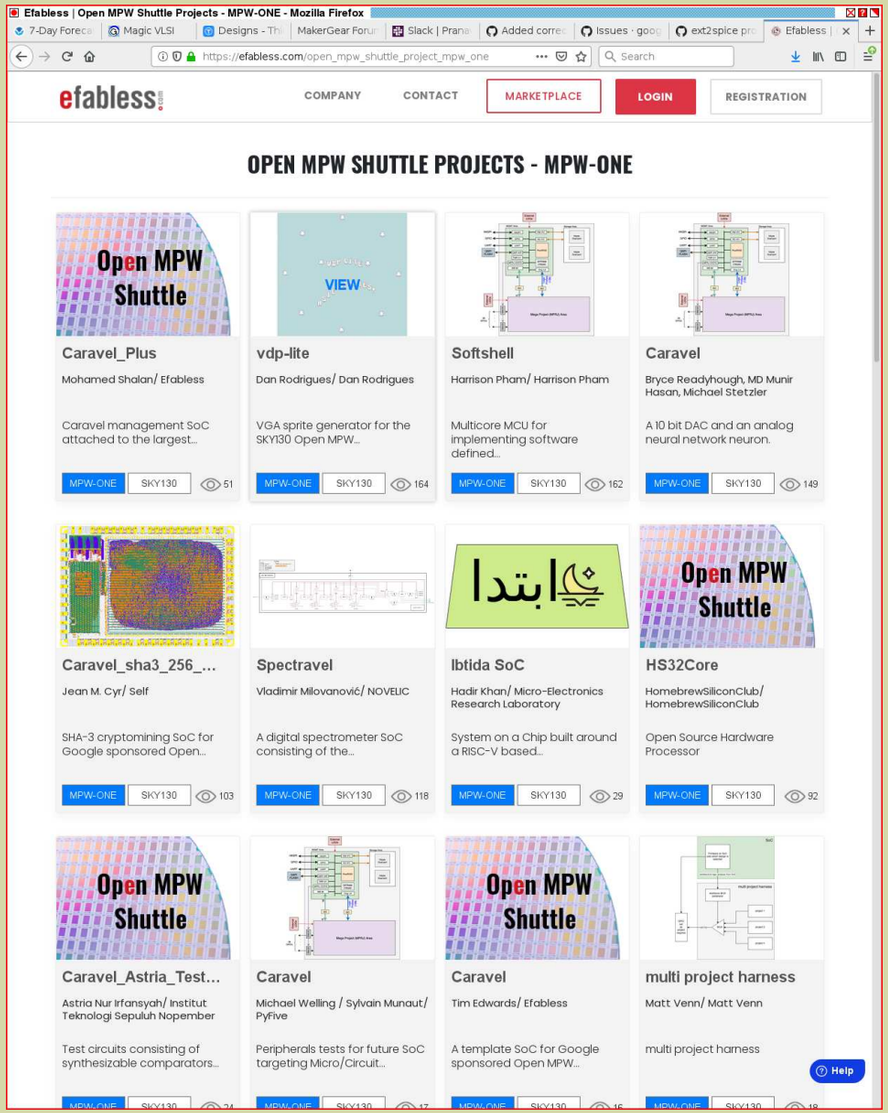
Introduction to the SkyWater PDK

efabless.com



Your project here!

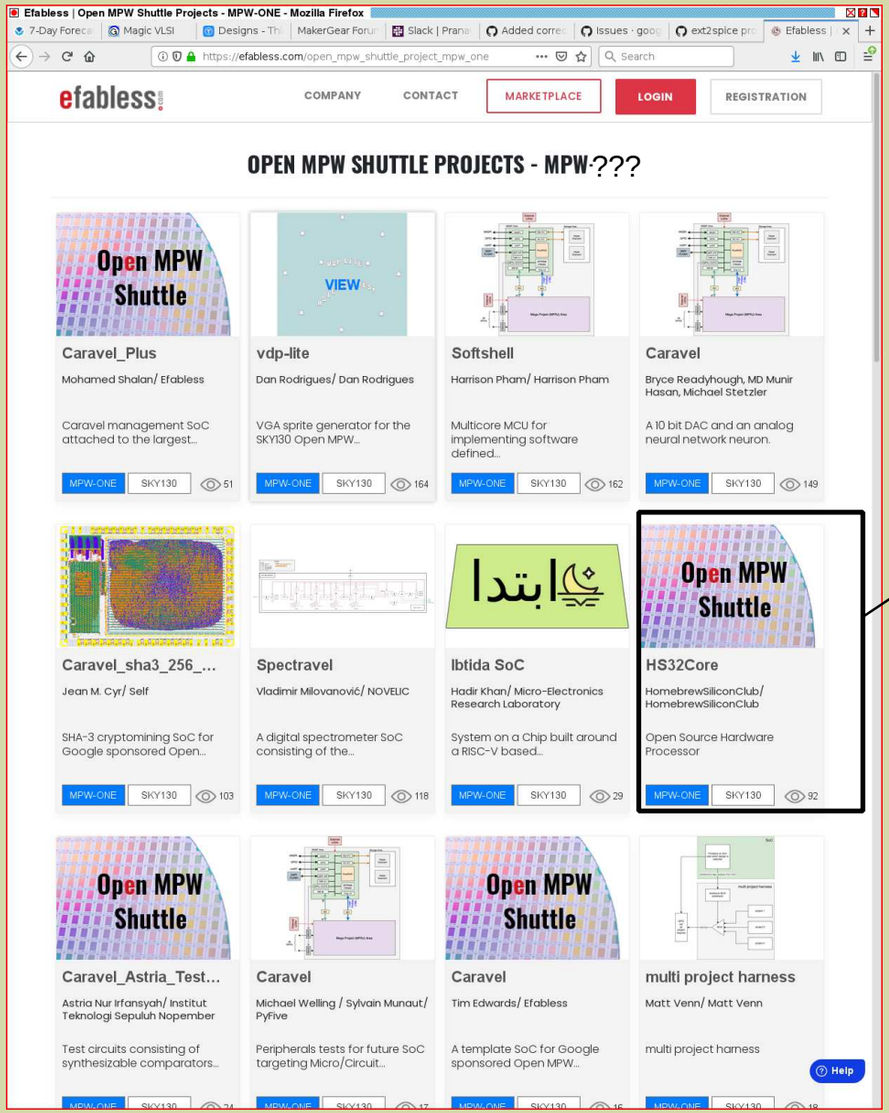
Introduction to the SkyWater PDK



Projects on Google/SkyWater MPW-One

https://efabless.com/open_mpw_shuttle_project_mpw_one

Introduction to the SkyWater PDK



Your project here!

The SkyWater Open PDK

PDK = "Process Design Kit"

The SkyWater Open PDK

SKY130

The SkyWater Open PDK

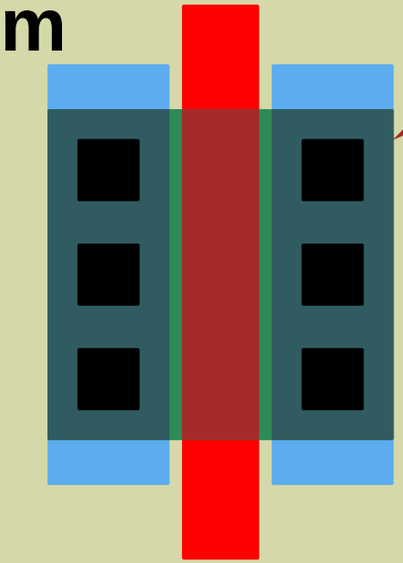
SKY130

130 nm

The SkyWater Open PDK

SKY130

130 nm



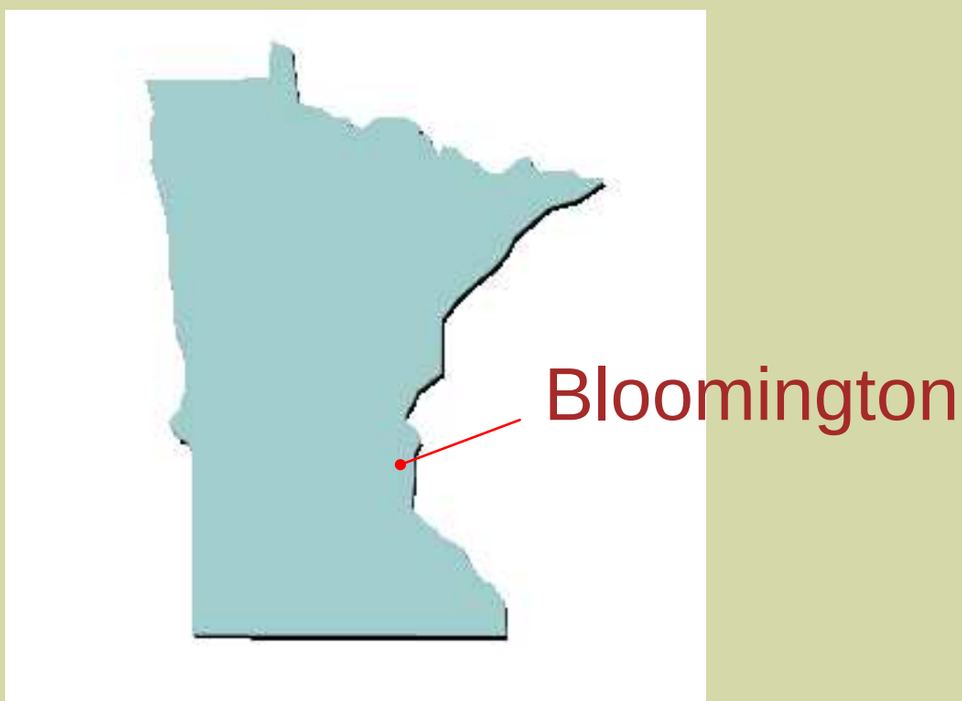
minimum-length transistor*

transistor length = 130 nm

"feature size"

*caveat: for obscure reasons, the minimum size device in the SKY130 process is actually 150 nm. . .

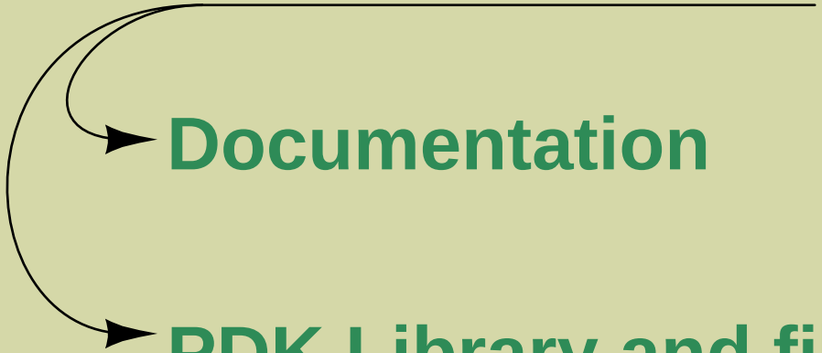
The SkyWater Open PDK



Minnesota

The SkyWater Open PDK

Public repository

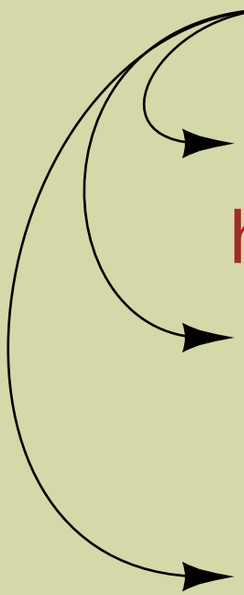


- Documentation
- PDK Library and files

The SkyWater Open PDK

The SkyWater Open PDK

Public repository



Documentation

https://skywater-pdk--136.org.readthedocs.build

PDK Library and files

Community

The SkyWater Open PDK

Public repository

Documentation

https://skywater-pdk--136.org.readthedocs.build

PDK Library and files

https://github.com/google/skywater-pdk

Community

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Public repository

Documentation

https://skywater-pdk--136.org.readthedocs.build

PDK Library and files

https://github.com/google/skywater-pdk

Community

slack

https://join.skywater.tools

Open-Source EDA Tools

Open-Source EDA Tools

open_pdks

http://opencircuitdesign.com/open_pdks
https://github.com/RTimothyEdwards/open_pdks

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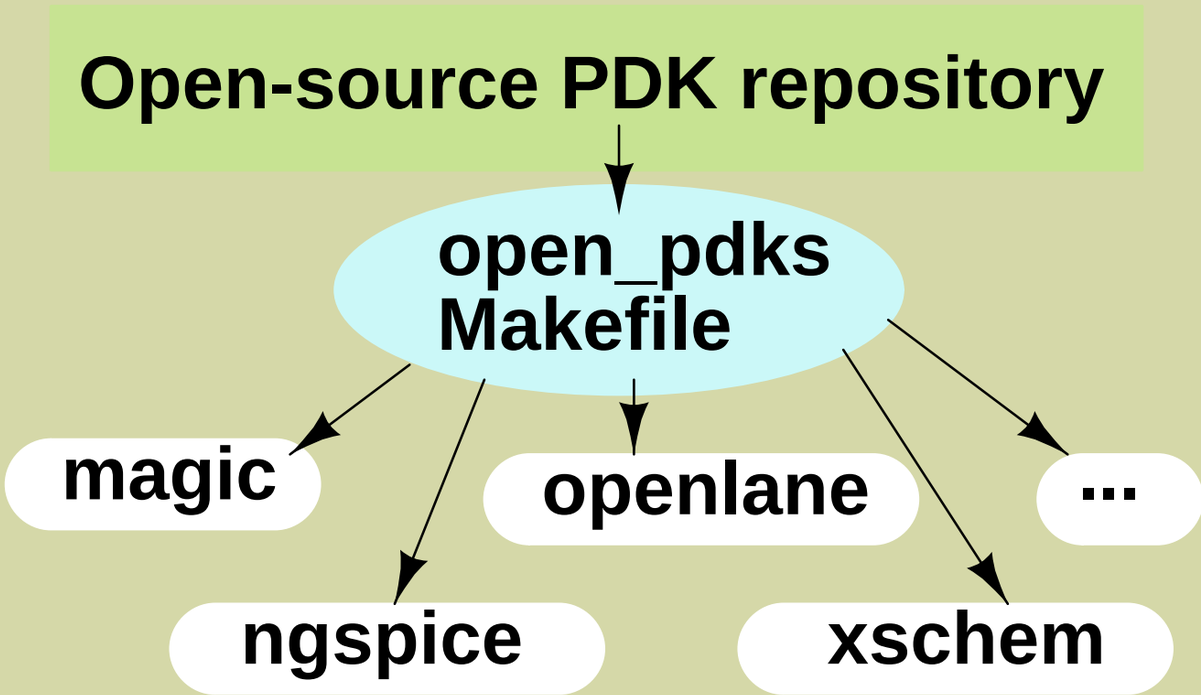


Open-Source EDA Tools

open_pdks

Steps to installing the SKY130 PDK

1. Clone the repository
   "git clone https://github.com/RTimothyEdwards/open_pdks"

2. Run "cd open_pdks"

3. Run "configure --enable-sky130-pdk"

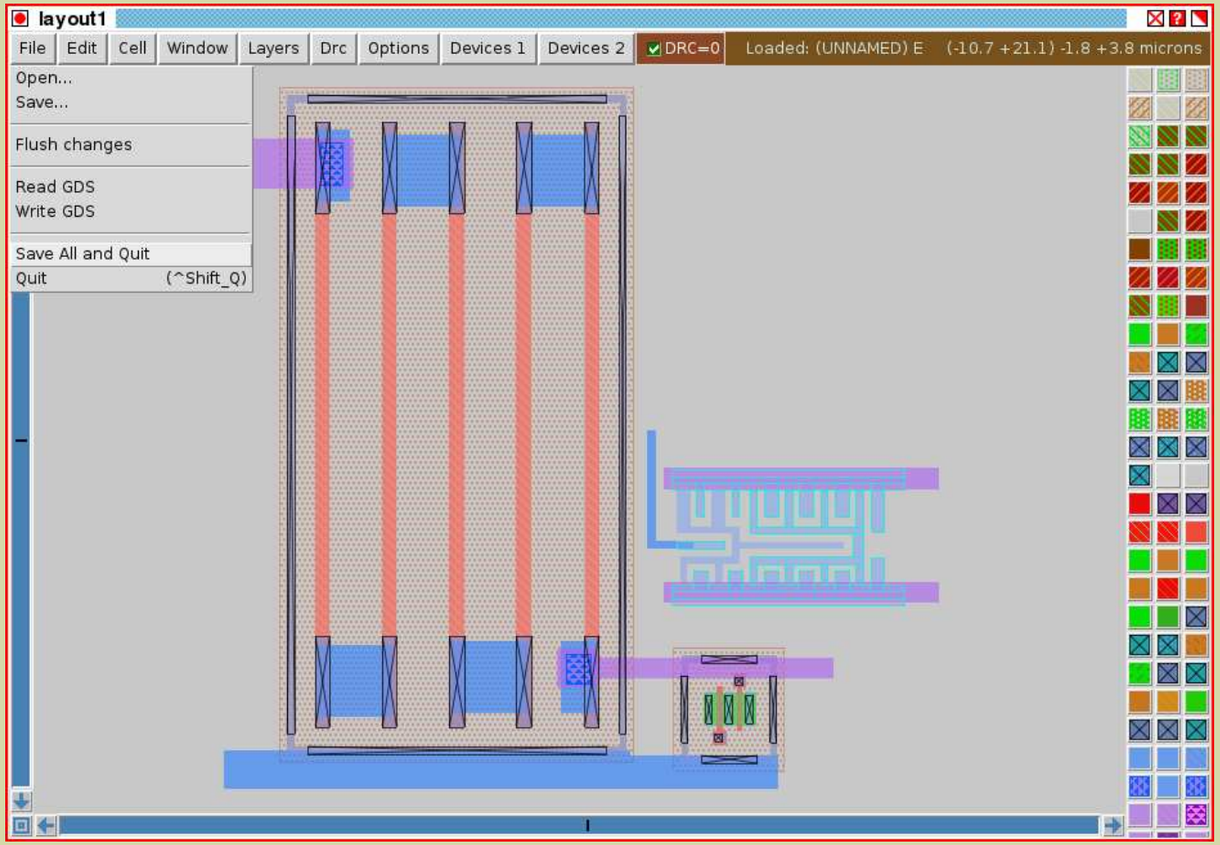
4. Run "make"

5. Run "sudo make install"

Open-Source EDA Tools

Tools Currently Supported by Open_PDKs

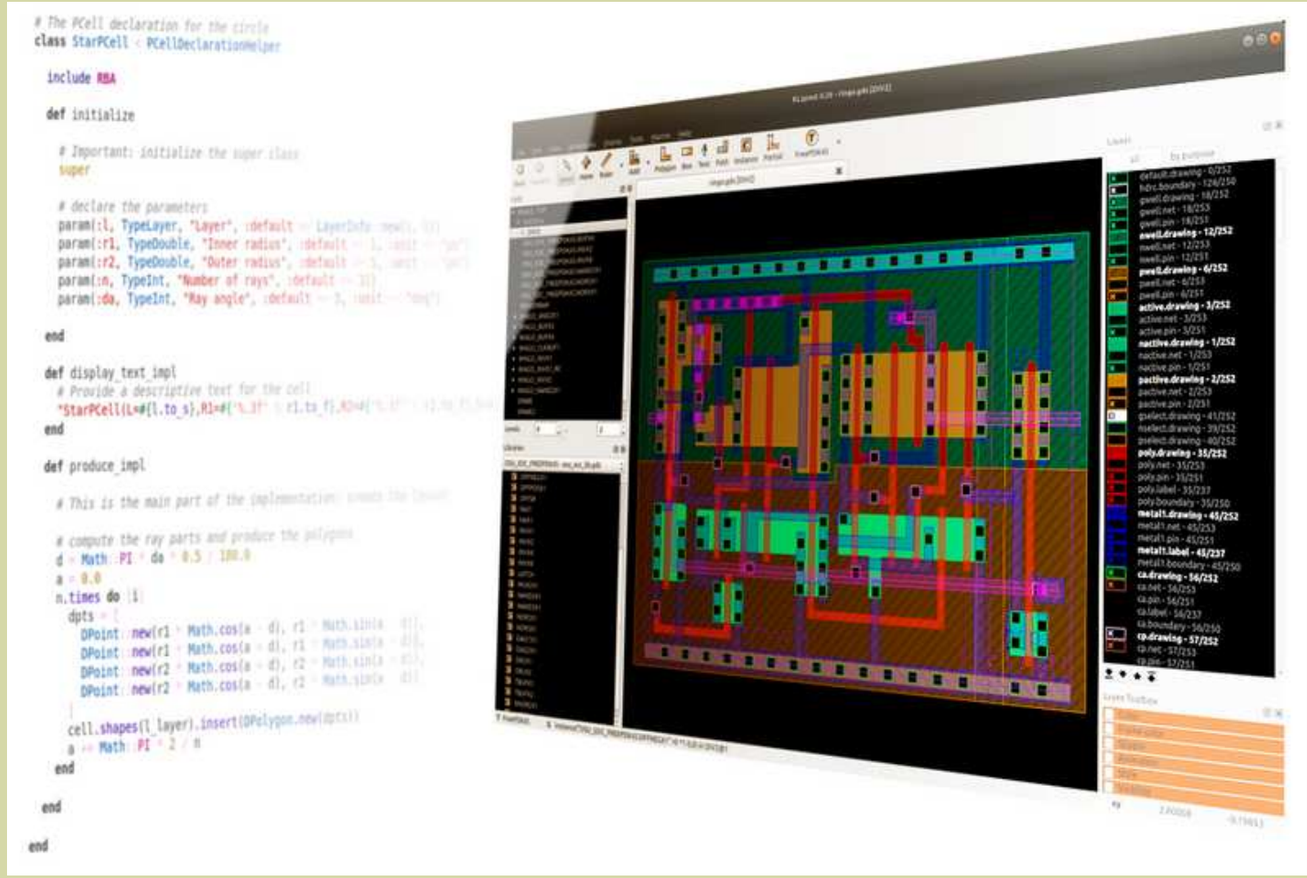
Magic http://opencircuitdesign.com/magic



Open-Source EDA Tools

Tools Currently Supported by Open_PDKs

Klayout https://www.klayout.de

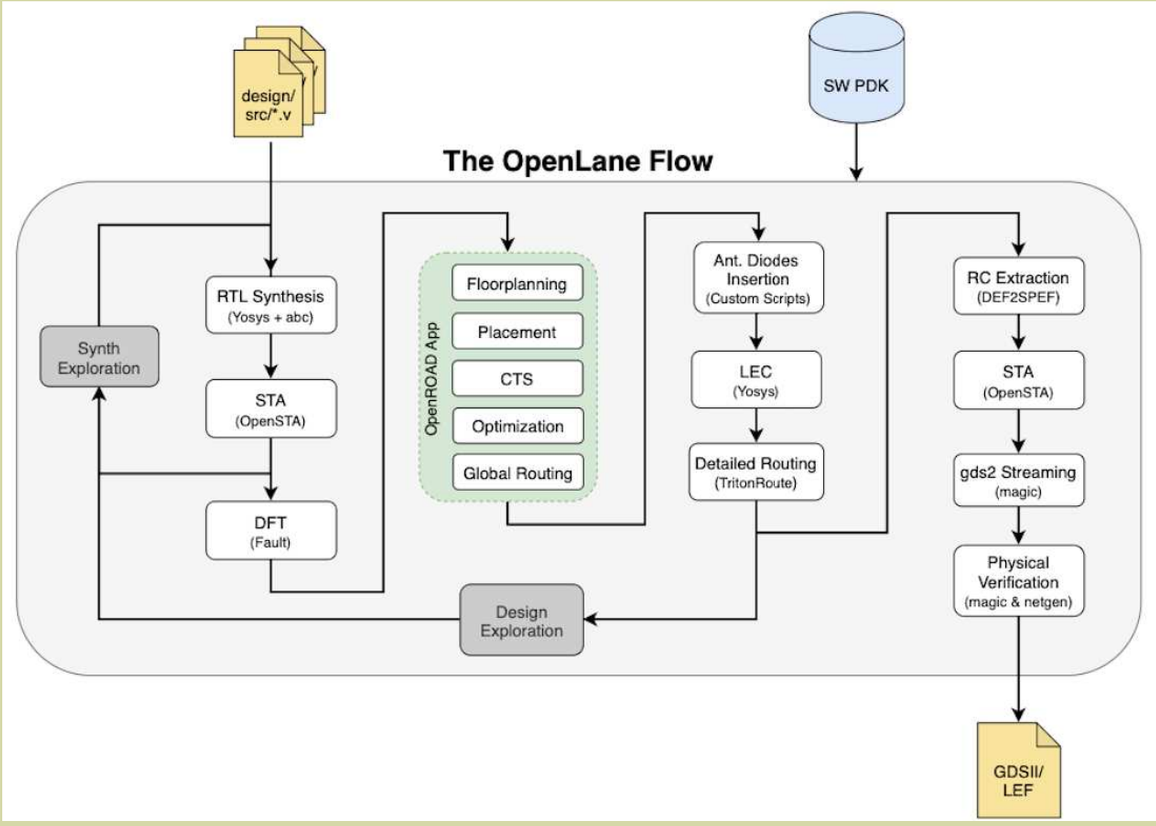


Open-Source EDA Tools

Tools Currently Supported by Open_PDKs

Openlane

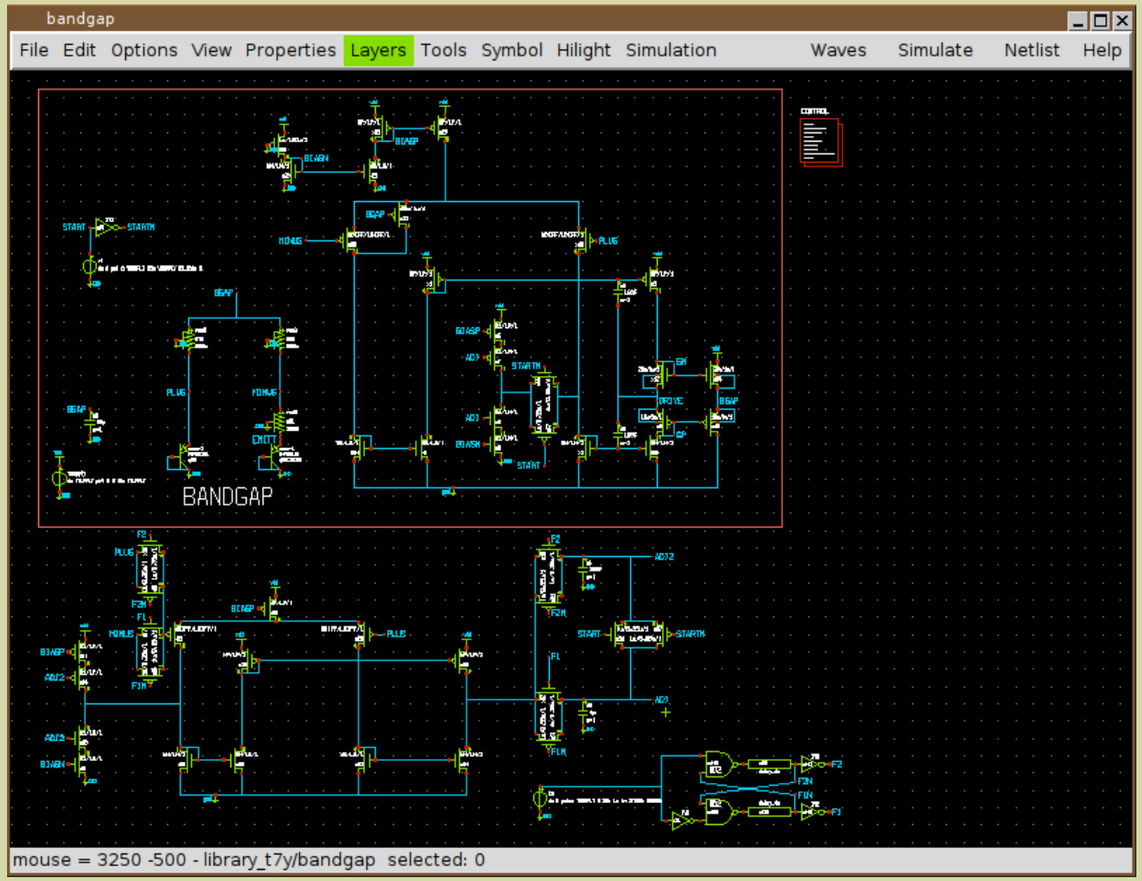
https://github.com/The-OpenROAD-Project/OpenLane



Open-Source EDA Tools

Tools Currently Supported by Open_PDKs

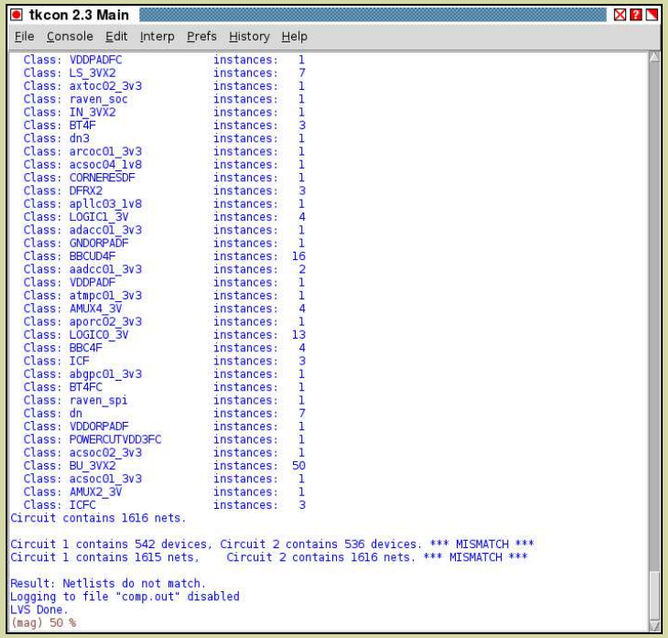
Xschem https://github.com/StefanSchippers/xschem

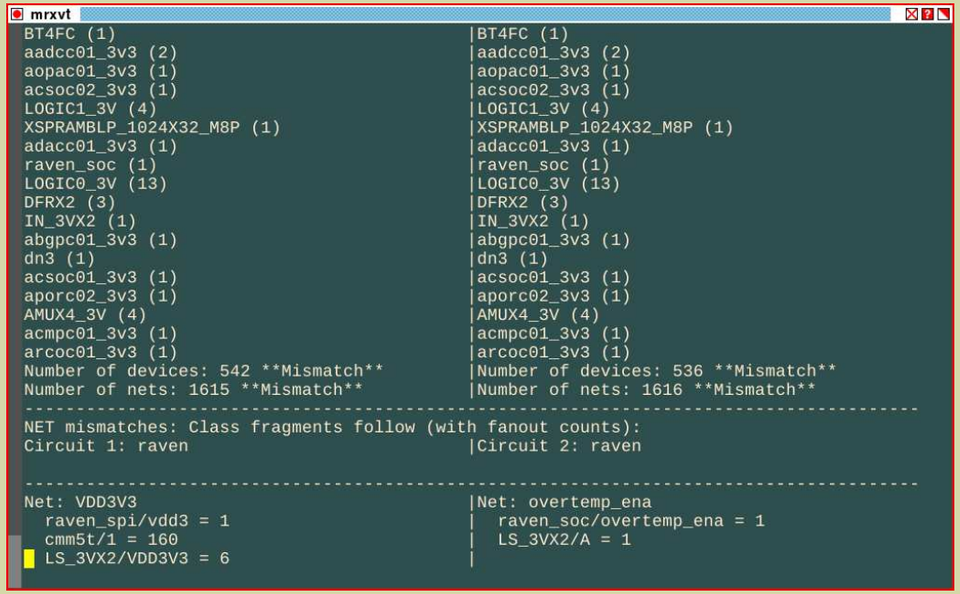


Open-Source EDA Tools

Tools Currently Supported by Open_PDKs

Netgen http://opencircuitdesign.com/netgen

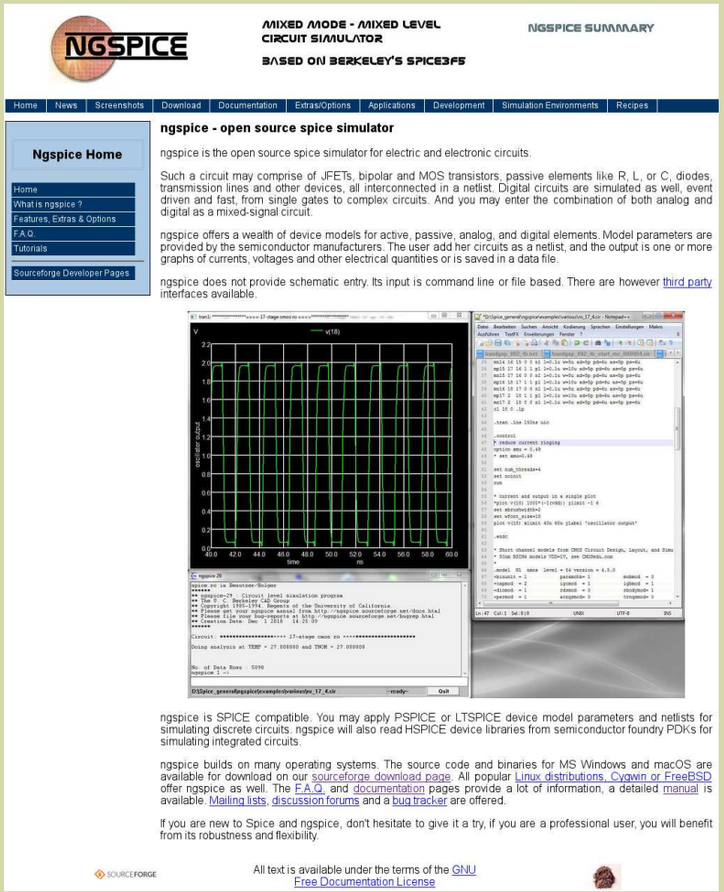




Open-Source EDA Tools

Tools Currently Supported by Open_PDKs

Ngspice https://ngspice.sourceforge.net



Open-Source EDA Tools

Tools Currently Supported by Open_PDKs

iverilog

https://iverilog.icarus.com

qflow

http://opencircuitdesign.com/qflow

IRSIM

http://opencircuitdesign.com/irsim

xcircuit

http://opencircuitdesign.com/xcircuit

xyce

https://xyce.sandia.gov

fun fact: These slides were drawn with xcircuit!

Open-Source EDA Tools

SkyWater SKY130 Libraries

1. **Digital standard cells**
   - sky130_fd_sc_hd
   - sky130_fd_sc_hdll
   - sky130_fd_sc_hs
   - sky130_fd_sc_ms
   - sky130_fd_sc_ls
   - sky130_fd_sc_lp
   - sky130_fd_sc_hvl

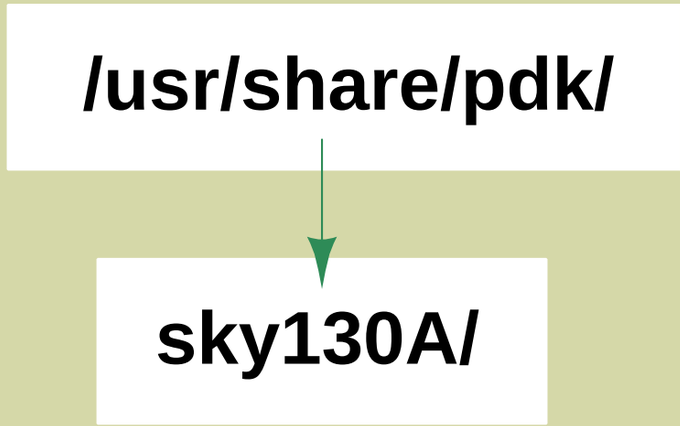
2. **Primitive devices / analog**
   - sky130_fd_pr

3. **I/O cells**
   - sky130_fd_io

4. **3rd-party libraries**
   - sky130_ml_xx_hd
   - sky130_sram_macros

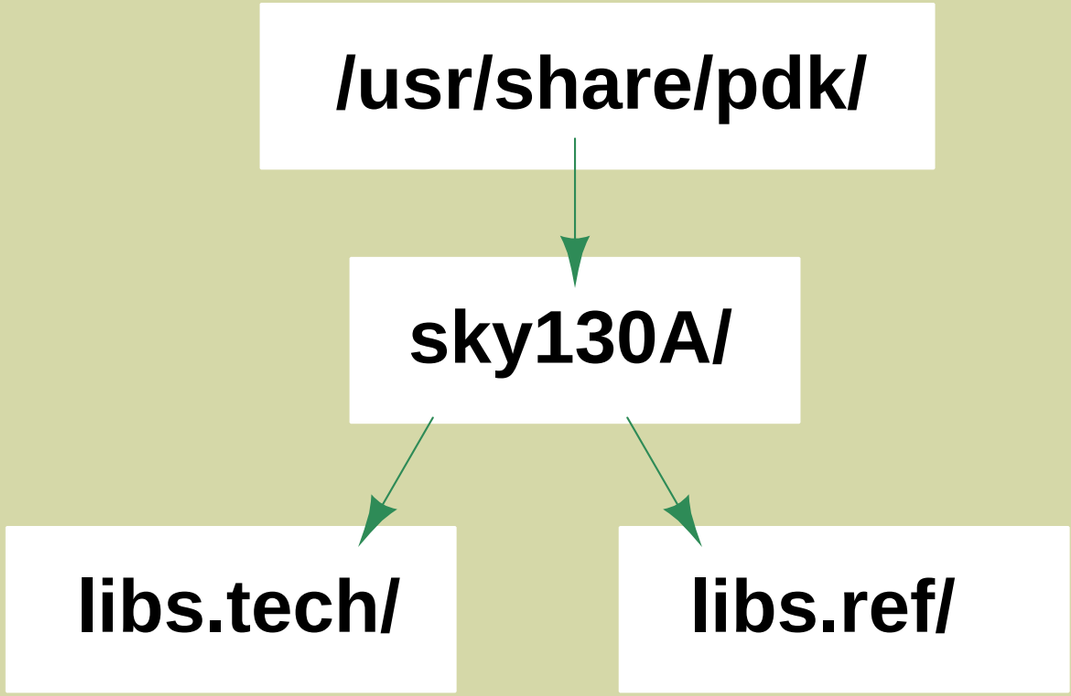
Open-Source EDA Tools

PDK (e.g., SKY130) Installed Filesystem Structure



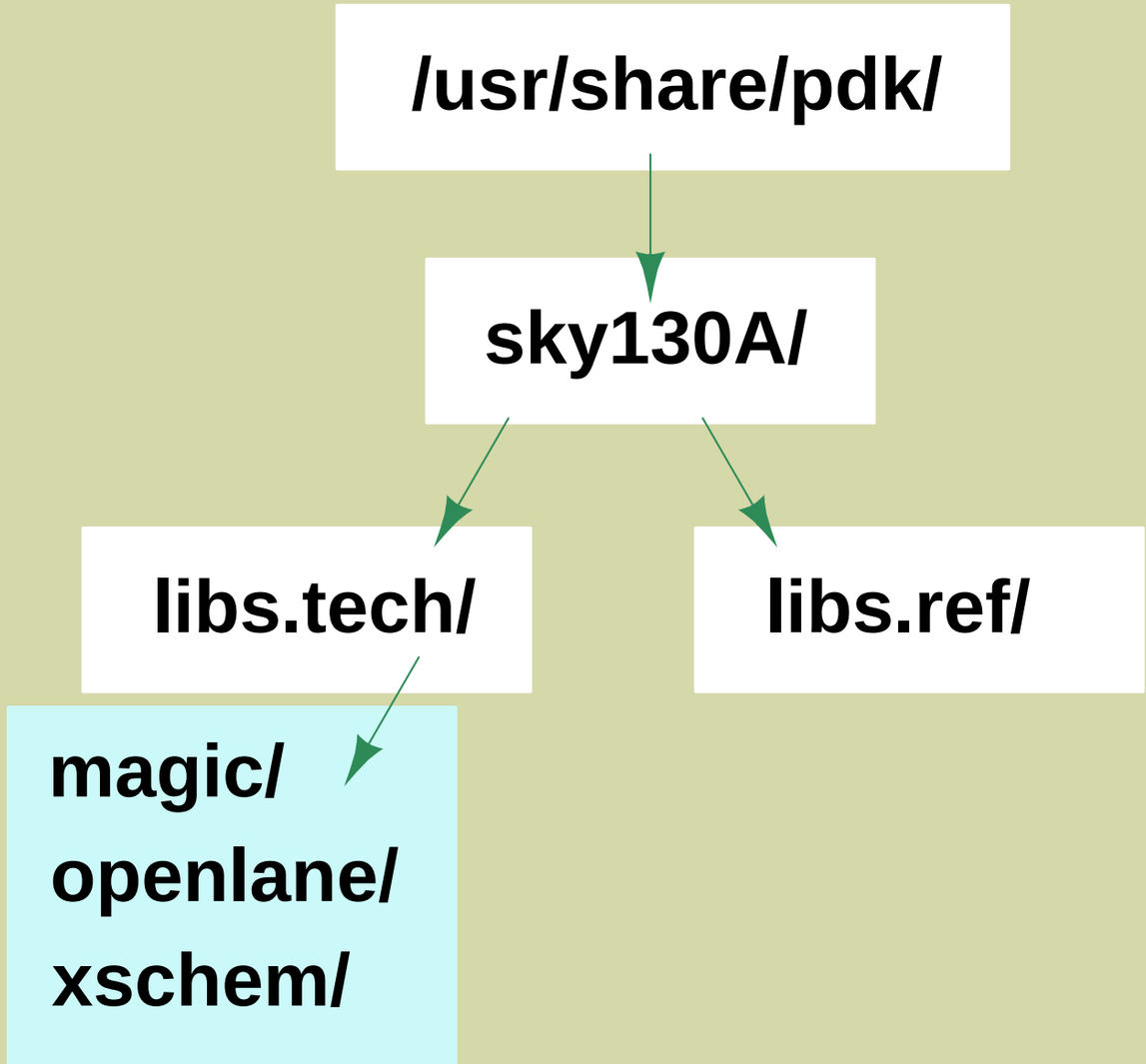
Open-Source EDA Tools

SkyWater SKY130 Installed Filesystem Structure



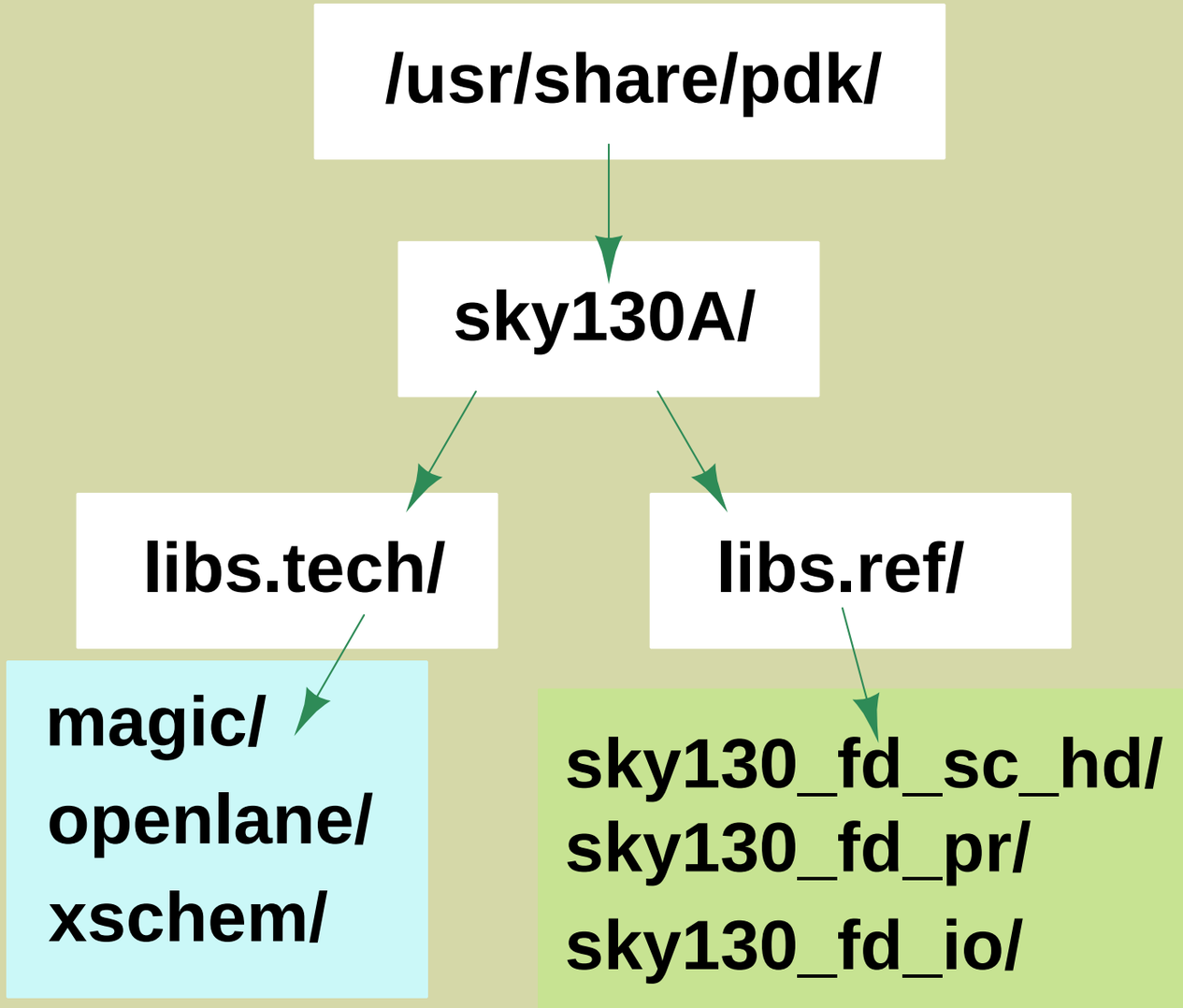
Open-Source EDA Tools

SkyWater SKY130 Installed Filesystem Structure



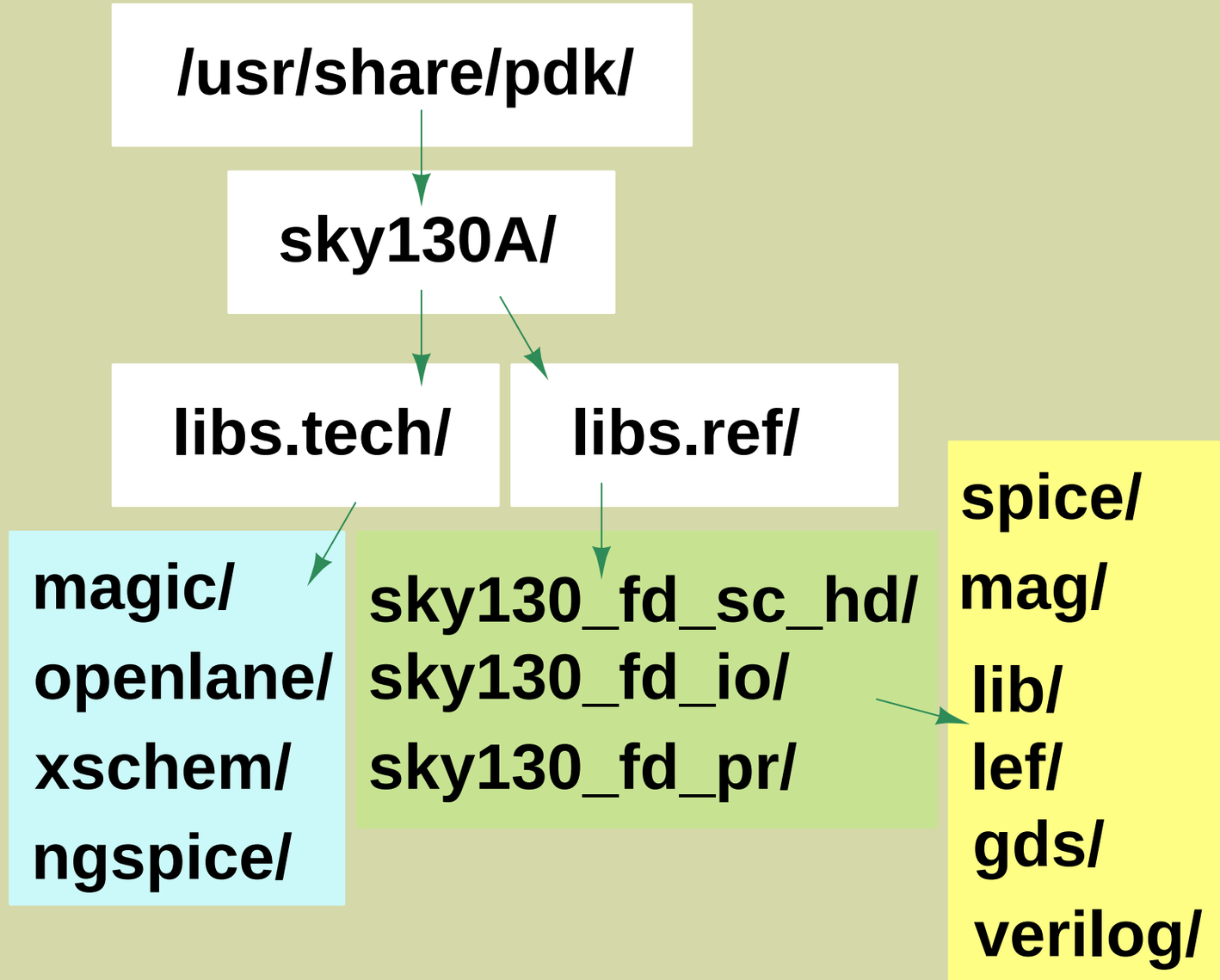
Open-Source EDA Tools

SkyWater SKY130 Installed Filesystem Structure



Open-Source EDA Tools

SkyWater SKY130 Installed Filesystem Structure



Open-Source EDA Tools

Open PDKs Project Filesystem Structure

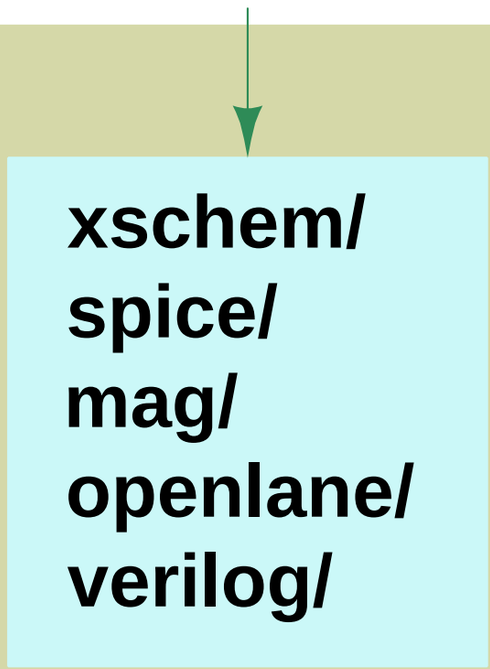
project_root/ e.g., "**`my_sky130_project`**"

Open-Source EDA Tools

Open PDKs Project Filesystem Structure

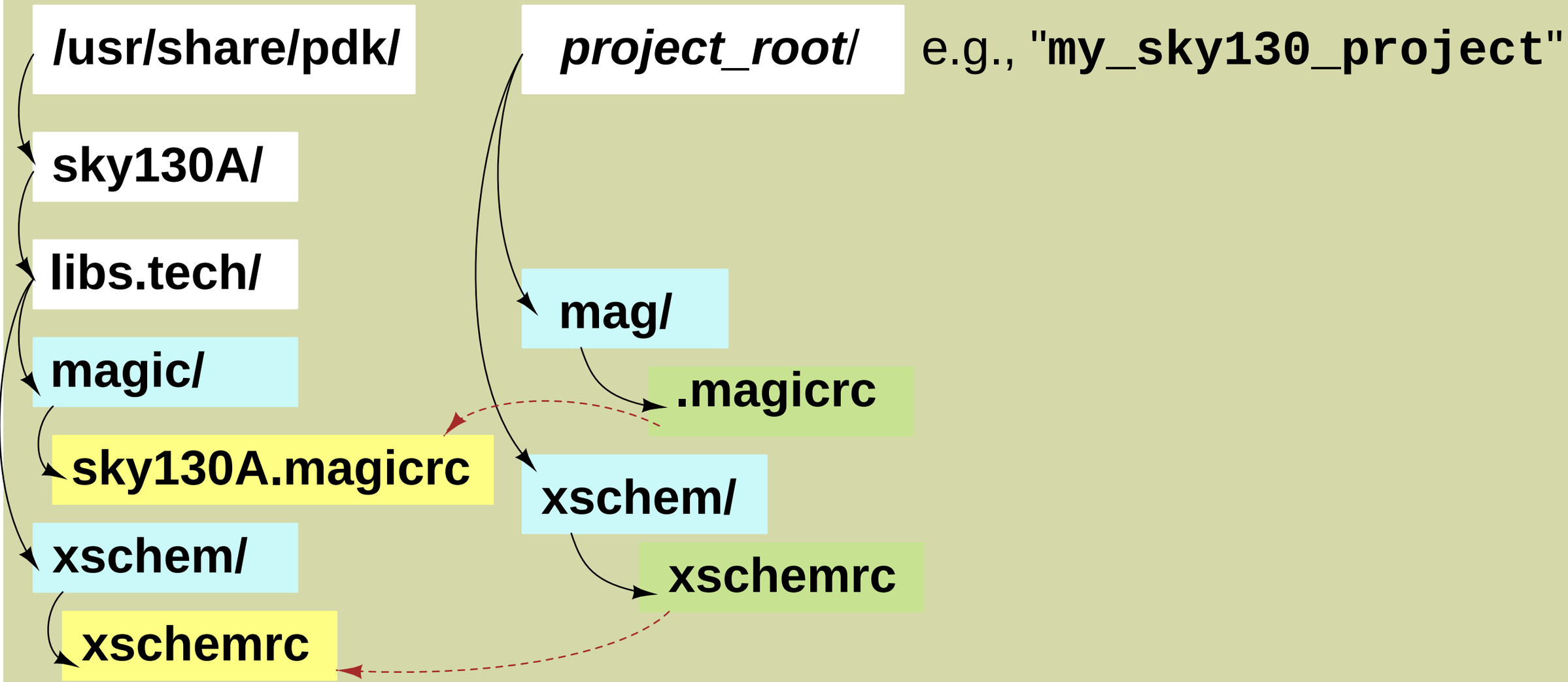
project_root/

e.g., "**`my_sky130_project`**"



Open-Source EDA Tools

Open PDKs Project Filesystem Structure



Open-Source EDA Tools

Open PDKs Project Filesystem Structure

Project Management

/usr/share/pdk/scripts/project_manager.py

(work in progress)

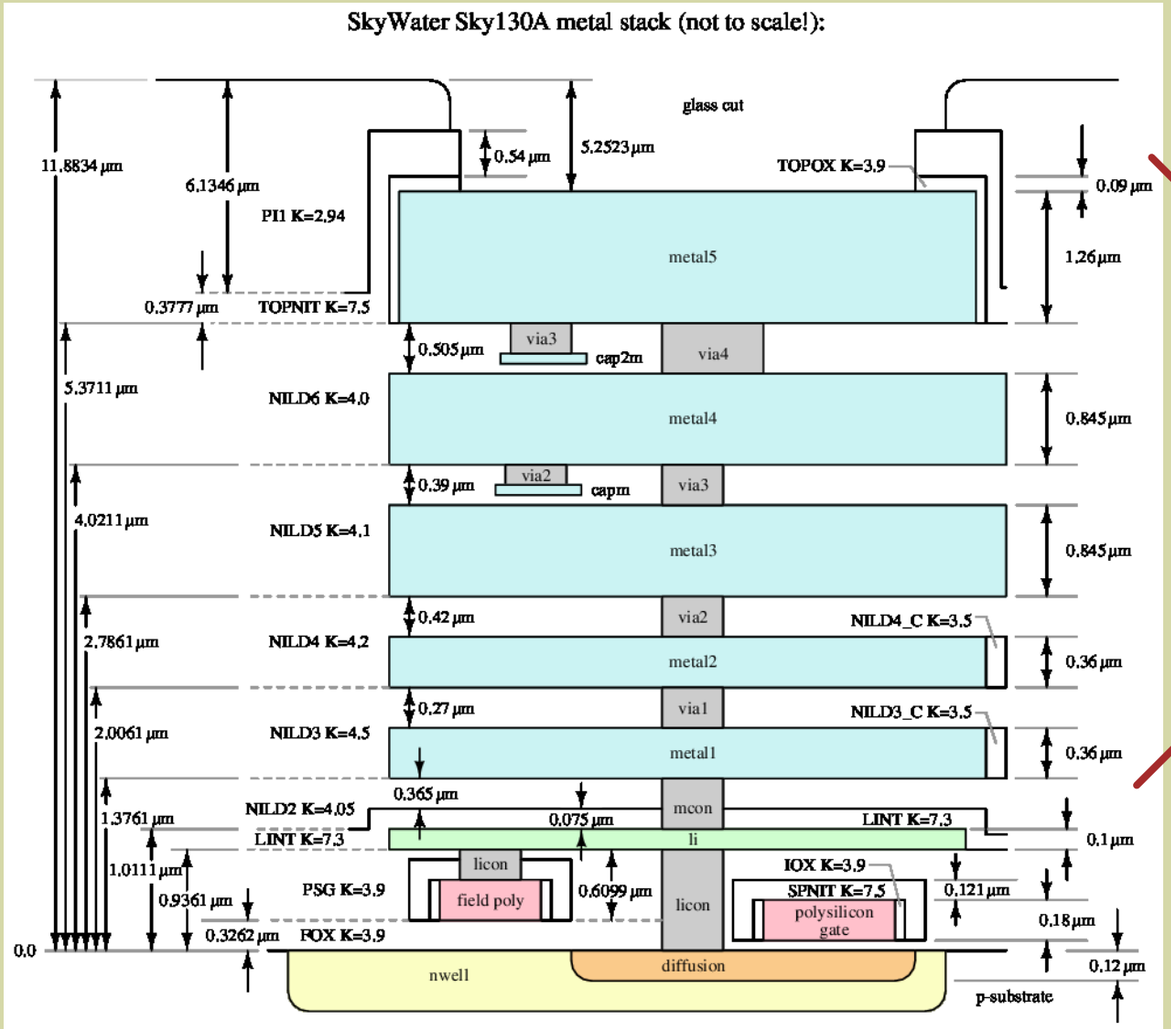
Understanding the SkyWater PDK

Layers

SKY130

Understanding the SkyWater PDK

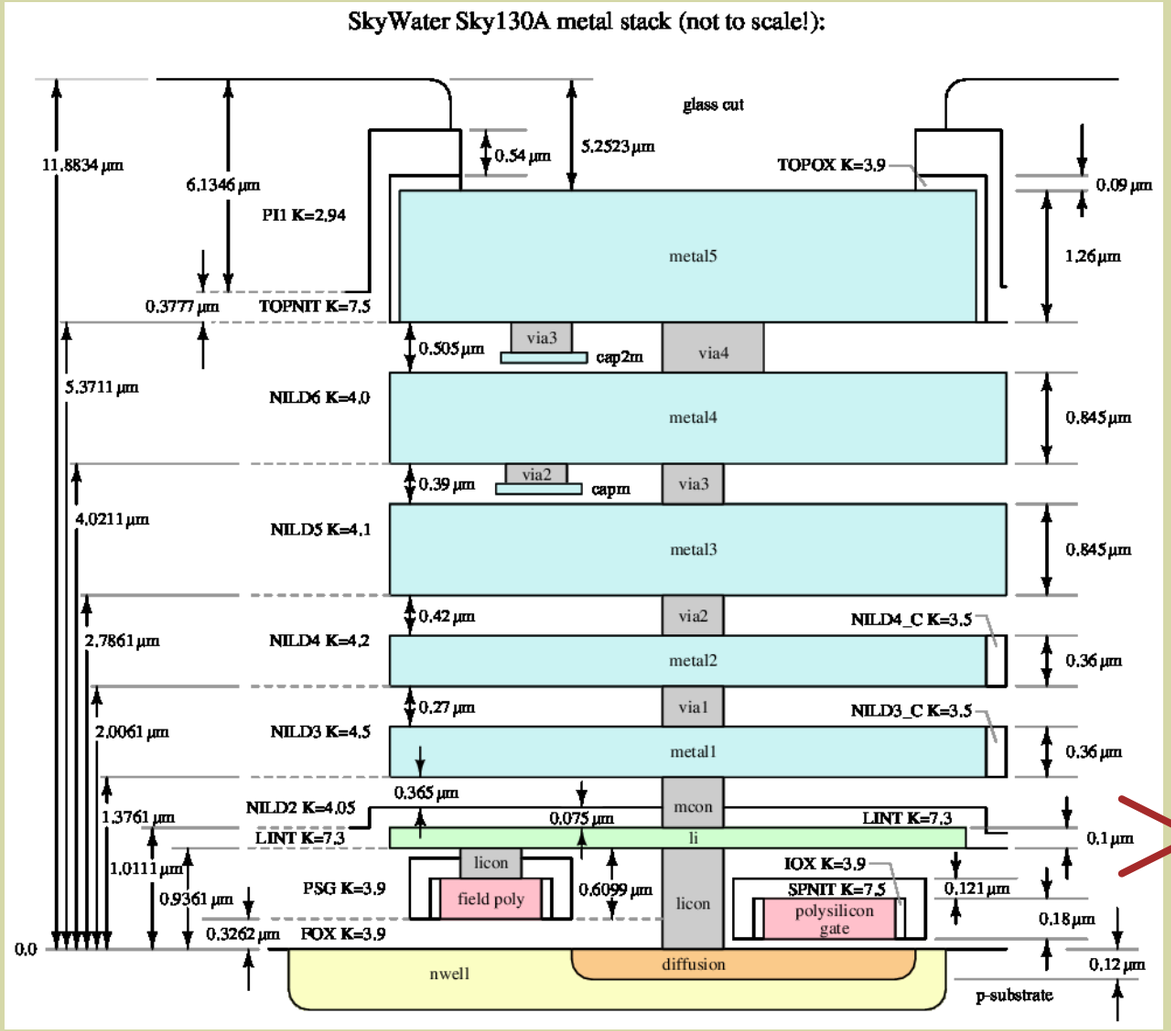
Layers



5 layers of aluminum metal

Understanding the SkyWater PDK

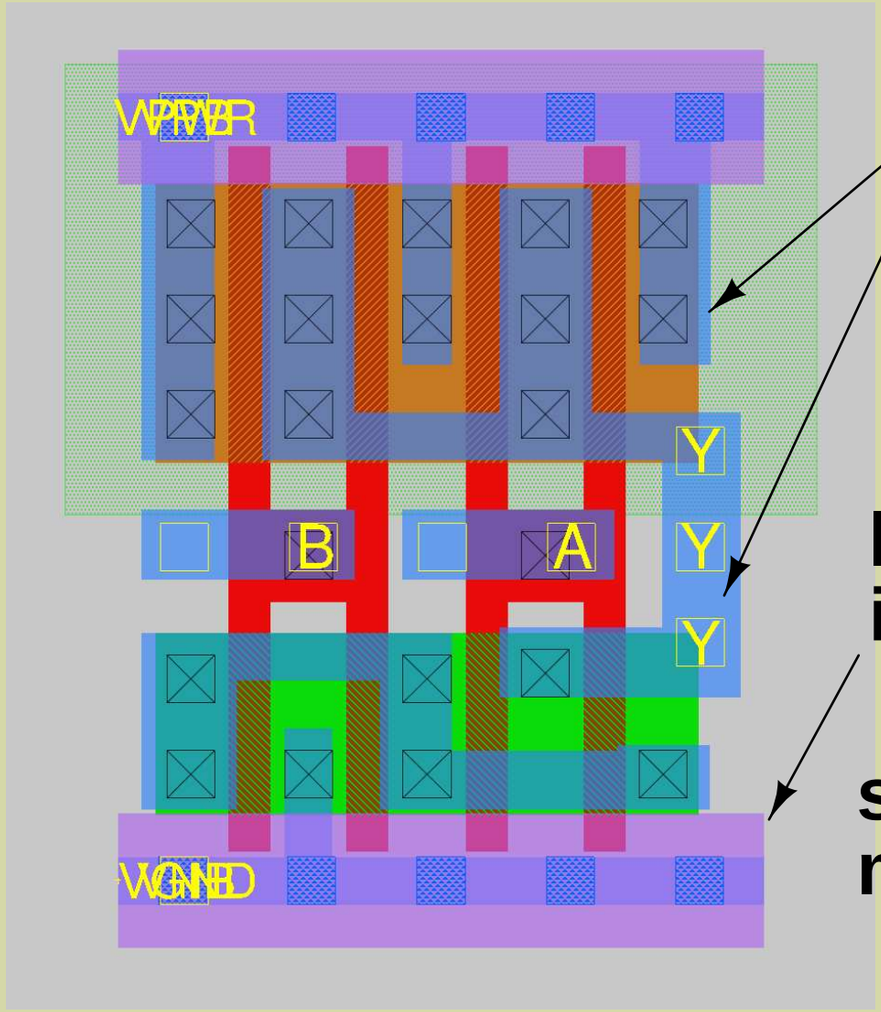
Layers



Titanium Nitride (TiN)
aka "Local interconnect"

Understanding the SkyWater PDK

sky130_fd_sc_hd__nand2_2



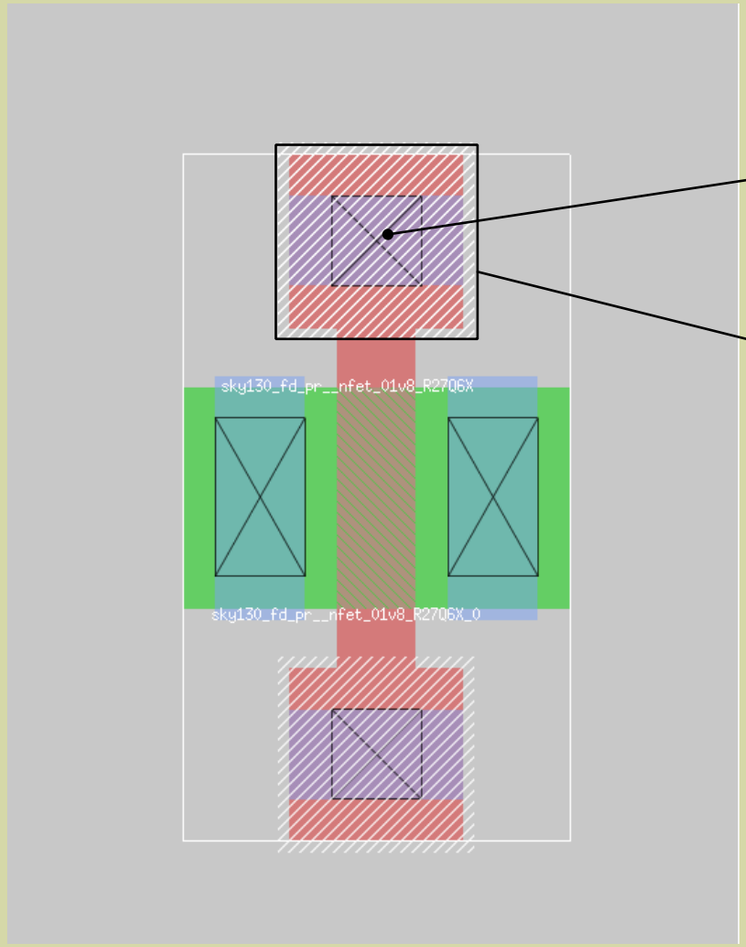
local interconnect (blue)

local interconnect (blue)

strapped with metal1 (purple)

Understanding the SkyWater PDK

Layers

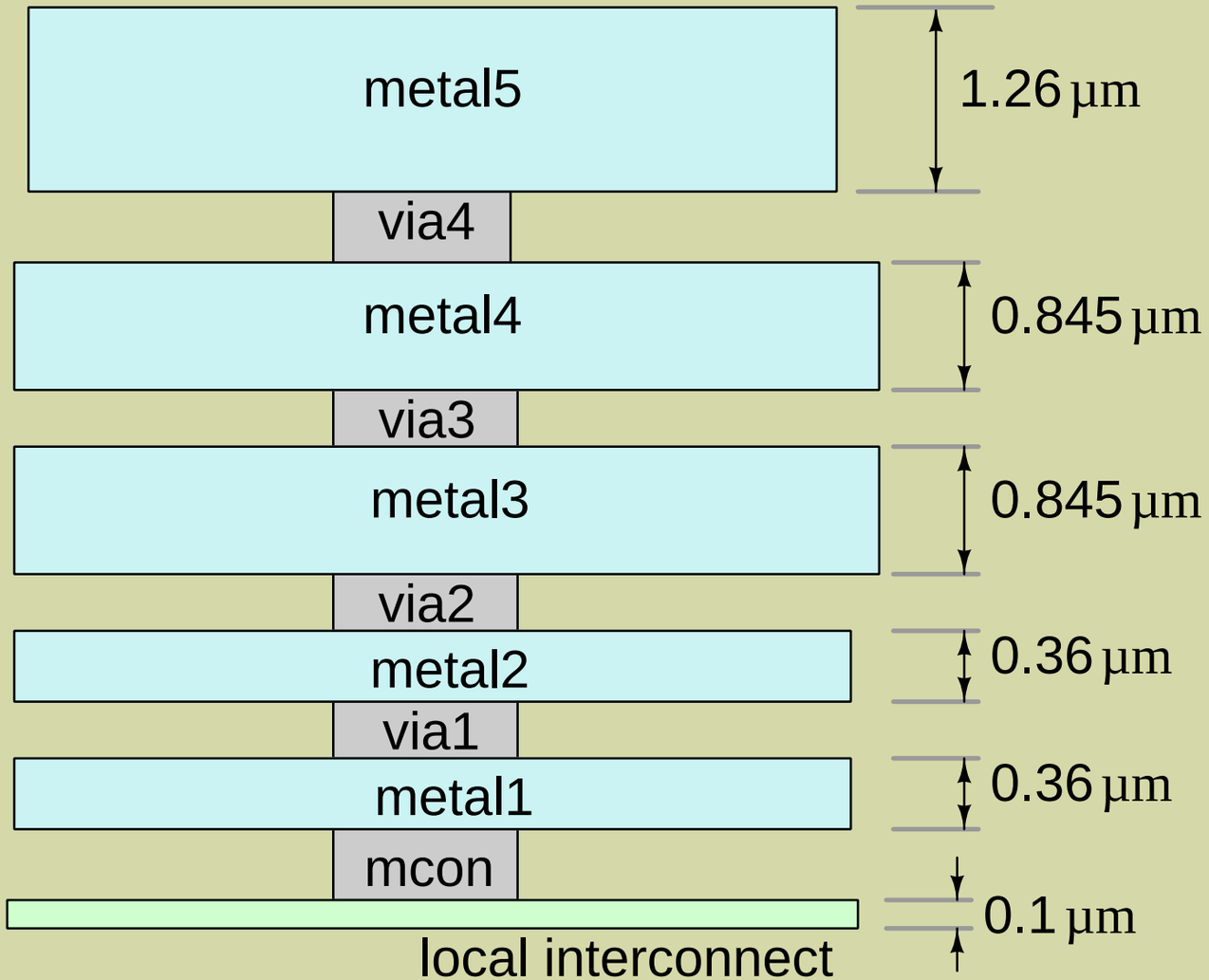


poly contact

nitride poly
cut layer
(NPC)

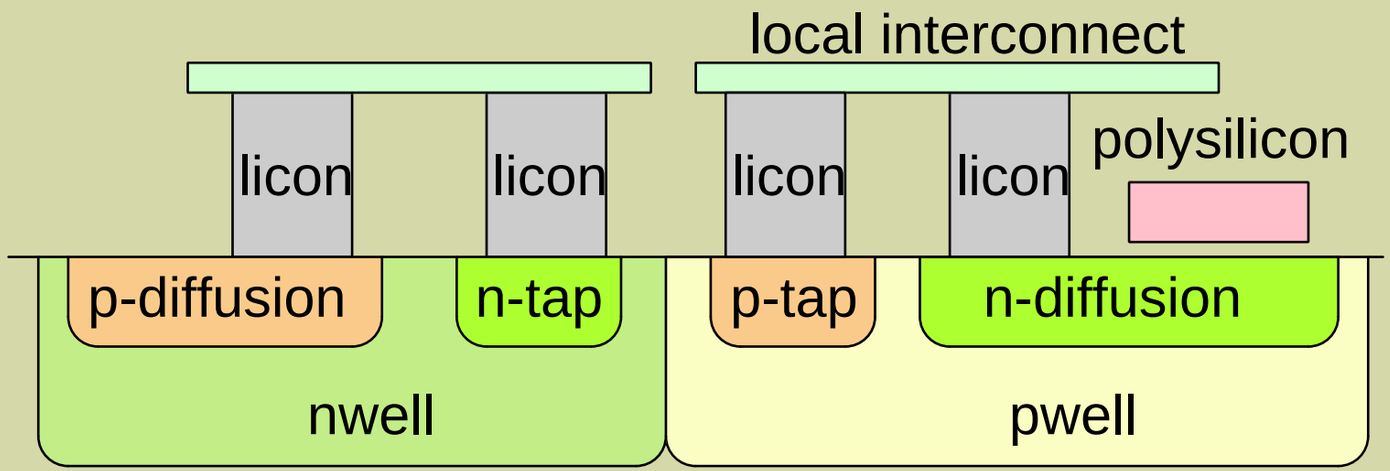
Understanding the SkyWater PDK

back-end metal stack



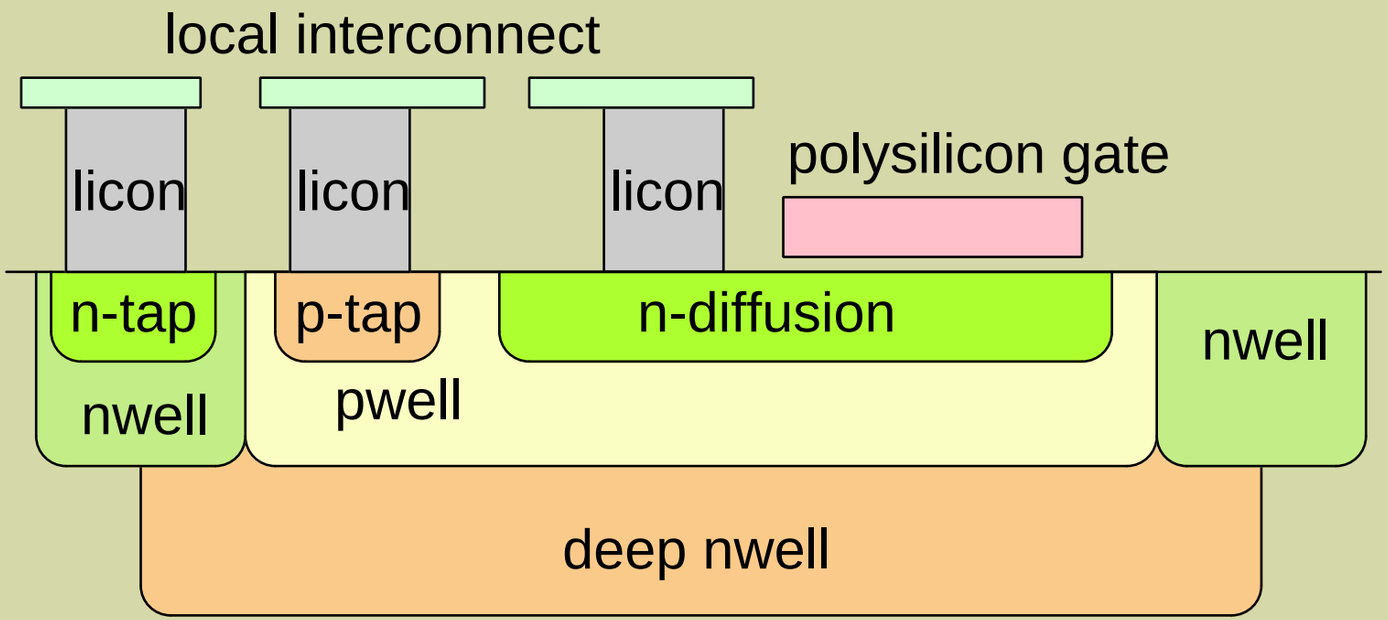
Understanding the SkyWater PDK

front-end layers



Understanding the SkyWater PDK

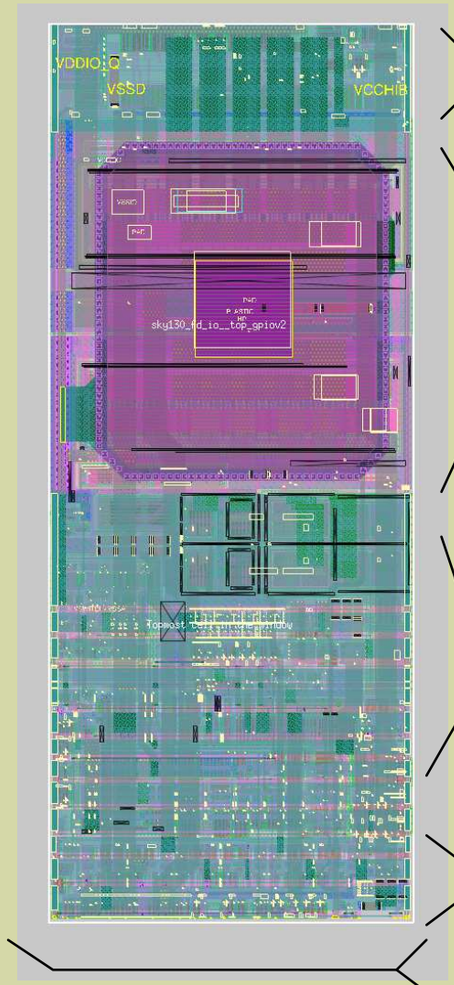
front-end layers



Understanding the SkyWater PDK

high voltage layer (HVI)

GPIO pad



3.3V busses

3.3V on pad

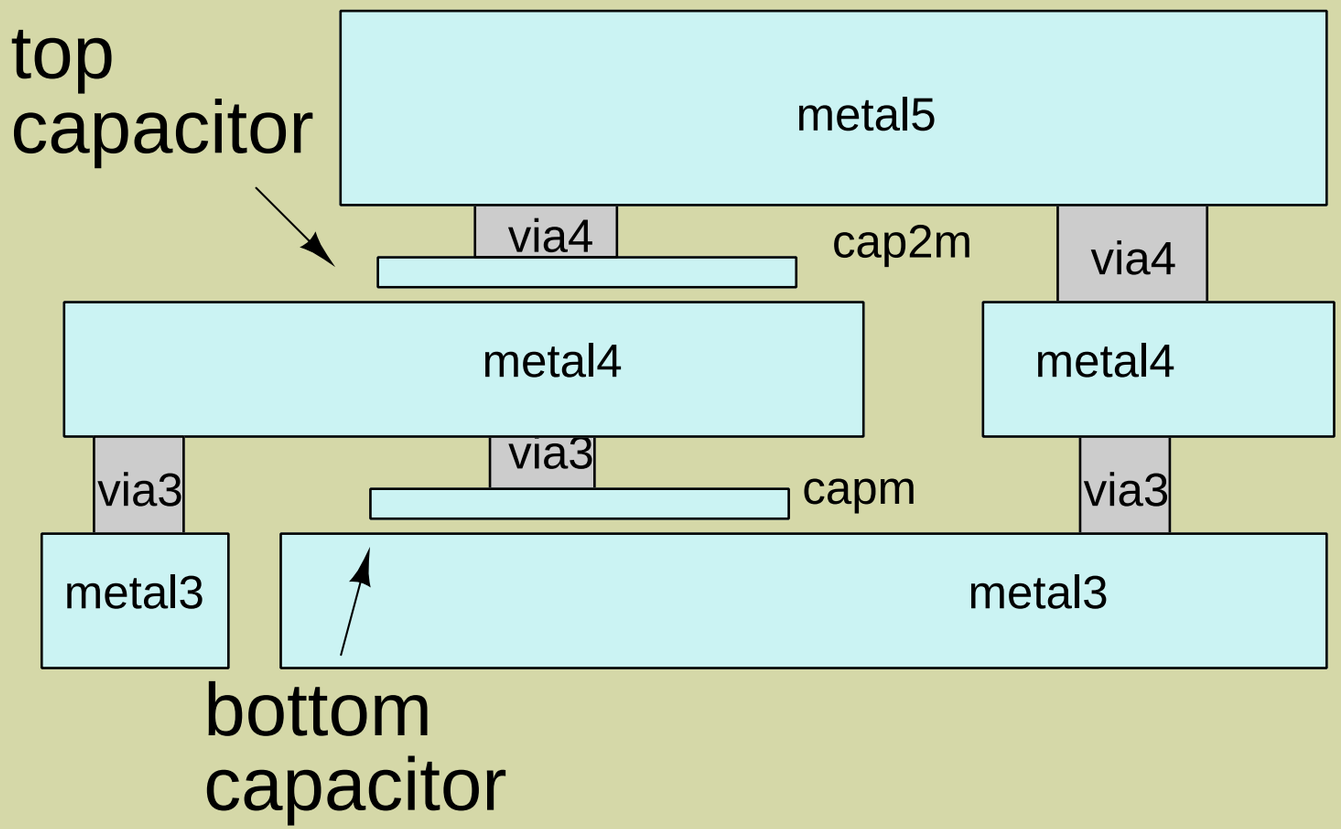
3.3V busses

1.8V busses

1.8V core signals

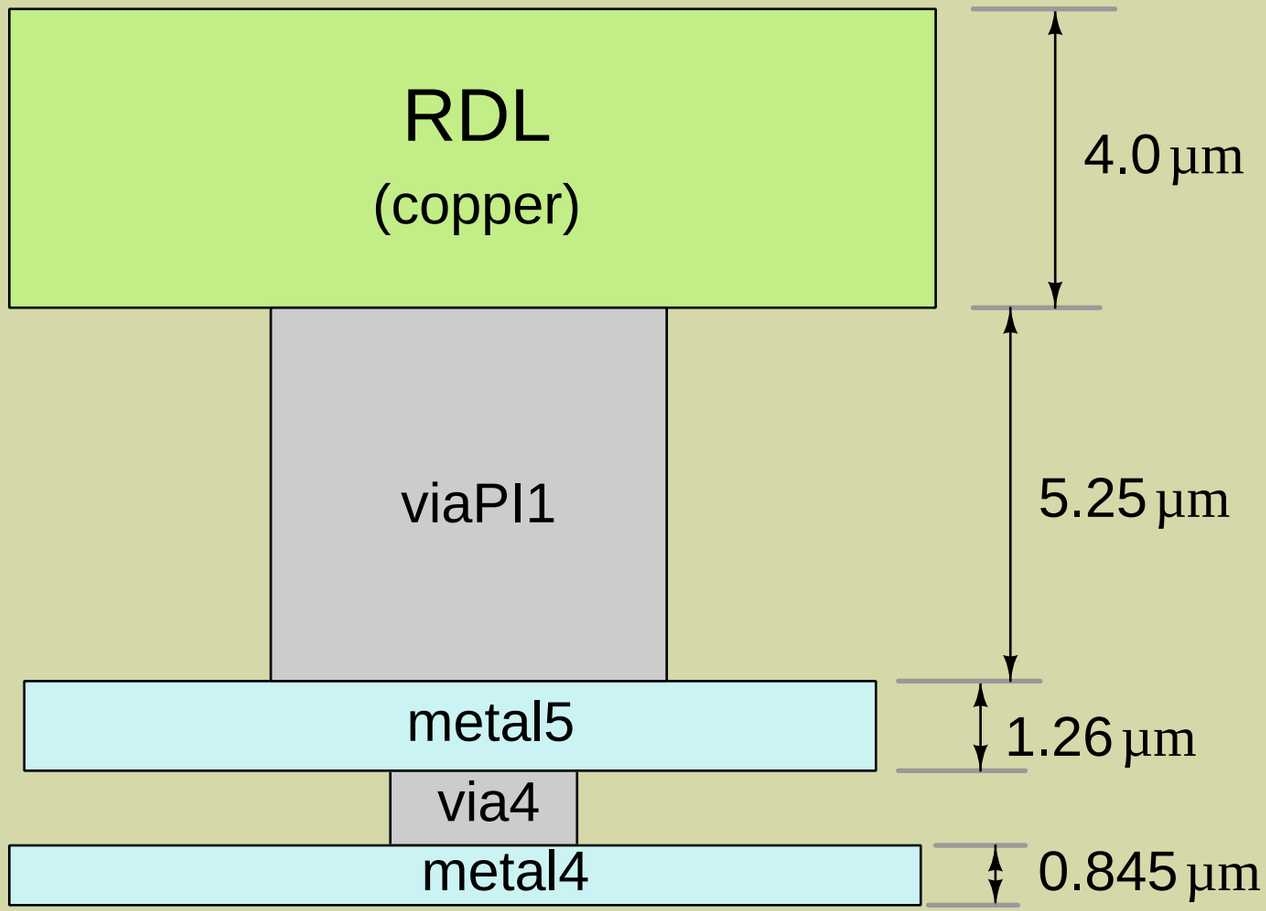
Understanding the SkyWater PDK

MiM cap layers



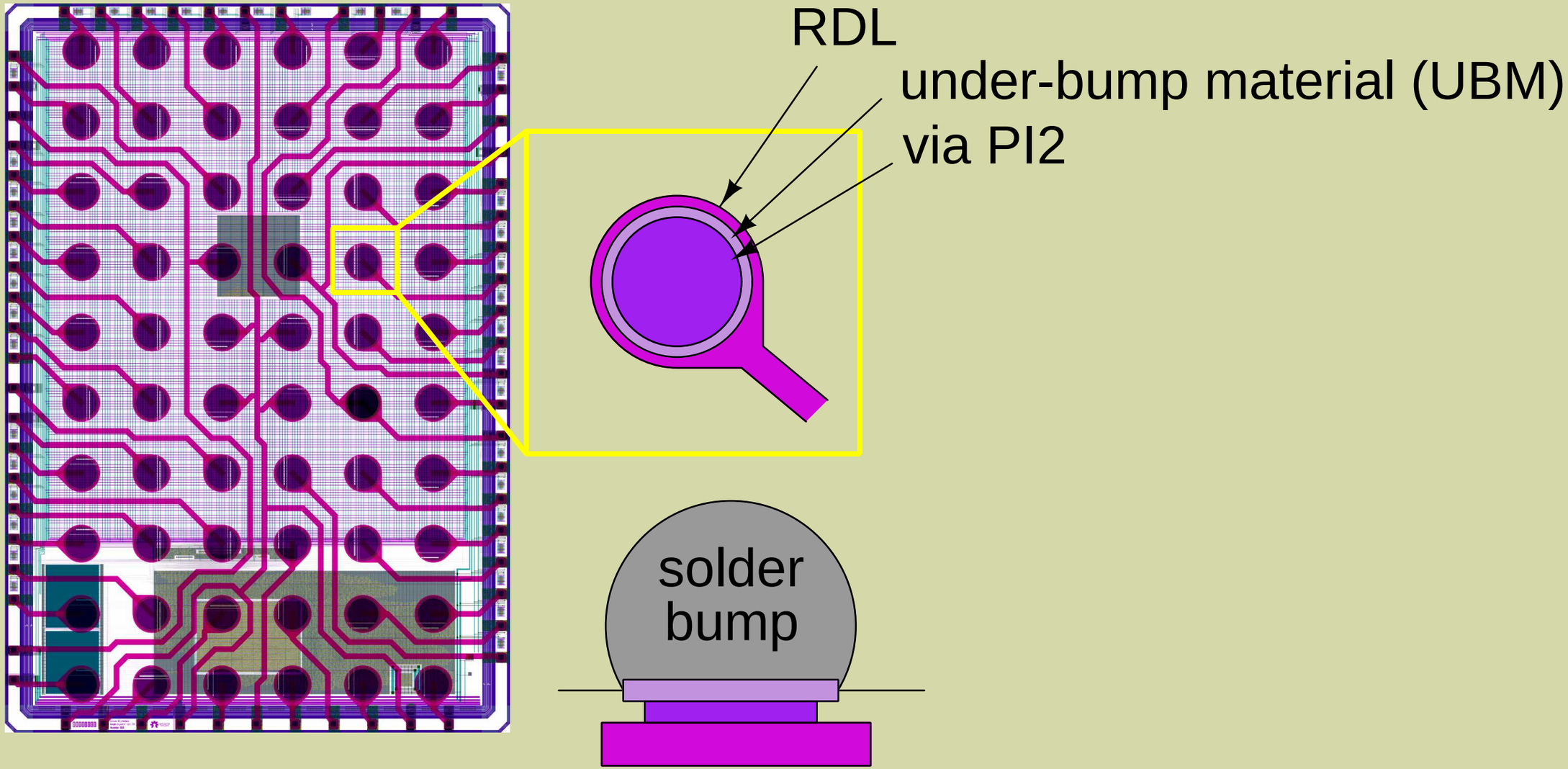
Understanding the SkyWater PDK

Redistribution layer



Understanding the SkyWater PDK

Redistribution layer



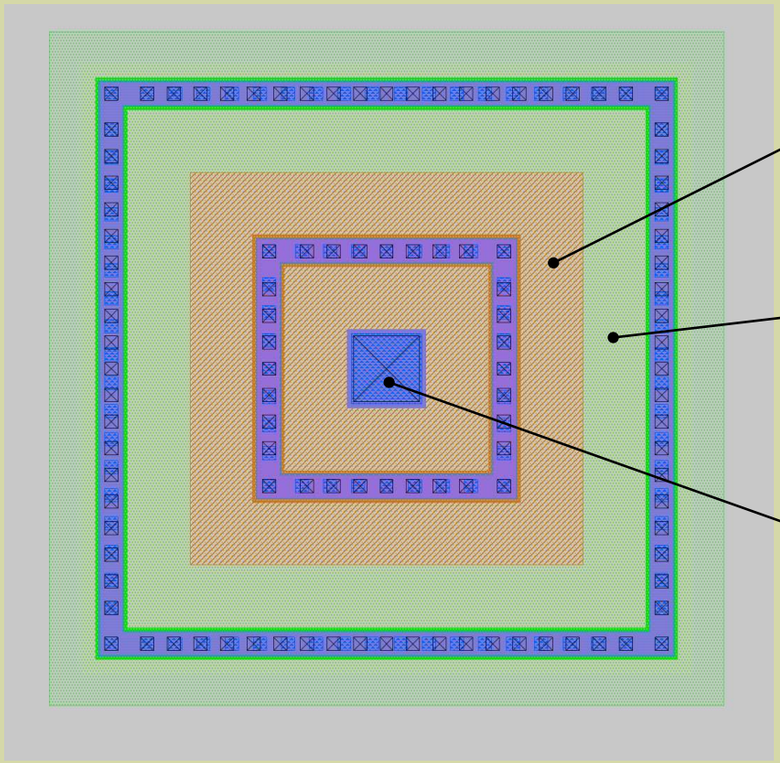
Understanding the SkyWater PDK

Devices

Understanding the SkyWater PDK

Devices

bipolar NPN



base
pwell in
deep nwell

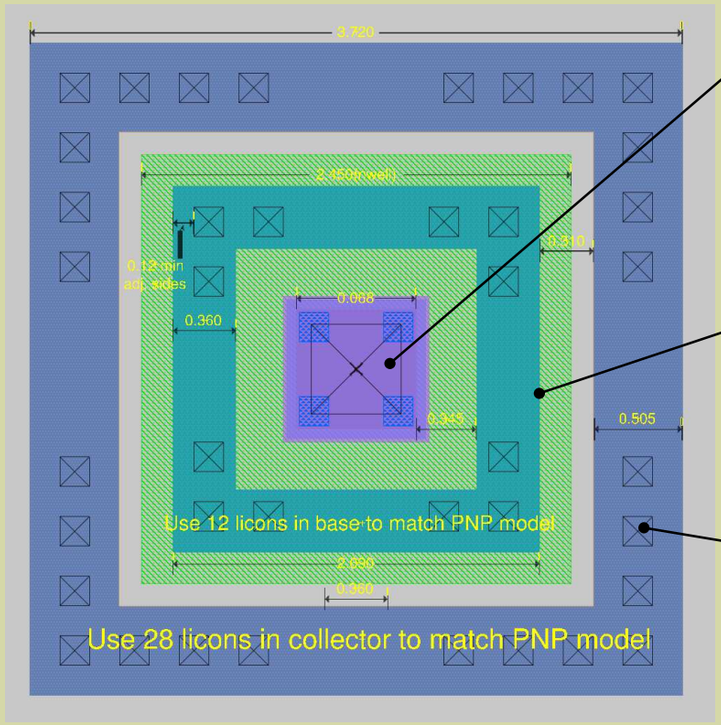
collector
n well

emitter
n diffusion

Understanding the SkyWater PDK

Devices

bipolar PNP



emitter

p diffusion

base

n well

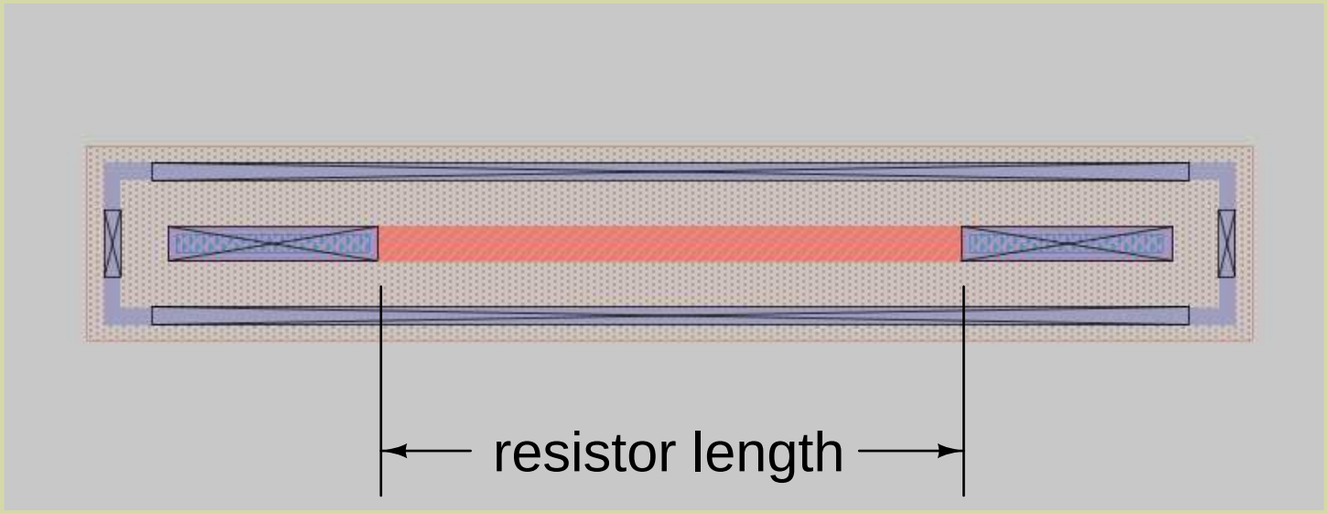
collector

p substrate

Understanding the SkyWater PDK

Devices

polysilicon resistors



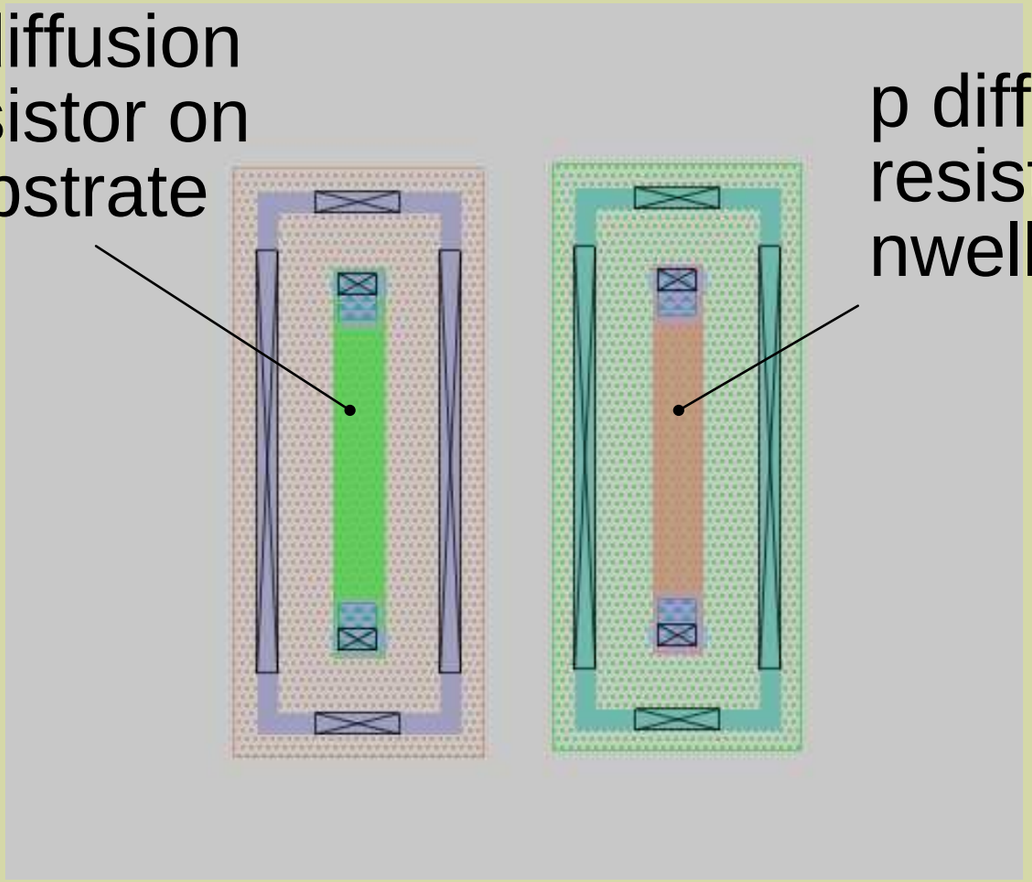
Understanding the SkyWater PDK

Devices

diffusion resistors

n diffusion resistor on substrate

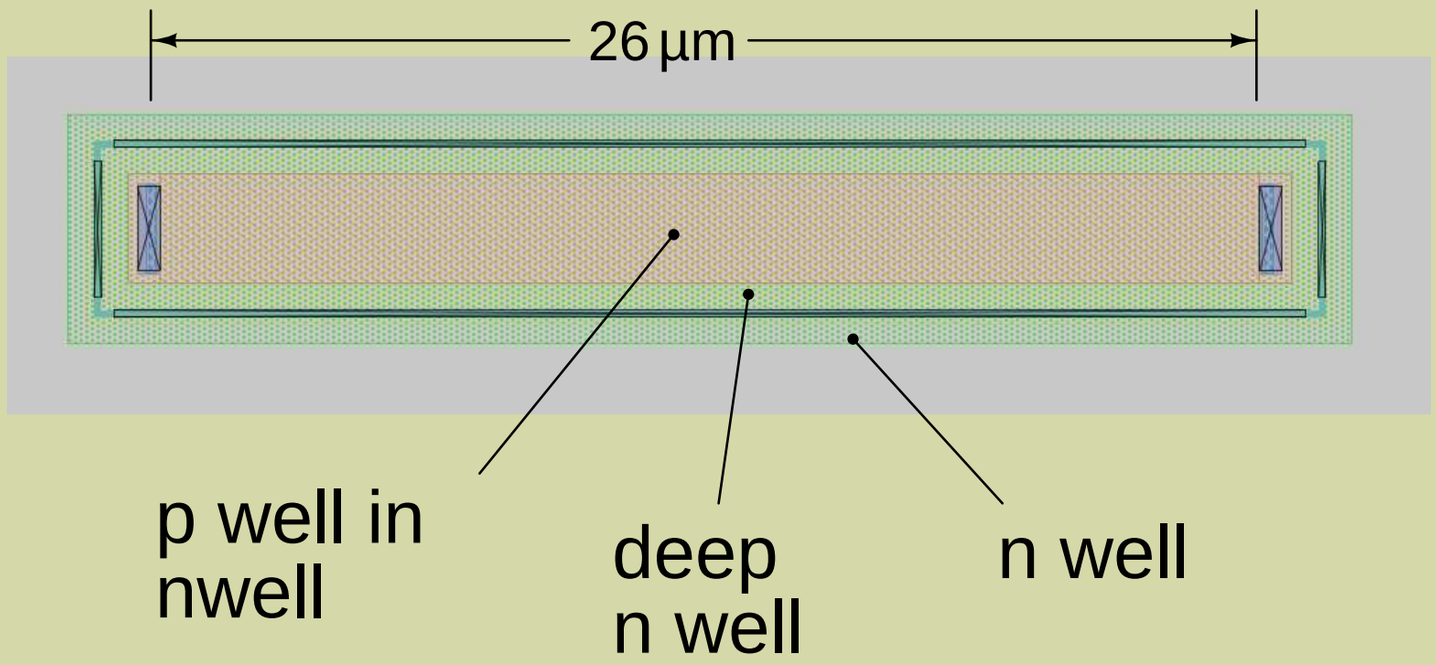
p diffusion resistor in nwell



Understanding the SkyWater PDK

Devices

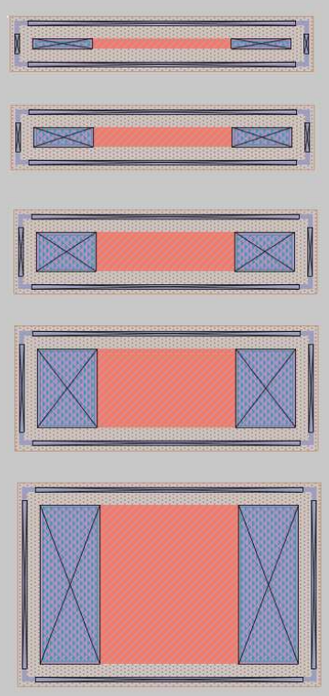
pwell resistor



Understanding the SkyWater PDK

Devices

Discrete widths



width = 0.35 µm

width = 0.69 µm

width = 1.41 µm

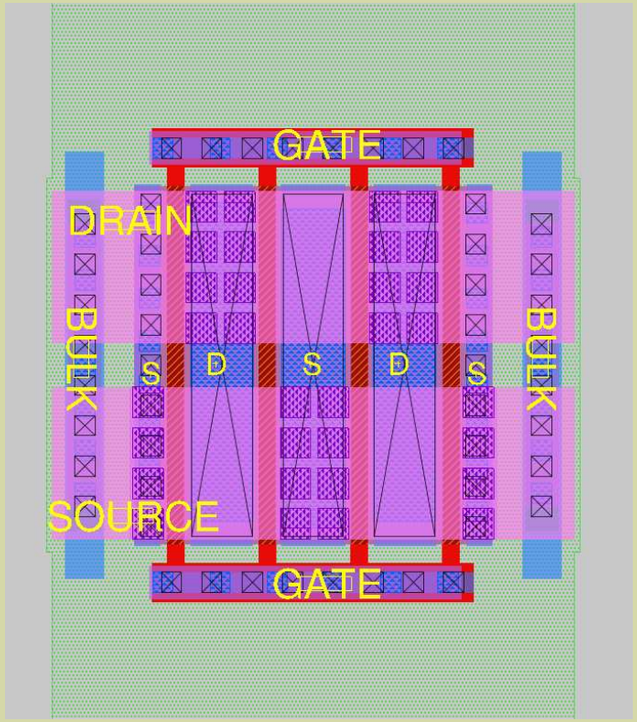
width = 2.85 µm

width = 5.73 µm

Understanding the SkyWater PDK

Devices

Reference layouts



RF 0.18V pFET

4 fingers

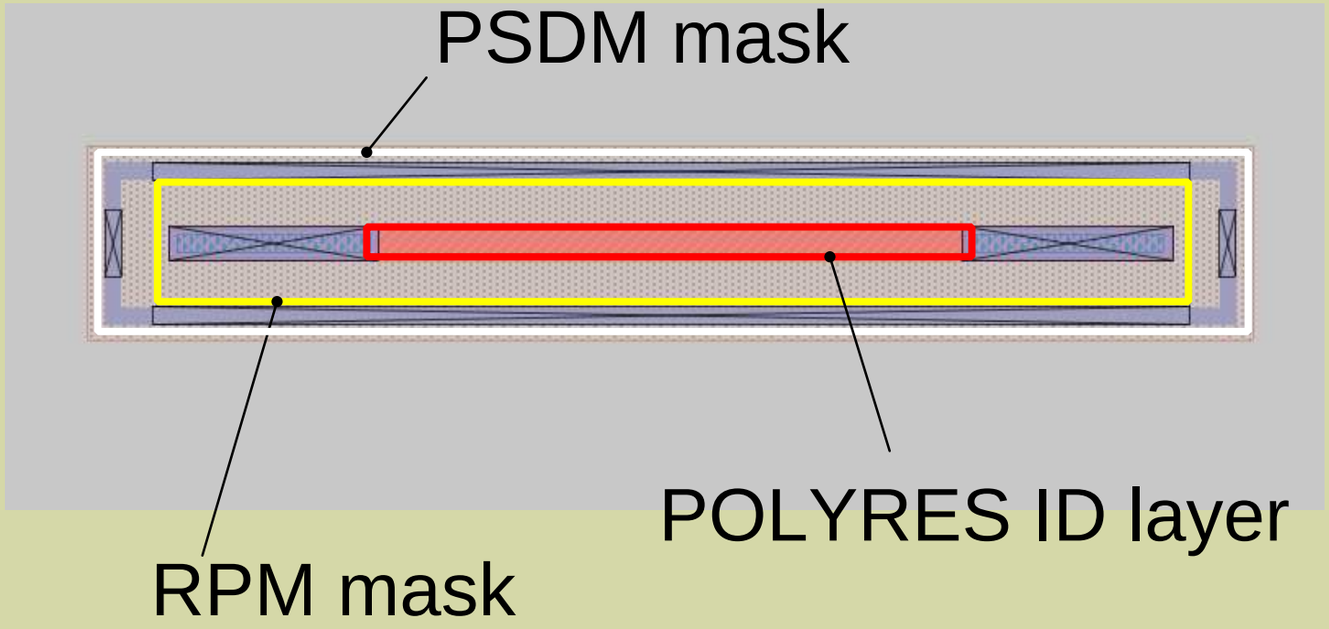
width = 3.0 µm

length = 0.15 µm

Understanding the SkyWater PDK

Devices

Hidden mask layers



Understanding the SkyWater PDK

Libraries

Understanding the SkyWater PDK

Libraries

Digital standard cells

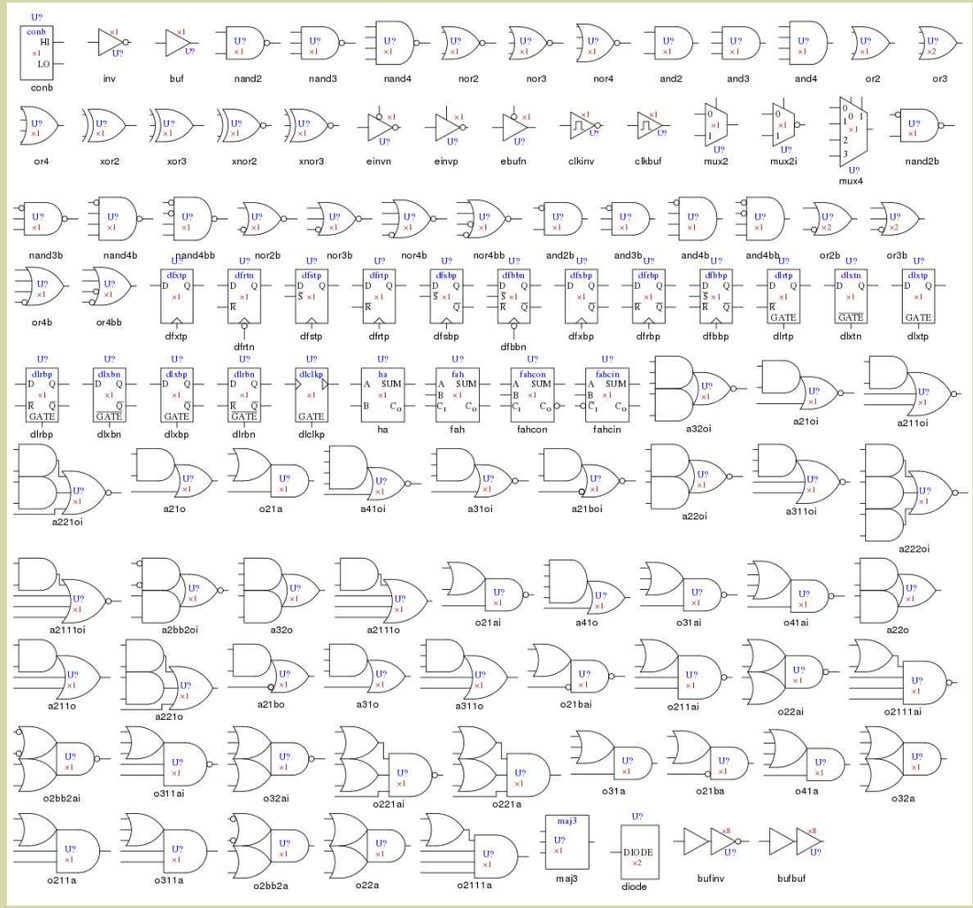
I/O cells

Primitive devices and models

Understanding the SkyWater PDK

Libraries

Digital standard cells



Understanding the SkyWater PDK

Libraries

Digital standard cells

Naming convention:

sky130_*vendor*_*library*−*type*[_*name*]

Understanding the SkyWater PDK

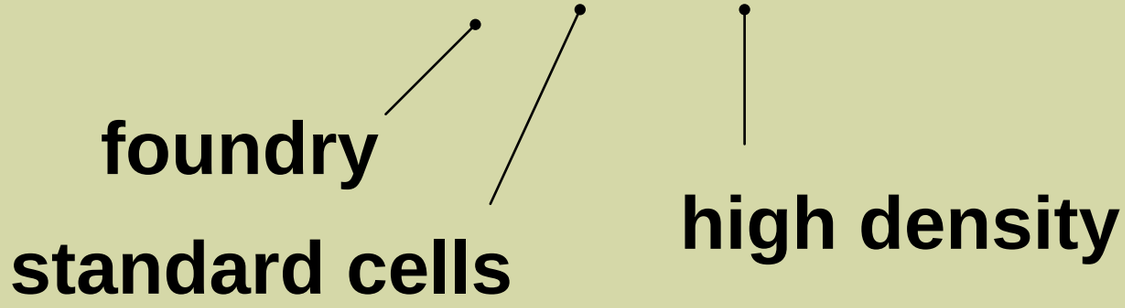
Libraries

Digital standard cells

Naming convention:

sky130_*vendor_library−type*[_*name*]

sky130_fd_sc_hd



Understanding the SkyWater PDK

Libraries

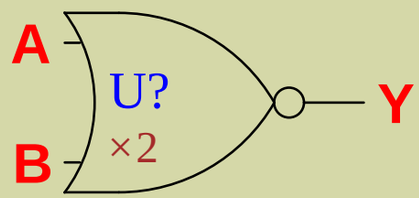
Digital standard cells

Naming convention:

sky130_*vendor_library−type*[_*name*]

library: **sky130_fd_sc_hd**

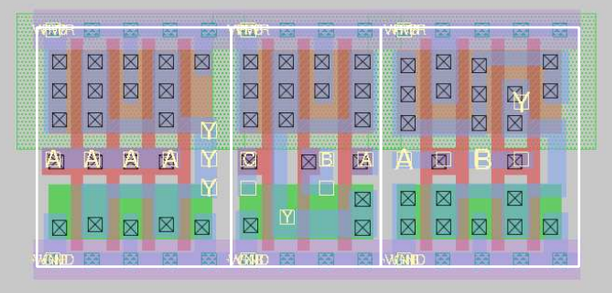
cellname: **sky130_fd_sc_hd__nor2_2**



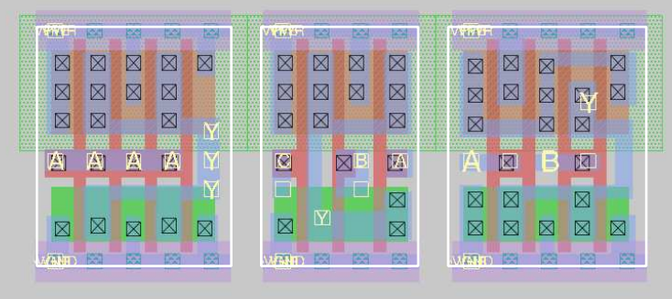
Understanding the SkyWater PDK

Libraries

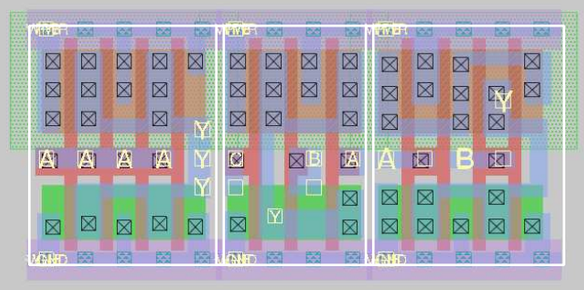
Digital standard cell abutment (when placed manually)



correct: abutment boxes touching



too far apart



too close together

Understanding the SkyWater PDK

Libraries

Digital standard cells

Documentation??

Understanding the SkyWater PDK

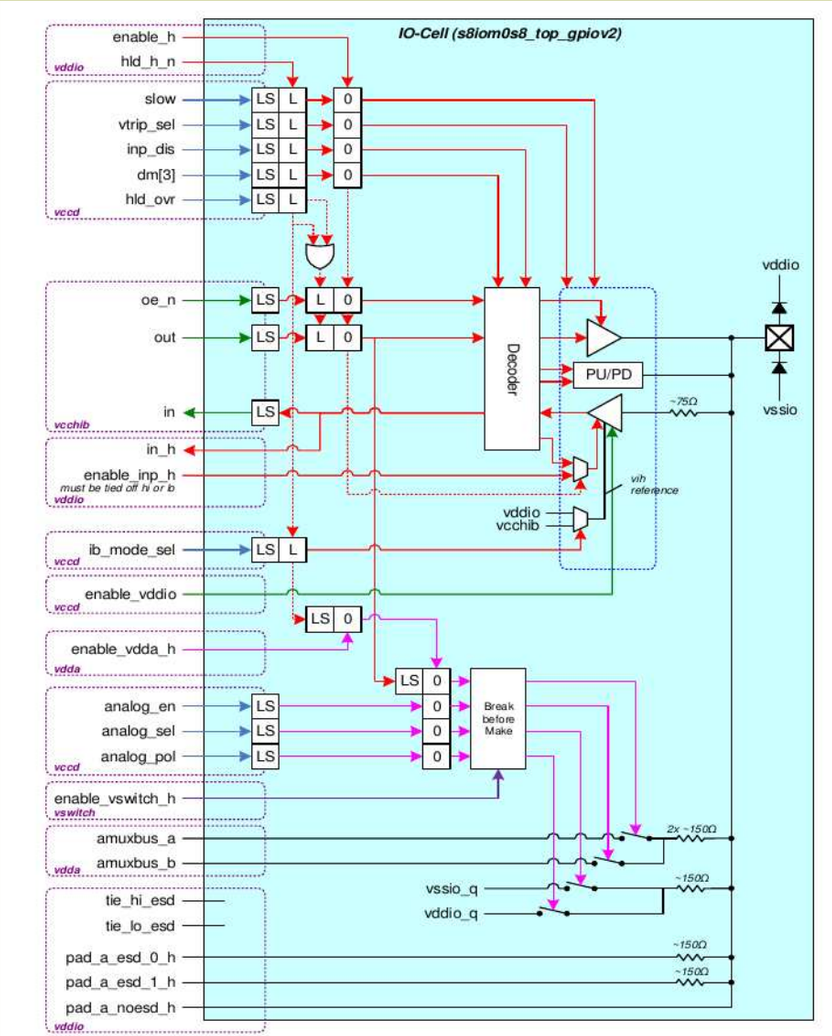


Figure 3: GPIO V2 Block Diagram

Libraries

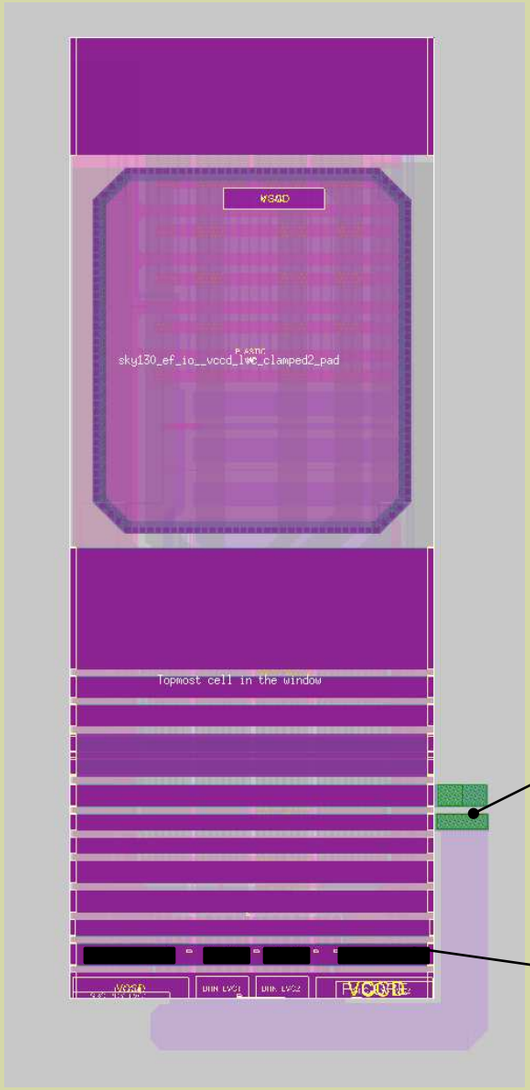
I/O cells

sky130_fd_io

input/output

foundry

Understanding the SkyWater PDK



Libraries

I/O cells

sky130_ef_io

efabless

overlay connects clamps to power rail

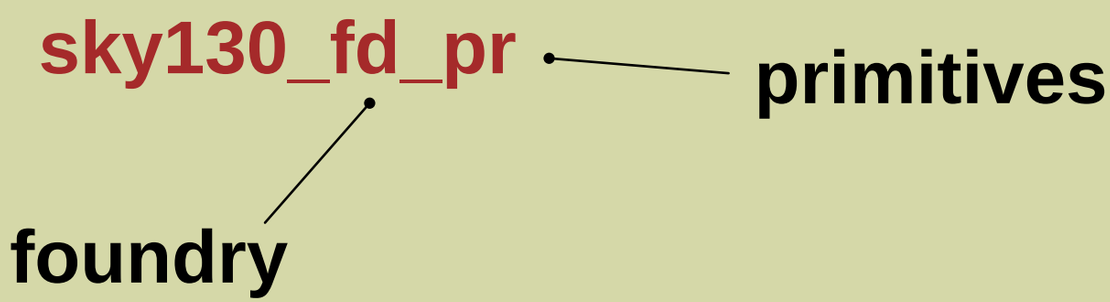
overlay connects pad to power rail

sky130_ef_io__vccd_lvc_clamped2_pad

Understanding the SkyWater PDK

Libraries

primitive devices and models

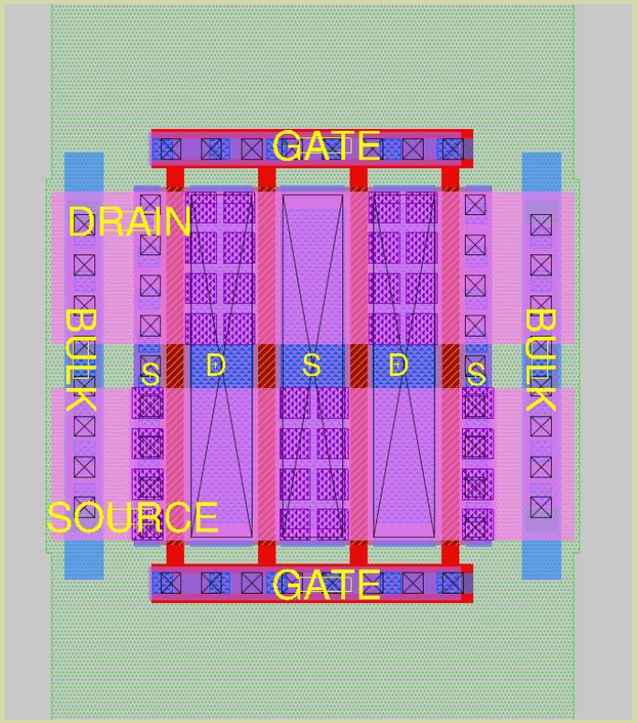


Understanding the SkyWater PDK

Libraries

primitive devices and models

sky130_fd_pr



RF frequency reference layout

RF 0.18V pFET

4 fingers

width = 3.0 µm

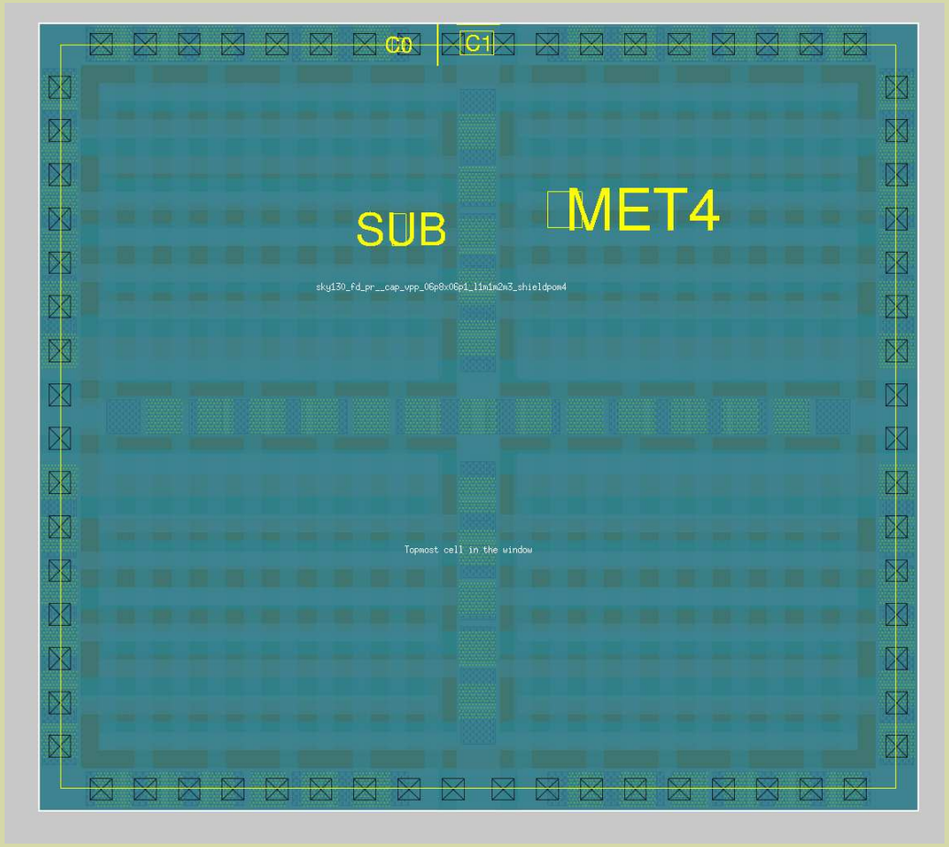
length = 0.15 µm

Understanding the SkyWater PDK

Libraries

primitive devices and models

sky130_fd_pr



vertical parallel plate capacitor

(vpp cap)

cap_vpp_06p8x06p1_l1m1m2m3_shieldpom4

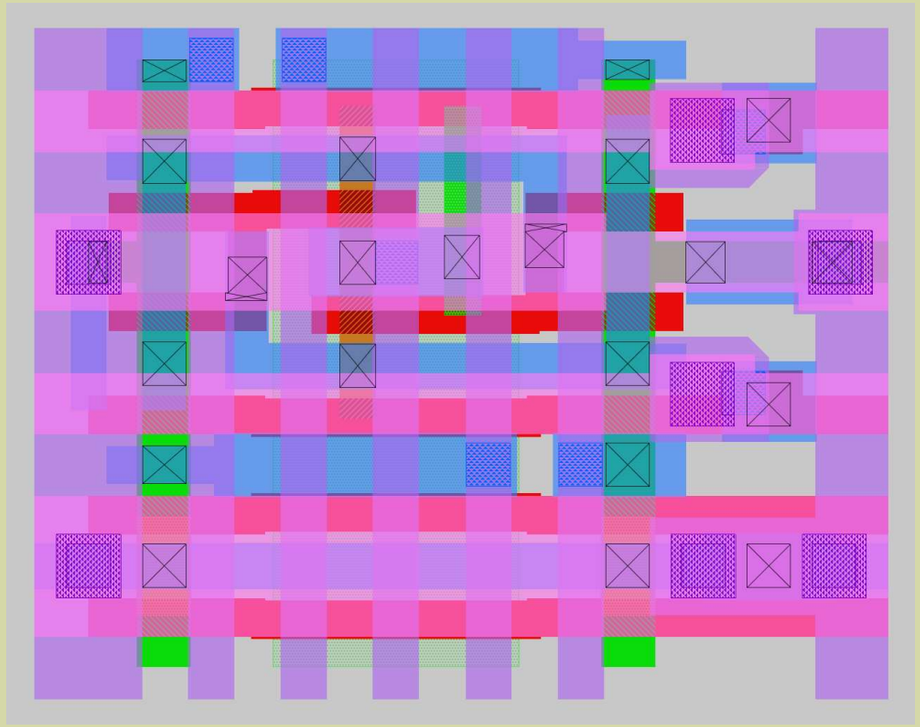
Understanding the SkyWater PDK

Libraries

SRAM

sky130_sram_macros — openRAM

sky130_fd_bd_sram — foundry (not yet available)



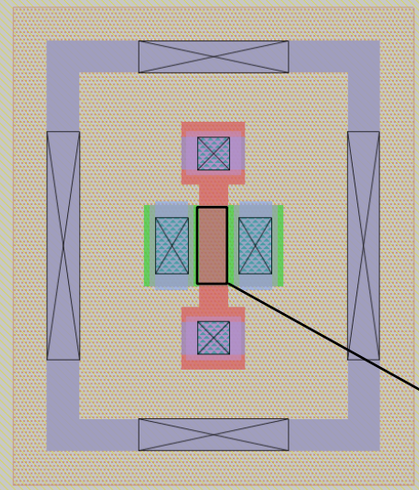
dual−port SRAM bit cell

Understanding the SkyWater PDK

Libraries

NVRAM

SONOS nFET transistor



buried floating gate

Open Source Tools and Flows

or. . . How can you design something?

Open Source Tools and Flows

A simple manual design flow

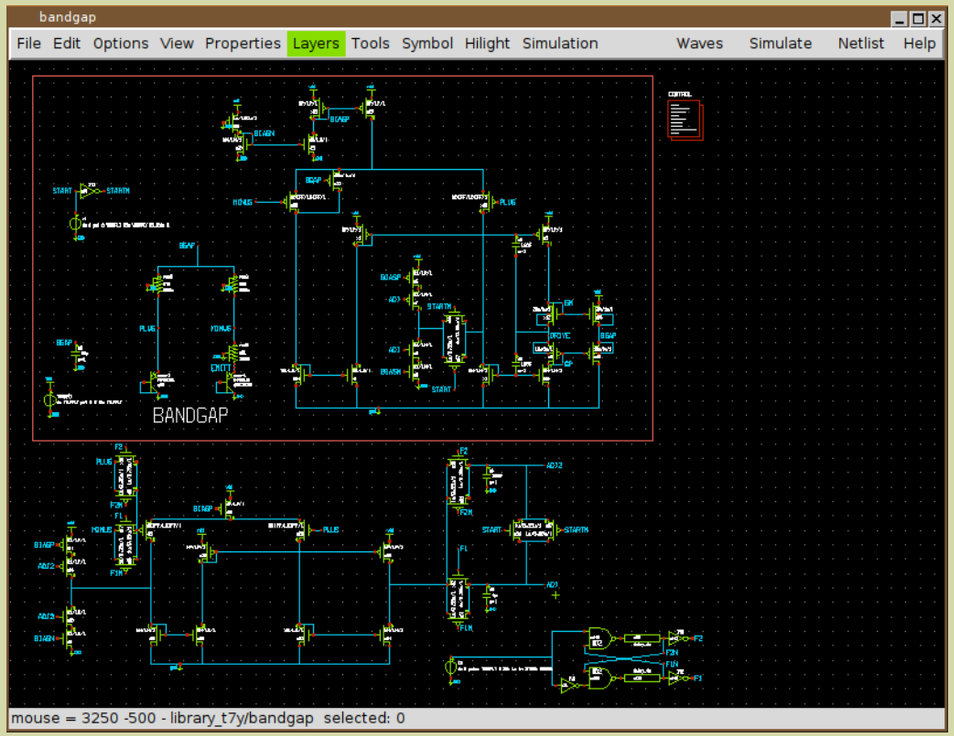
1. Schematic

Open Source Tools and Flows

A simple manual design flow

1. Schematic

xschem

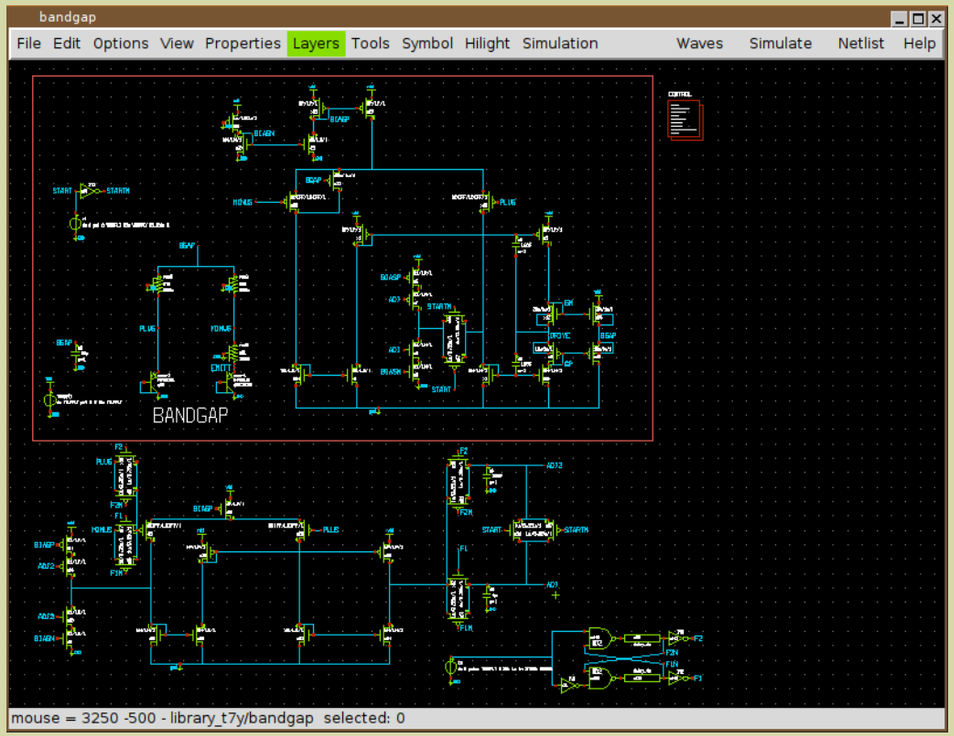


Open Source Tools and Flows

A simple manual design flow

1. Schematic → **ngspice** (analog simulation)

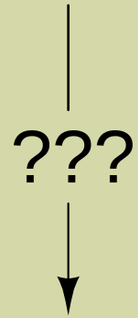
xschem → **gaw** (waveform viewing)



Open Source Tools and Flows

A simple manual design flow

1. Schematic



2. Layout

Open Source Tools and Flows

A simple manual design flow

1. Schematic

export →

netlist

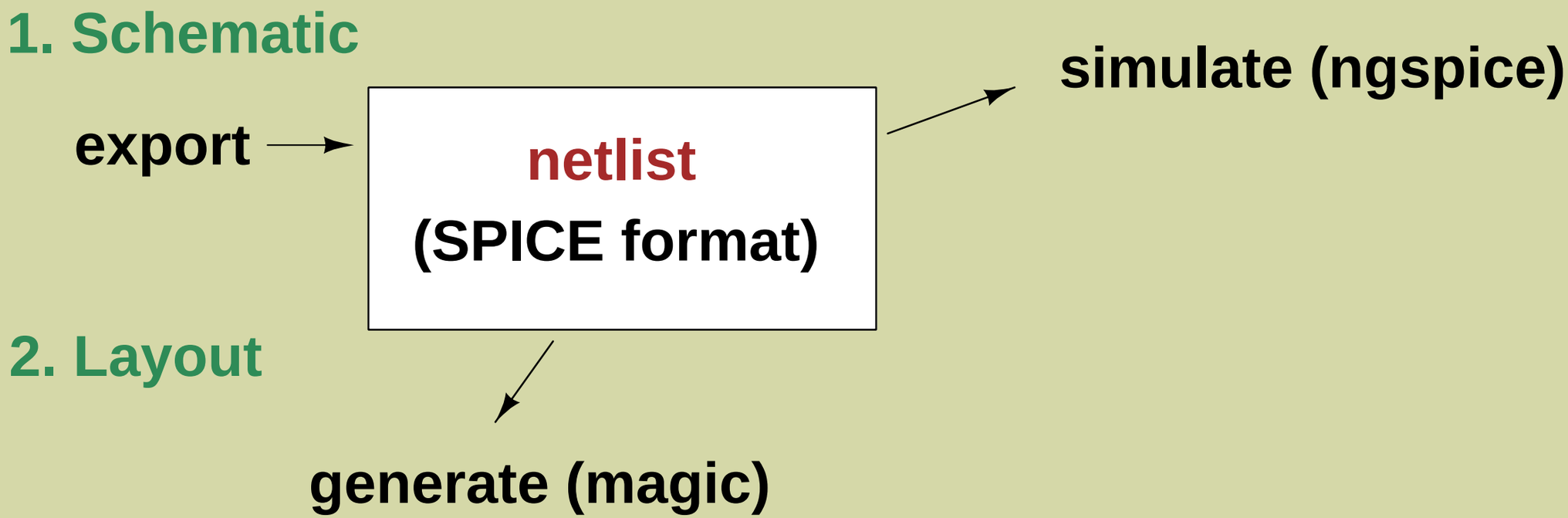
(SPICE format)

→ simulate (ngspice)

2. Layout

Open Source Tools and Flows

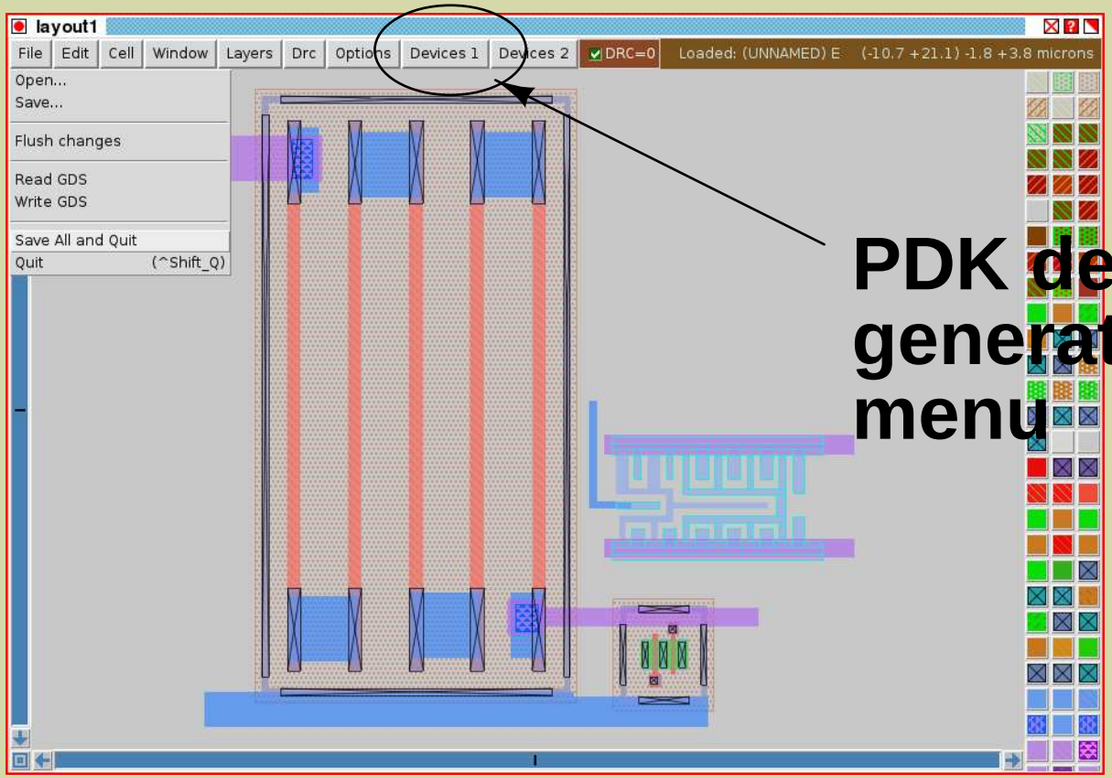
A simple manual design flow



Open Source Tools and Flows

A simple manual design flow

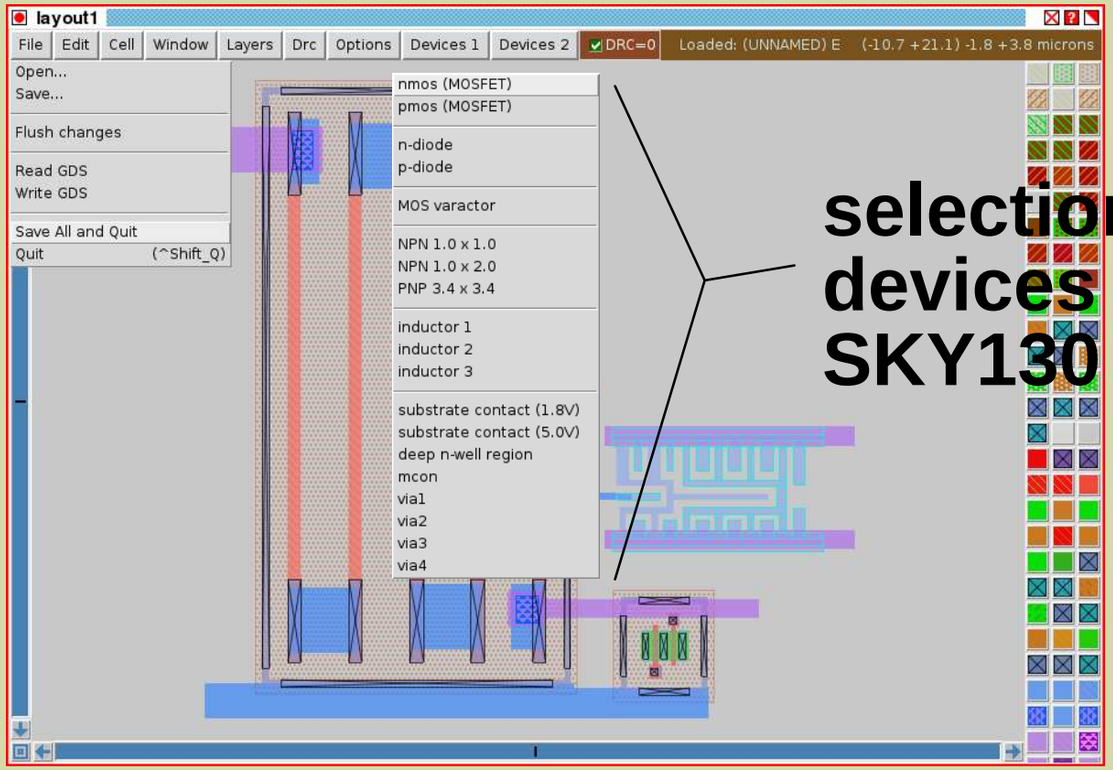
Parameterized devices in magic



Open Source Tools and Flows

A simple manual design flow

Parameterized devices in magic



selection of devices from SKY130 PDK

Open Source Tools and Flows

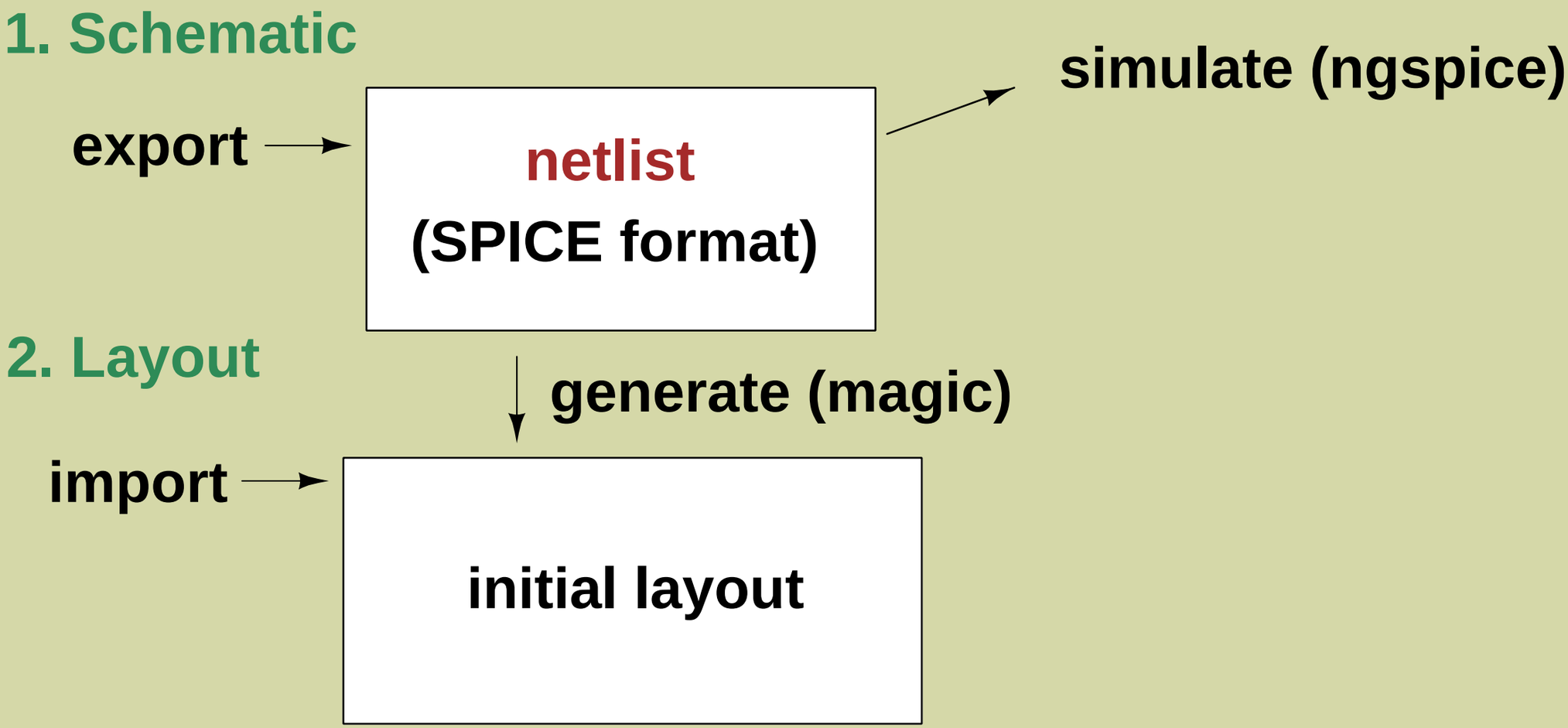
A simple manual design flow

Parameterized devices in magic

parameter selection window

Open Source Tools and Flows

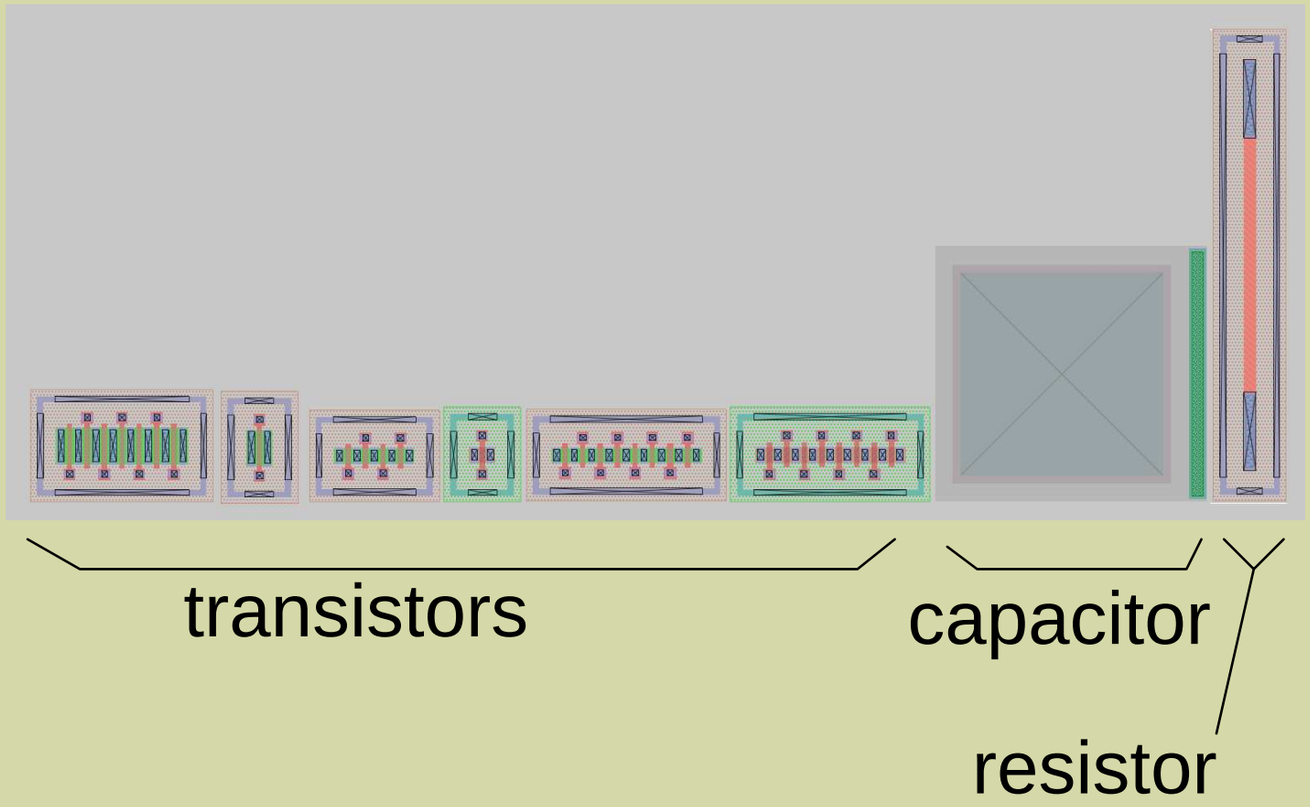
A simple manual design flow



Open Source Tools and Flows

A simple manual design flow

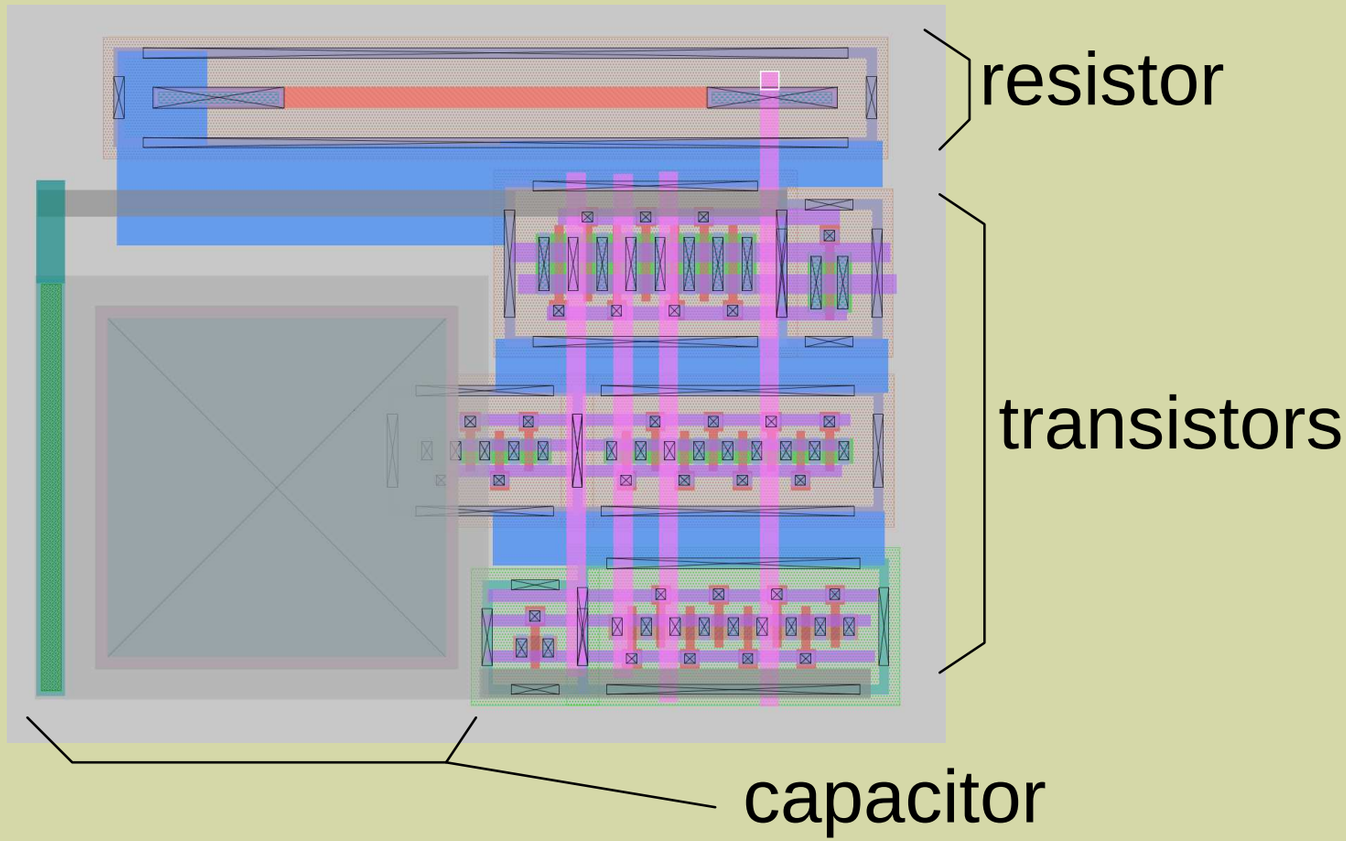
Example initial layout of devices in magic, imported from schematic



Open Source Tools and Flows

A simple manual design flow

Analog example layout
work in progress in magic



Open Source Tools and Flows

A simple manual design flow

1. Schematic

export →

(schematic capture)

netlist

(SPICE format)

2. Layout

export →

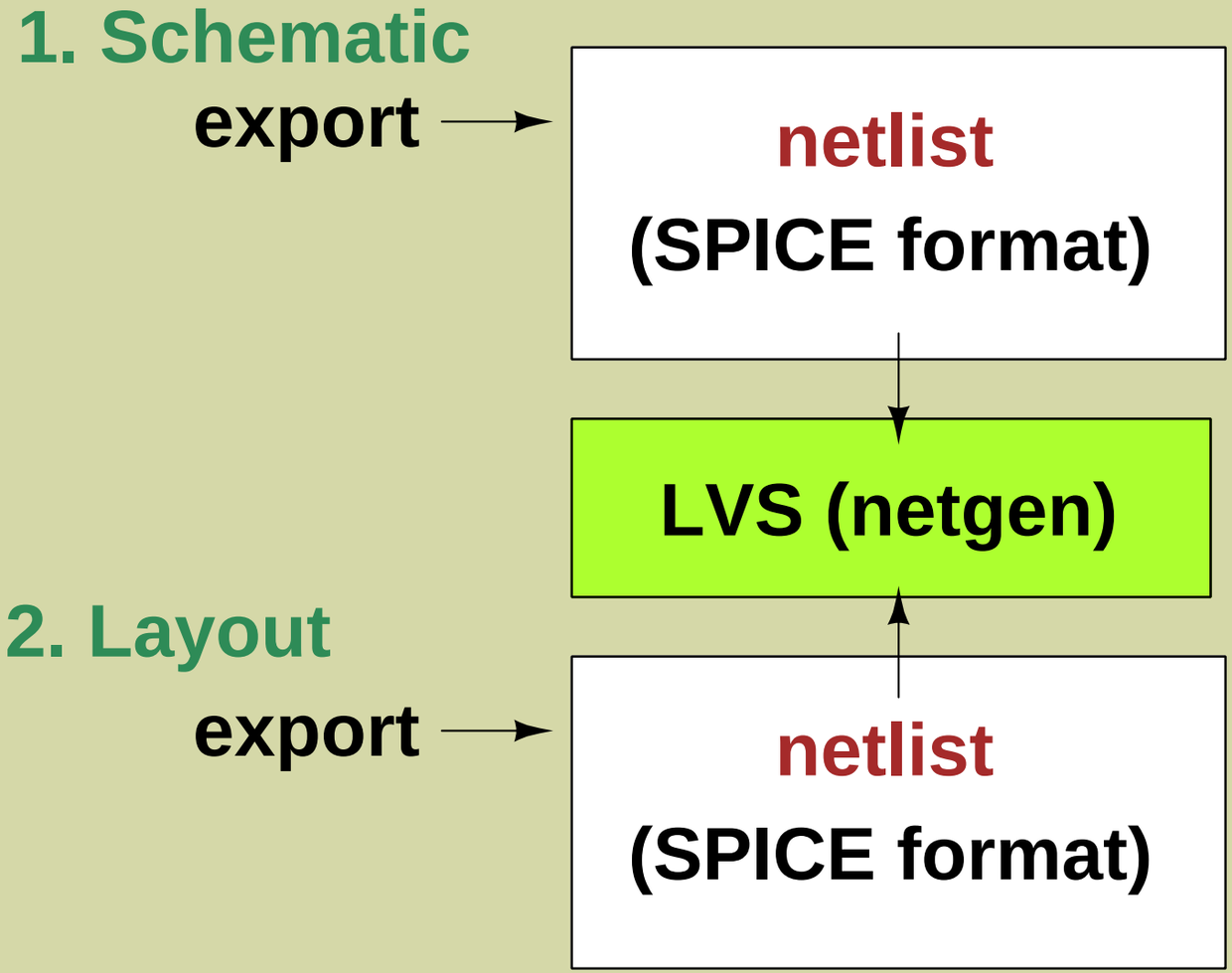
(extraction)

netlist

(SPICE format)

Open Source Tools and Flows

A simple manual design flow



Backend validation DIY

Running a simple example through the entire validation flow

1. **xschem** **Create a schematic**
2. **ngspice** **Simulation validation**
3. **magic** **Layout, DRC validation**
4. **netgen** **LVS validation**