Neuromorphic Integrated Bioelectronics - Fall 2025

BENG 216, UC San Diego

Homework 1: Due October 10, 2025

In this homework we will construct a silicon neuron from first principles, implementing a simplified version of the Hodgkin-Huxley model of spiking neuronal dynamics. In the process of this homework we will study fundamental building blocks for neuromorphic integrated circuit design, using simple models of metal-oxide-semiconductor (MOS) field-effect transistors in the subthreshold region of operation. This homework will also serve as an introduction to the electronic design automation (EDA) tools using the open-source SKY130 PDK for integrated circuit design and simulation in a 130nm CMOS (complementary MOS) process. Detailed guidelines and step-by-step instructions on using these tools for all homework and projects in this class are in the Cadence® Virtuoso® tutorial posted at https://isn.ucsd.edu/courses/beng216/complab/tut1.pdf.

Background

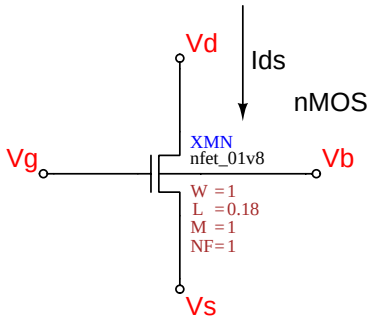
Subthreshold MOS Characteristics

Throughout this course we will primarily consider the MOS transistor in its *subthreshold* region of operation, for values of gate voltage below threshold where the channel connecting the source and the drain becomes cut-off on both sides. Under these conditions the channel current flowing from the source to the drain is dominated by diffusion of charge carriers (electrons or holes) that make it over the energy barrier in the channel due to their thermal energy. The gate voltage controls the height of the energy barrier, whereas the source and drain voltages control the carrier energy distribution on both sides of the channel. Hence the subthreshold channel current is exponential in voltage, following a Boltzmann distribution with a voltage scale given by the thermal voltage $V_t = kT/q$, where k is the Boltzmann constant, T is temperature, and q is the charge per carrier. For holes and electrons, V_t is around 25 mV at room temperature, and 26 mV at body temperature.

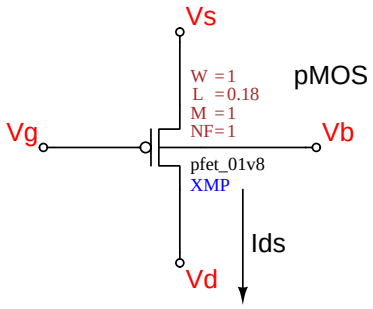
The subthreshold channel current is so small that it is often considered "leakage." Conventional models of the MOS transistor operating above-threshold even neglect subthreshold current altogether. However, not only is the subthreshold channel current non-zero, but it ranges over several orders of magnitude, from femtoamps to nanoamps. The high dynamic range and low power consumption of the MOS transistor operating in subthreshold make it the preferred circuit element in neuromorphic integrated circuit design. The physical correspondence of its Boltzmann thermodynamics with that for ion transport through biological membrane channels provide even further motivation for using MOS subthreshold circuits to directly emulate biological neural circuits.

Below are the equations describing the channel current I_{ds} of the MOS transistor in subthreshold as a function of the gate voltage V_g, source voltage V_s, drain voltage V_d, and bulk voltage V_b. Note that the direction of the channel current I_{ds}, as indicated in the diagrams below, is from source to drain for the pMOS transistor, but reverts direction from drain to source for the nMOS transistor because electrons flowing from source to drain imply a negative sign in the current. I_{ds} only depends on differences between voltages,

which are expressed in shorthand notation as gate-to-bulk voltage $V_{gb} = V_g - V_b$, drain-to-source voltage $V_{ds} = V_d - V_s$, etc.



$$\begin{aligned} I_{ds} &= I_n \frac{W}{L} e^{\frac{\kappa_n V_{gb}}{V_t}} \left(e^{-\frac{V_{sb}}{V_t}} - e^{-\frac{V_{db}}{V_t}}\right) \\ &= I_n \frac{W}{L} e^{\frac{\kappa_n V_{gb} - V_{sb}}{V_t}} \left(1 - e^{-\frac{V_{ds}}{V_t}}\right) \\ &= I_n \frac{W}{L} e^{\frac{\kappa_n V_{gb} - V_{sb}}{V_t}} \quad \text{in saturation } (V_{ds} \gg V_t) \end{aligned} \tag{1}$$

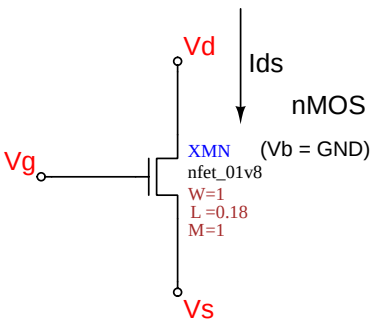


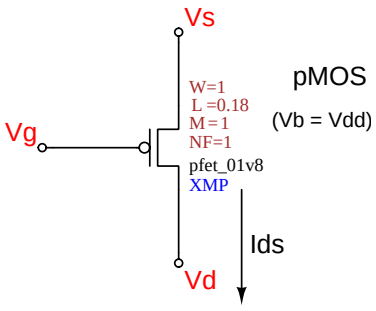
$$\begin{aligned} I_{ds} &= I_p \frac{W}{L} e^{-\frac{\kappa_p V_{gb}}{V_t}} \left(e^{\frac{V_{sb}}{V_t}} - e^{\frac{V_{db}}{V_t}}\right) \\ &= I_p \frac{W}{L} e^{-\frac{\kappa_p V_{gb} - V_{sb}}{V_t}} \left(1 - e^{\frac{V_{ds}}{V_t}}\right) \\ &= I_p \frac{W}{L} e^{-\frac{\kappa_p V_{gb} - V_{sb}}{V_t}} \quad \text{in saturation } (V_{ds} \ll -V_t) \end{aligned} \tag{2}$$

Here, I_n and I_p are process dependent current constants specific to the type and threshold of nMOS and pMOS transistor, typically in the pA range. Likewise, κ_n and κ_p are process dependent constant factors that characterize the gate-to-channel coupling efficiency relative to the bulk, typically around 0.7. Transistor width W and length L, in microns, are design parameters allowing control over the scale of the current. Multiplicy M and number of fingers NF shown in the diagrams are additional design parameters as multiplicative factors that are (almost) equivalent to scaling the width W by the same factors, but are convenient for layout purposes mitigating effects of transistor mismatch.

These equations are simplified and don't capture the complete subthreshold behavior of the MOS transistor, which include important effects such as drain conductance, drain induced barrier loading, etc. but are sufficient for most purposes in this class.

A further simplification results from considering that the bulk of a typical nMOS transistor is connected to the (lightly p-doped) substrate biased at Vss, the lowest supply voltage in the circuit which is typically set to the ground voltage GND at zero volts. Conversely, the (lightly n-doped) n-well bulk of a typical pMOS transistor is connected to the supply voltage Vdd as the highest voltage in the circuit. In such typical settings the bulk as fourth terminal of the MOS transistor is omitted from its symbol, but assumed connected to GND and Vdd:

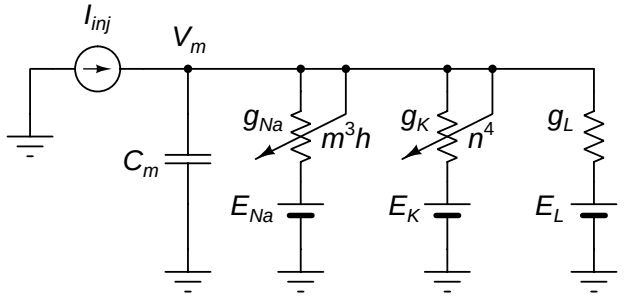




Hodgkin-Huxley Neurodynamics

Hodgkin and Huxley's classic (1952) model of action potential generation in the squid giant axon has become the standard model of single-cell neural dynamics. The Hodkin-Huxley (HH) model expresses the dynamics of the cell membrane voltage $V_m(t)$, under activation of an external current $I_{inj}(t)$ injected into the membrane, in terms of the membrane capacitance C_m and three membrane conductances, two of which are voltage-gated with dynamically varying dependence on membrane voltage:

$$\begin{aligned} C_m \frac{dV_m}{dt} &= -I_{Na} - I_K - I_L + I_{inj} \\ I_{Na} &= g_{Na}\, m^3 h\, (V_m - E_{Na}) \\ I_K &= g_K\, n^4\, (V_m - E_K) \\ I_L &= g_L\, (V_m - E_L) \end{aligned} \tag{3}$$



In particular, upon an increase in membrane voltage, the sodium conductance $g_{Na}\, m^3 h$ undergoes *fast activation* through the $m(t)$ gating variable, followed by *slow inactivation* through the $h(t)$ gating variable. Similarly, the potassium conductance $g_K\, n^4$ responds to an increase in voltage with *slow activation* through the $n(t)$ gating variable. The time varying sodium and potassium conductances, together with the constant leak conductance g_L, drive the membrane voltage dynamically between the three reversal potentials. The sodium reversal potential E_{Na} is the highest of the three, around +60 mV, whereas the potassium reversal potential E_K is the lowest, around -90 mV, with the leak reversal potential E_L near rest in the center. Hence, beyond a given threshold in membrane potential, positive feedback by fast sodium activation causes a runaway condition that generates a fast-rising action potential reaching towards E_{Na}, then followed by slow sodium inactivation and potassium activation that terminate the action potential and maintain the membrane potential near E_K for the duration of a refractory period that lasts until all gating variables and the membrane return to rest, leaving the membrane in a low conductance state. The neuron is then ready for the next action potential in response to the external current I_{inj} charging the membrane capacitance C_m.

The precise functional form of the kinetics of the gating variables m, n and h specified by Hodgkin and Huxley is not important and, in fact, amounts to heuristic curve fitting of their measured data. Here we will investigate a simple neuromorphic silicon instantiation of the HH model implementing the dynamic voltage-gated sodium and potassium conductances with MOS transistors in subthreshold. In particular, pMOS transistors connected to a positive supply E_{Na} as high as Vdd will implement the sodium conductances, whereas nMOS transistors connected to a lower supply E_K as low as GND will implement the potassium conductances. Activation and inactivation by the gating variables will be approximated using exponential voltage dependence that is innate to the subthreshold conductances. Fast sodium activation m will require inverting amplification of the membrane potential driving a pMOS gate for fast positive feedback to generate the action potential, whereas slow sodium inactivation h combined with slow potassium activation n will require delayed buffering of the membrane potential driving pMOS and nMOS gates for slow negative feedback to terminate the action potential and maintain a refractory period.

Computational Laboratory and Homework

1. *Conductance-based model of action potential generation and refractory period* [15 points].

   Consider the simplified HH model given in (3) and shown above.

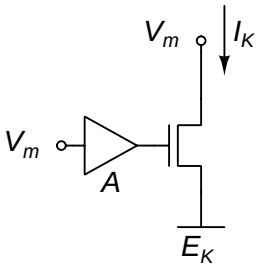
   (a) Ignoring the slow response of h and n to changes in membrane potential V_m, find an expression for a condition on V_m defining the onset of an action potential. *Hint*: consider the small-signal membrane conductance $g_m = dI_m \,/\, dV_m$ for fast small-signal changes in membrane potential, and evaluate its polarity.

   (b) What determines the duration of the refractory period to first order, in qualitative terms?

2. *MOS transconductance as a model of a voltage-gated ion channel* [40 points].

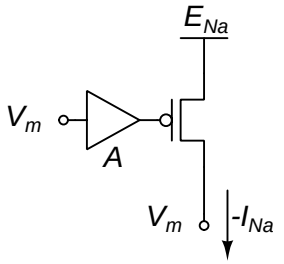
   Now consider an MOS transistor with source terminal connected to a constant voltage supply, modeling an ion channel with constant reversal potential and variable, voltage-gated conductance. Naturally, we use pMOS conductances with high reversal potentials, and nMOS conductances with low reversal potentials.

   (a) First consider an nMOS transistor with source connected to E_K, modeling a potassium ion channel with reversal potential E_K. The drain connects to the membrane, and a buffered version of the membrane voltage V_m with gain $A = 1$ is presented to the gate. Find the small-signal membrane conductance $g_m = dI_K \,/\, dV_m$ as a function of the membrane voltage V_m. Does this implement activation or inactivation with rising membrane voltage?

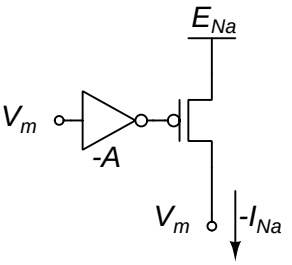


   (b) Quantify the subthreshold slope for $\kappa_n = 0.7$ at room temperature, and compare with that observed by Hodgkin and Huxley for the squid giant axon potassium channel below threshold, around 4.8 mV/e-fold. Explain the discrepancy in the magnitude of the slope, and explain how you can correct for it by adjusting the amplifier gain A.

   (c) Repeat the analysis for a pMOS transistor with source connected to E_{Na}, modeling a sodium ion channel with reversal potential E_{Na}. Note that the sodium current flows opposite to the potassium current, into the cell, hence I_{Na} is negative. In the electrical diagram on the right this is shown as a positive current $-I_{Na}$ flowing from E_{Na} into the membrane.



   (d) Now consider an inverting amplifier instead of a buffer, amplifying the membrane voltage with inverting gain $-A < 0$ to drive the gate of the pMOS transistor. Show how inversion of the gain turns sodium inactivation into sodium activation. (*Note on drawing conventions*: Small open circles at ending lines denote terminals to interface pins, whereas the larger open circles at inputs and outputs of gate symbols, such as for the pMOS transistor and inverting amplifier, denote logical inversion.)



   (e) For $A = -1$ and $\kappa_p = 0.7$ at room temperature, compare the subthreshold slope with that experimentally observed by Hodgkin and Huxley for squid giant axon subthreshold sodium activation, around 3.9 mV/e-fold. Again explain the discrepancy and correct for it by adjusting the inverting amplifier gain.

3. *Series combination of MOS transconductors for multiplicative voltage gating* [15 points].

   (a) Show that a series combination of two identical pMOS transistors, with gate voltages V_{g1} and V_{g2}, gives a current that is equivalent to that of a single identical pMOS transistor with gate voltage V_g satisfying:

$$e^{-\frac{\kappa_p V_g}{V_t}} = \frac{e^{-\frac{\kappa_p V_{g1}}{V_t}}\, e^{-\frac{\kappa_p V_{g2}}{V_t}}}{e^{-\frac{\kappa_p V_{g1}}{V_t}} + e^{-\frac{\kappa_p V_{g2}}{V_t}}} \tag{4}$$

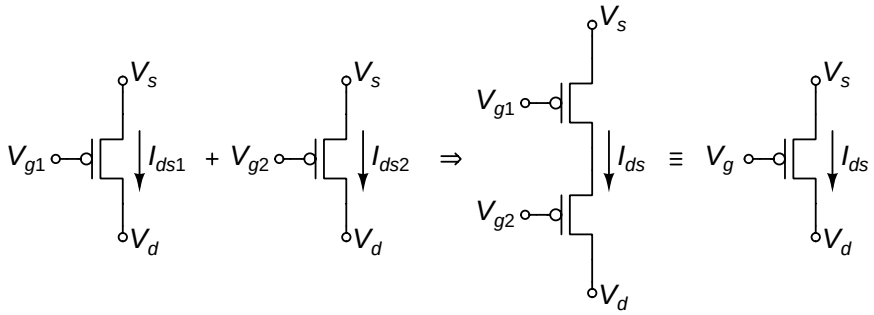
   or, equivalently:

$$e^{\frac{\kappa_p V_g}{V_t}} = e^{\frac{\kappa_p V_{g1}}{V_t}} + e^{\frac{\kappa_p V_{g2}}{V_t}}. \tag{5}$$

   (b) Does exchanging the order of the two transistors make a difference? Why?

   Note the similarity of (4) and (5) to the statements for series combinations of conductances and resistances, respectively: $G = G_1\, G_2\, /\, (G_1 + G_2)$ and $R = R_1 + R_2$, except that they hold even for the large-signal nonlinear MOS conductances:

$$I_{ds} = \frac{I_{ds1}\, I_{ds2}}{I_{ds1} + I_{ds2}}. \tag{6}$$

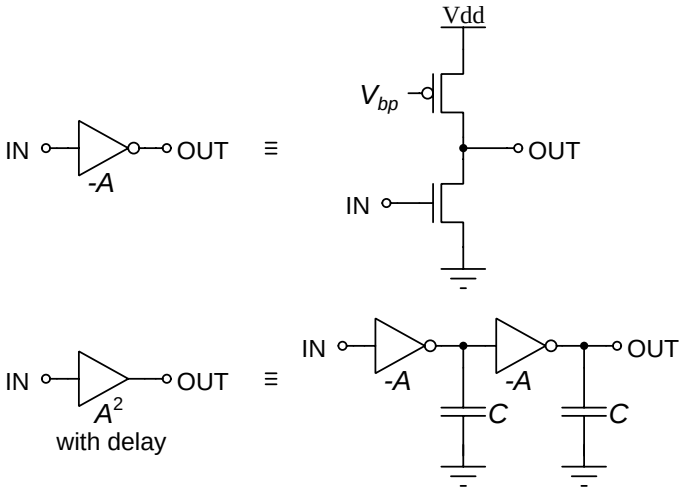


   We will use this property to approximate the multiplicative voltage gating m^3h in the sodium conductance by series combination of two MOS transconductors realizing m^3 and h respectively, giving rise to combined voltage gating by $m^3h\, /\, (m^3 + h)$. This implements a normalized version of the desired product term. We will leave the normalization factor for what it is; realizing just the product m^3h can be done with translinear MOS circuits at slightly greater complexity and we will return to this later.

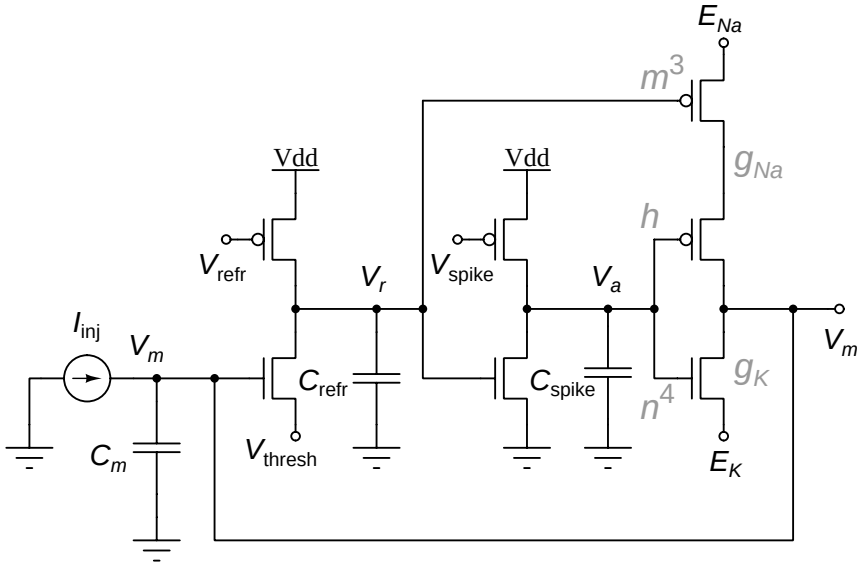
4. *Putting it all together: A simple 7-MOS silicon HH neuron* [30 points].

   What is left for us to do in order to implement the HH dynamics (3) in a neuromorphic silicon circuit with subthreshold MOS transconductances is to work out the circuits for the inverting and non-inverting amplifiers. A fast inverting amplifier is needed to realize fast Na activation by the m gating variable. This is implemented by a two-transistor pseudo-nMOS inverter circuit comprising an nMOS transconductor and a pMOS current comparator as shown below. The pMOS transistor with gate bias V_{bp} supplies a constant reference current which defines the threshold of the input, so that OUT goes low or high when the nMOS current is greater or smaller, respectively. The input voltage for which the nMOS transconductor generates the same current defines the inverter threshold, with OUT going low for IN above the threshold, and vice versa. A slow non-inverting amplifier to realize both slow Na inactivation by h and slow K activation by n is realized by cascading two inverting amplifiers,

with one or both of the nodes loaded with a capacitance. The capacitances together with the reference current set the slew rate on the voltage transitions of the center node, which determines the switching delay.



The complete HH neuron circuit is shown below. The inverting amplifier for m fast Na activation is reused as the first in the chain of two inverting amplifiers implementing the non-inverting delaying buffer for the h slow Na inactivation and n slow K activation. Separate bias voltages for the current references in the two inverting amplifiers provide independent control over spiking and refractory time scales. A separate source voltage bias for the nMOS transistor in the first inverting amplifier provides independent control over the neuron firing threshold.



All nMOS and pMOS transistors are 1 μm wide and 0.18 μm long, using the devices available in the 130nm CMOS process part of the Skywater SKY130 Open PDK. Use the `sky130_fd_pr_main nfet_1v8` and `pfet_1v8` devices included with the PDK. (See the BENG 216 Cadence Skywater 130nm tutorial at https://isn.ucsd.edu/courses/beng216/complab/tut1.pdf). The membrane capacitance C_m is 1 pF, the spike accommodation capacitance C_{spike} is 100 fF, and the refractory period capacitance C_{refr} is 10 fF. The following settings of voltage supplies and biases provide a good starting point to explore the dynamics of the circuit in the simulations:

$\text{Vdd} = 1.2$ V $\quad I_{\text{inj}} = 10$ pA
$E_{Na} = \text{Vdd} \quad E_K = V_{\text{thresh}} = \text{GND}$
$V_{\text{refr}} = V_{\text{spike}} = 0.8\text{V}$

(a) [10 pts] Enter the HH neuron circuit, as shown, in Cadence® Virtuoso® using the Skywater 130nm CMOS process. These tools are installed and available from your class accounts, and you can directly proceed by following the steps and guidelines as outlined in the Cadence Skywater 130nm tutorial.

(b) [20 pts] Simulate the circuit using Cadence® Spectre® for at least three values of injected current: $I_{inj} = 1$ pA, 10 pA, and 100 pA. Record the voltage waveforms for V_m and the intermediate variables V_r and V_a in the circuit, and explain what you observe. Compare the dynamics of these waveforms with those for V_m, m, n and h in the HH model, in qualitative terms. *Note*: You may need to adjust the default simulator settings to get the circuit to run at the very low levels of current it is designed for. In particular, the absolute tolerance for currents should be at most 10 fA, and the relative tolerance at most 10^{-4}.

If you find that your simulation is taking forever to settle into the limit cycle you expect of a regularly spiking neuron, you may want to set initial conditions away from the Spectre default which is the stationary point found for the DC operating point. For instance, you could initialize the membrane to GND, which consistently initializes the first inverter output to Vdd, and the second to GND. This corresponds to initializing the neuron circuit in its integration region of operation, just following the refractory period of the previous spike, during which the membrane integrates the input current until the membrane reaches the threshold for the next spike.

If you find that your neuron spikes at a rate much faster than can be expected from any biophysical neuron, you need to adjust the neuron parameters accordingly. Increasing V_{thresh} will increase the integration time window, and increasing V_{refr} will increase the refractory period.

Background: One of the artifacts of noiseless spice simulations is that it takes forever to escape from an unstable stationary point. This is a typical problem encountered with multistable and astable circuits such as latches and ring oscillators; in fact, the neuron circuit is a special form of a three-stage ring oscillator. The transients are small-signal growing oscillations away from the stationary point and towards the large-signal limit cycle, very slowly! And this behavior can also be seen in the noiseless HH model starting from its stationary point, see for instance https://isn.ucsd.edu/courses/beng260/lectures/week3.pdf. Getting stuck near a stationary point is an artificial problem not encountered in real circuits: additive noise naturally present pushes the dynamics away from the stationary point a lot faster.

(c) [*Bonus*: Extra +10 pts] Estimate the energy efficiency of the HH silicon neuron, by observing the total current flowing through the voltage supply Vdd. This current, multiplied by Vdd, gives the instantaneous power. If the supply E_{Na} is independent from Vdd, make sure to include its supplied power as well. The time integral of the total power over the interval between spikes gives an estimate of the energy consumption per spike. Adjust the biases in order to minimize this energy without compromising the spiking dynamics of the circuit. Compare your energy with that for biological neurons, which is on the order of 1 pJ per spike (10^{12} neurons firing at 10 Hz on average with 10 W of metabolic brain power). Is this a fair comparison, and why?

Submission Guidelines

You are encouraged to work on teams and exchange solution strategies and share configuration of the EDA tools, but you must complete the homework yourself, and are not allowed to copy other's work. In particular

you cannot share schematics for homework submission and need to complete the capture and simulation of your schematic entirely by yourself. It is anticipated that no two independent schematic entries are identical.

Turn in your homework as a single PDF over canvas by the due date. Scanned handwritten notes are fine. Include a printout or screenshots of your schematic as entered, and recorded waveforms for at least three values of injected current.