BENG 216
Neuromorphic Integrated Bioelectronics

Week 1: Biophysical Foundations

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http://isn.ucsd.edu/courses/beng216

BENG 216 Neuromorphic Integrated Bioelectronics

Date	Topic
9/29, 10/1	Biophysical foundations of natural intelligence in neural systems. Subthreshold MOS silicon models of membrane excitability. Silicon neurons. Hodgkin-Huxley and integrate-and-fire models of spiking neuronal dynamics. Action potentials as address events.
10/6, 10/8	Silicon retina. Low-noise, high-dynamic range photoreceptors. Focal-plane array signal processing. Spatial and temporal contrast sensitivity and adaptation. Dynamic vision sensors.
10/13, 10/15	Silicon cochlea. Low-noise acoustic sensing and automatic gain control. Continuous wavelet filter banks. Interaural time difference and level difference auditory localization. Blind source separation and independent component analysis.
10/20, 10/22	Silicon cortex. Neural and synaptic compute-in-memory arrays. Address-event decoders and arbiters, and integrate-and-fire array transceivers. Hierarchical address-event routing for locally dense, globally sparse long-range connectivity across vast spatial scales.
10/27, 10/29	Midterm review. Modular and scalable design for neuromorphic and bioelectronic integrated circuits and systems. Design for full testability and controllability.
11/3, 11/5	Low-noise, low-power design. Fundamental limits of noise-energy efficiency, and metrics of performance. Biopotential and electrochemical recording and stimulation, lab-on-a-chip electrophysiology, and neural interface systems-on-chip.
11/10, 11/12	Adaptive offset cancelation and autoranging in dynamic vision sensing. Tobi Delbruck's lecture on silicon retina history with a live demo of event-based dynamic vision systems.
11/17, 11/19	Learning and adaptation to compensate for external and internal variability over extended time scales. Background blind calibration of device mismatch. Correlated double sampling and chopping for offset drift and low-frequency noise cancellation.
11/24, 11/26	Energy conservation. Resonant inductive power delivery and data telemetry. Ultra-high efficiency neuromorphic computing. Resonant adiabatic energy-recovery charge-conserving synapse arrays.
12/1 - 12/5	Project final presentations. All are welcome!

Lee Sedol vs. AlphaGo
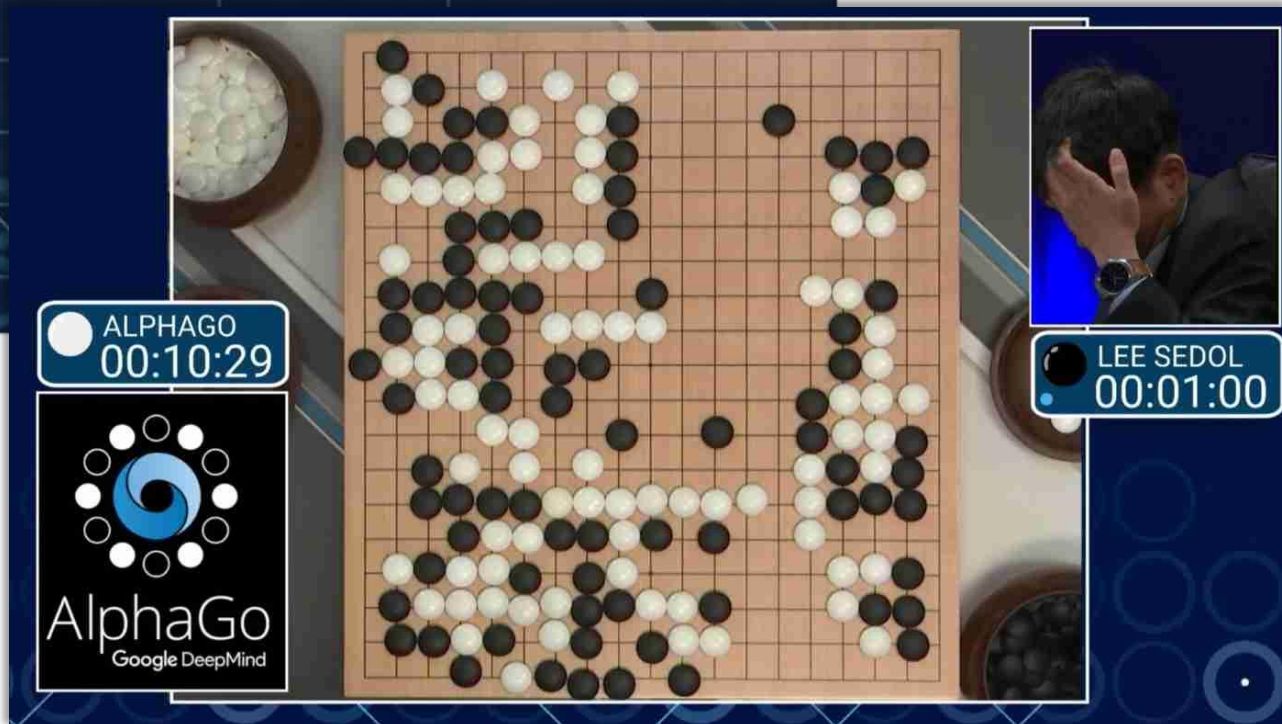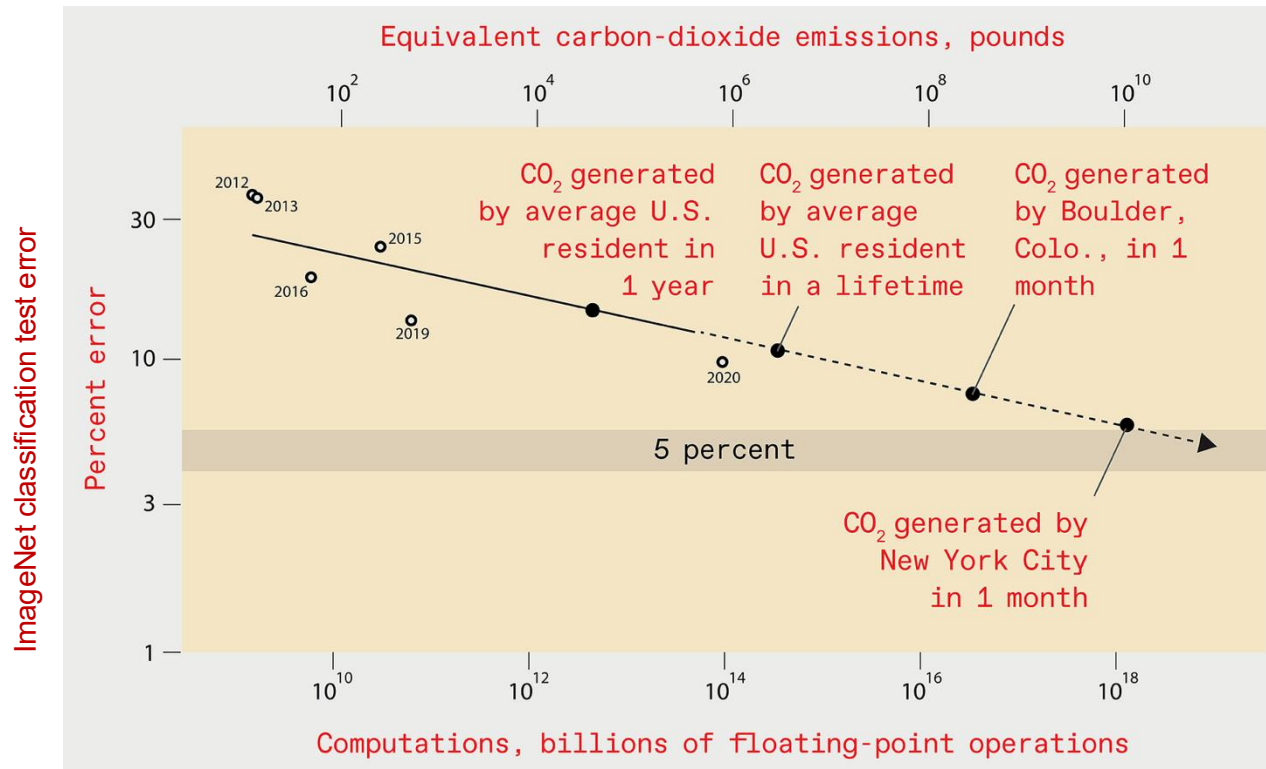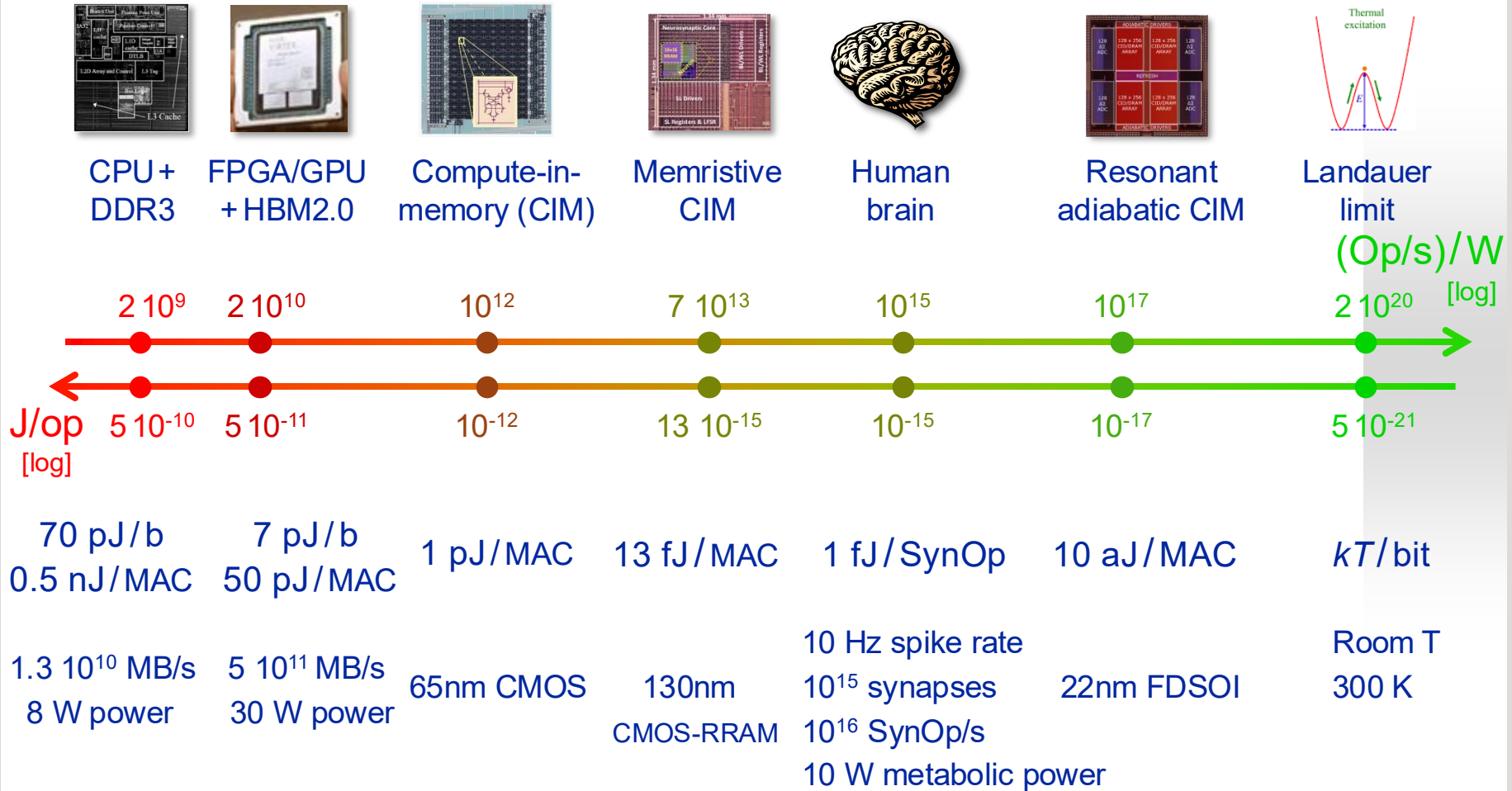*Go World Champion vs. Google DeepMind*
~ 100 W   **~ 100 kW**

Steep Costs of Today's Deep Learning

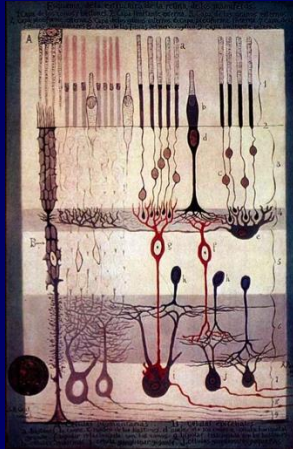
N.C. Thompson, K. Greenewald, K. Lee, G.F. Manso, "Deep learning's diminishing returns--The cost of improvement is becoming unsustainable." IEEE Spectrum, 24 Sept. 2021.
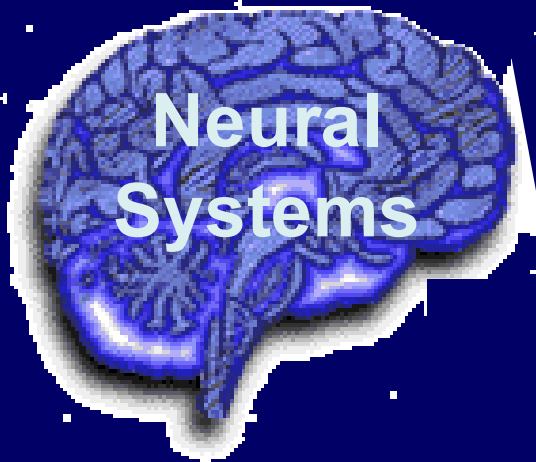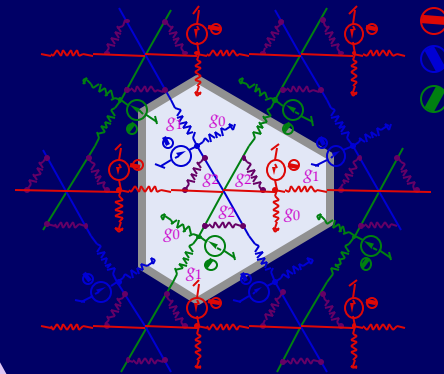
Energy Efficiency Spectrum

| CPU+ DDR3	FPGA/GPU +HBM2.0	Compute-in-memory (CIM)	Memristive CIM	Human brain	Resonant adiabatic CIM	Landauer limit

(Op/s)/W [log]

$2\ 10^9$	$2\ 10^{10}$	10^{12}	$7\ 10^{13}$	10^{15}	10^{17}	$2\ 10^{20}$

J/op [log]

$5\ 10^{-10}$	$5\ 10^{-11}$	10^{-12}	$13\ 10^{-15}$	10^{-15}	10^{-17}	$5\ 10^{-21}$

70 pJ / b 0.5 nJ / MAC	7 pJ / b 50 pJ / MAC	1 pJ / MAC	13 fJ / MAC	1 fJ / SynOp	10 aJ / MAC	kT / bit
$1.3\ 10^{10}$ MB/s 8 W power	$5\ 10^{11}$ MB/s 30 W power	65nm CMOS	130nm CMOS-RRAM	10 Hz spike rate 10^{15} synapses 10^{16} SynOp/s 10 W metabolic power	22nm FDSOI	Room T 300 K

Neuromorphic Engineering
"in silico" neural systems design

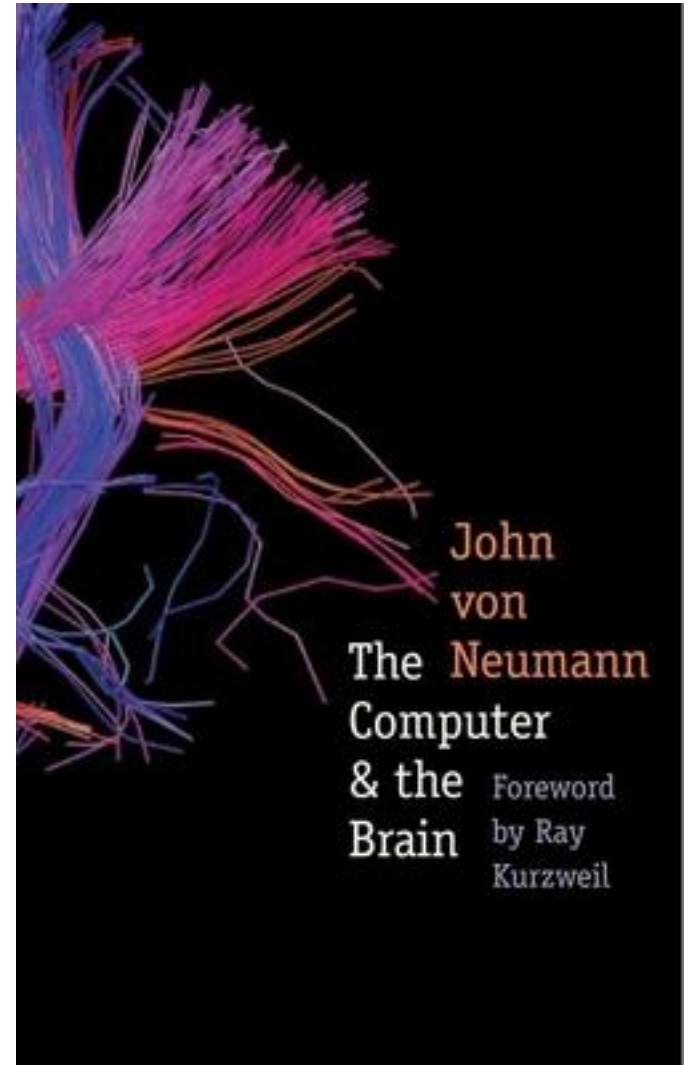*Neuromorphic Engineering*

Neural Systems

Learning & Adaptation
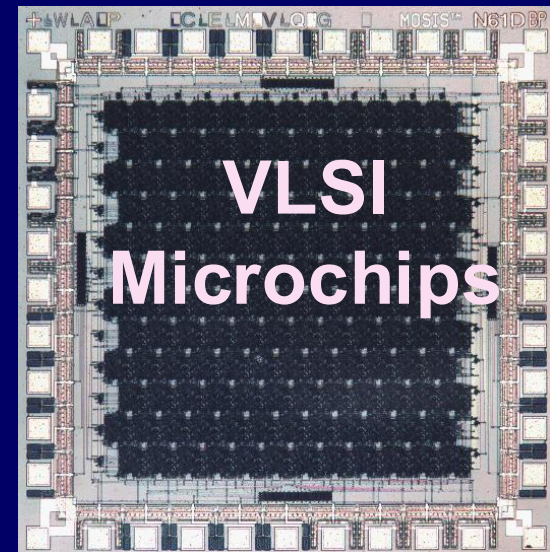
VLSI Microchips

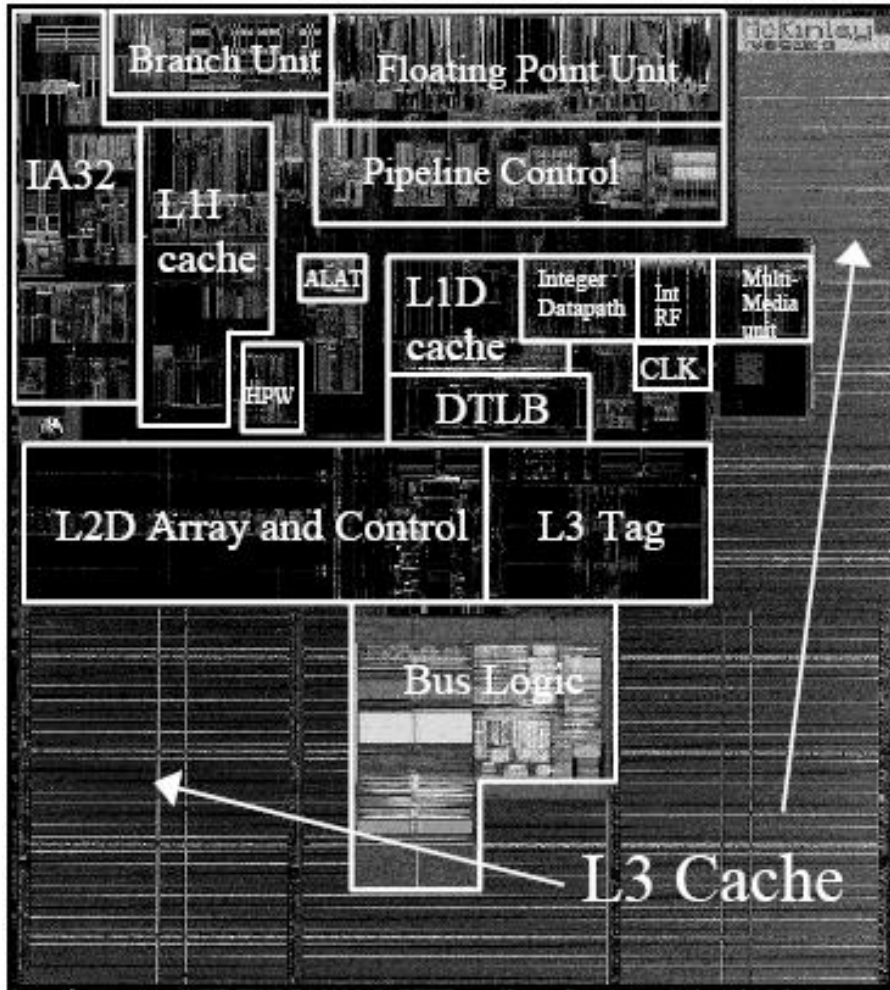# The Computer and the Brain
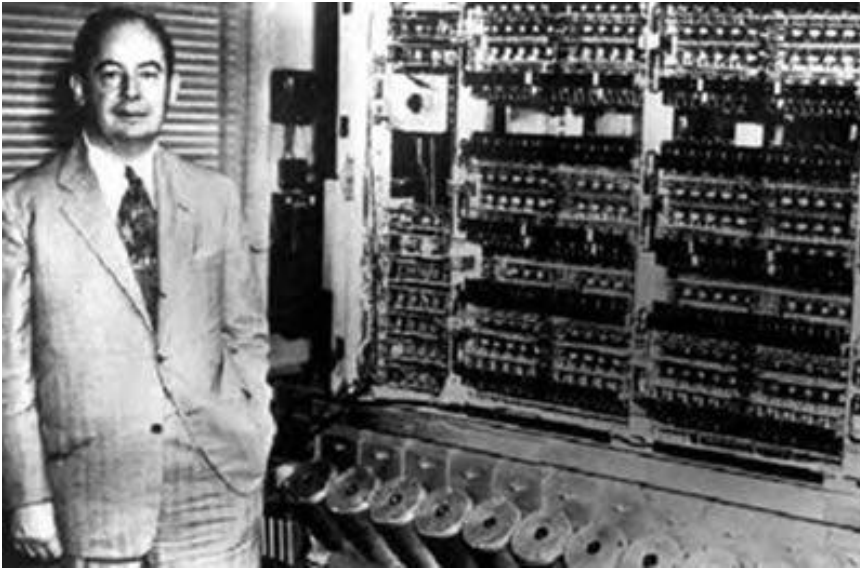
John von Neumann

One of History's *Hottest* CPU Microchips

Intel's Itanium 2

The numbers …

- 0.5 billion transistors in 120nm CMOS
- 1.6GHz clock, 64-bit instruction, 9MB L3 cache, 6.4GB/s I/O
- 2553 SPECfp_base2000 (30% faster than 2.8GHz P4)
- 130 Watts

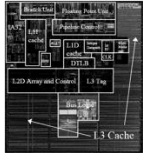## … and what they mean

Faster/cooler:

- *Scientific computing*
- *Database search*
- *Web surfing*
- *Video games*

What about intelligence?

Chips and Brains

- **Itanium:**
  - $3 \cdot 10^9$ floating op/s
    - *$5 \cdot 10^8$ transistors*
    - *$2 \cdot 10^9$ Hz clock*
  - 10^{10} Hz memory I/O
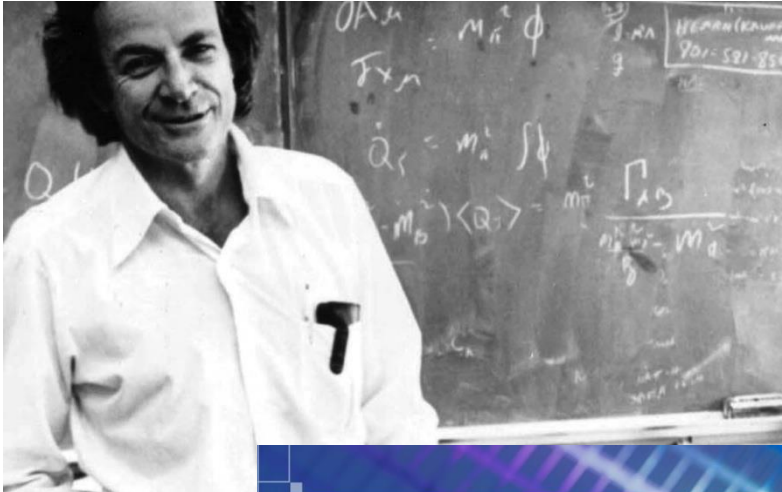   - *128-b data bus @ 400MHz*
  - 130 Watts

- **Human brain:**
  - 10^{15} synaptic op/s
    - *10^{15} synapses*
    - *1 Hz average firing rate*
  - 10^{10} Hz sensory/motor I/O
    - *10^8 nerve fibers*
  - 25 Watts

- **Silicon technology is approaching the *raw* computational power and bandwidth of the human brain.**

- **However, to emulate brain intelligence with chips requires a radical paradigm shift in computation:**
  - Distributed representation in massively parallel architecture
    - *Local adaptation and memory*
    - *Sensor and motor interfaces*
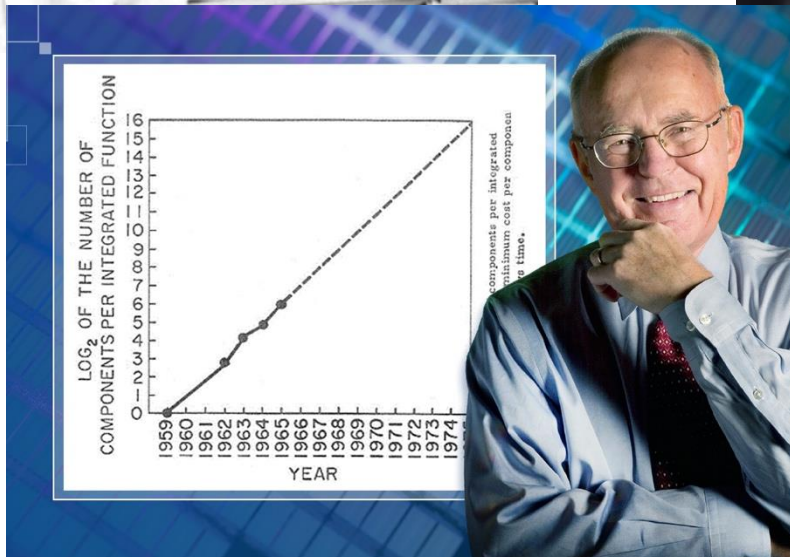 - Physical foundations of computing

The Nanoscale Systems Revolution
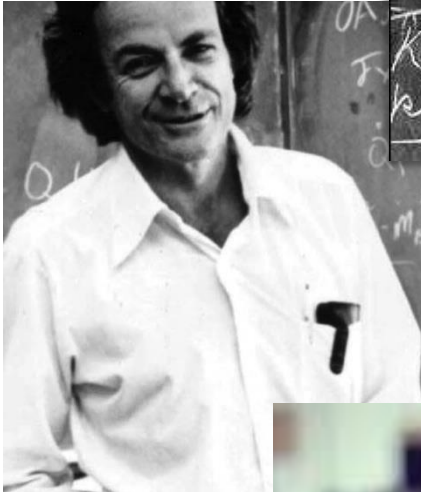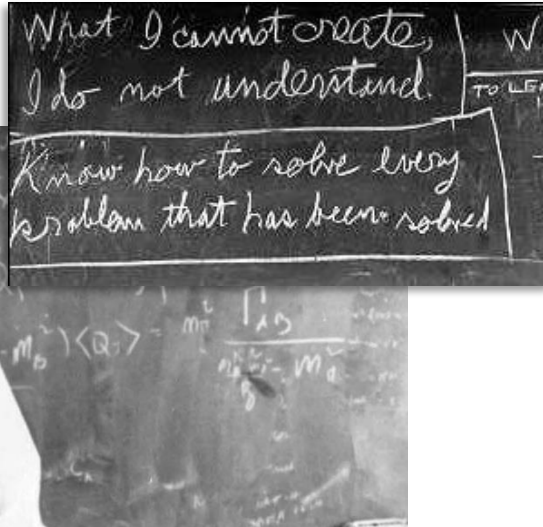

Richard Feynman
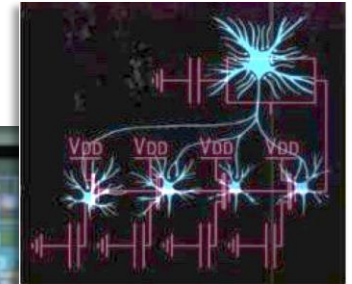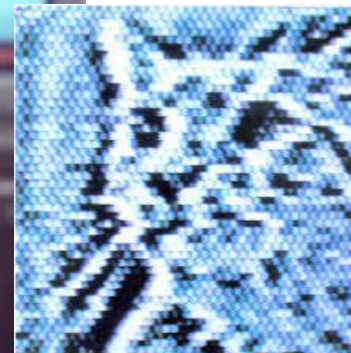

Carver Mead

Gordon Moore

Analysis by Synthesis

What I cannot create, I do not understand.

Know how to solve every problem that has been solved.

Richard Feynman

Carver Mead

Misha Mahowald

NICE 2024

https://niceworkshop.org/nice-2024/

Computational Systems Neuroscience

Analysis

Synthesis

Brain 1 m

Systems

Maps 1 cm

Networks

Neurons 100 μm

V_{Pre}

$E_{Reversal}$ V_{Post}

Synapses 1 μm

$C_{Membrane}$

Pre   Post

Membrane

Ion channel

Channels 10 nm

Source   Gate   Drain

MOSFET channel

Carriers 1 Å

Energy

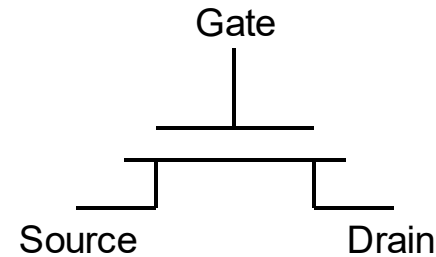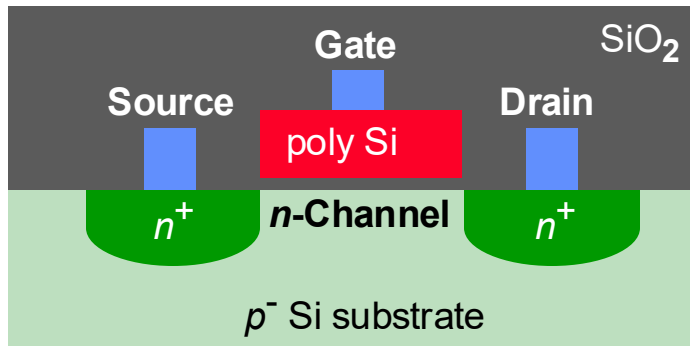Gate voltage

Neuromorphic Systems Engineering
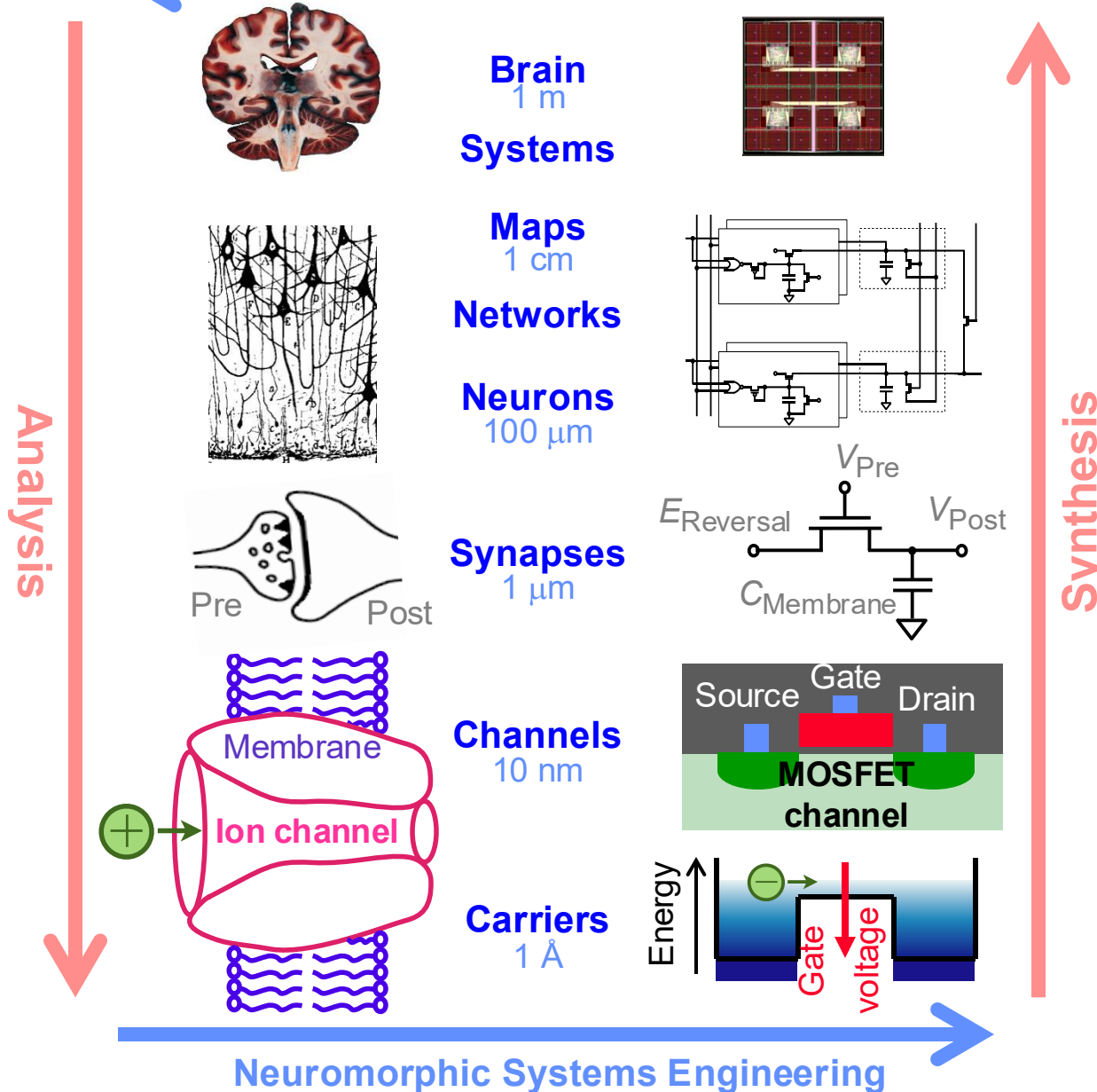
Multi-scale levels of investigation in analysis of the central nervous system (adapted from Churchland and Sejnowski 1992) and corresponding neuromorphic synthesis of highly efficient silicon cognitive microsystems. Boltzmann statistics of ionic and electronic channel transport provide isomorphic physical foundations.
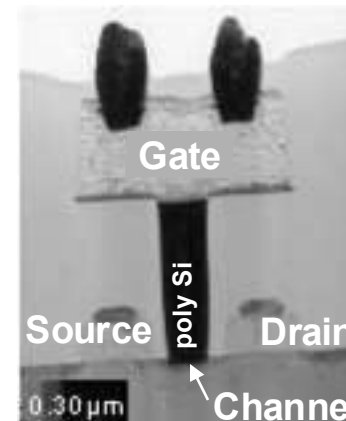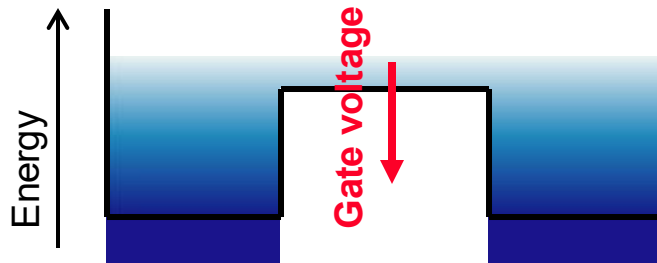
G. Cauwenberghs, "Reverse Engineering the Cognitive Brain," *PNAS*, 2013

Physics of Computation

CMOS Silicon Technology

Voltage-dependent *n*-channel
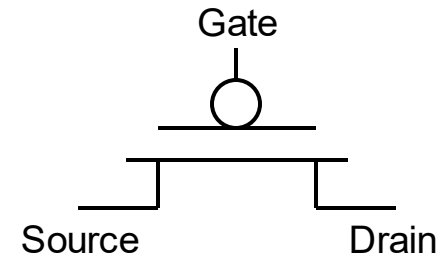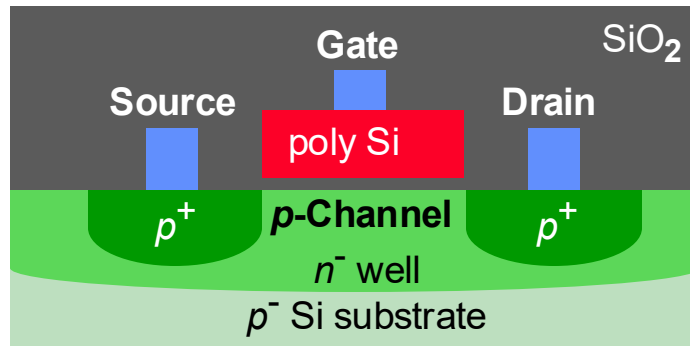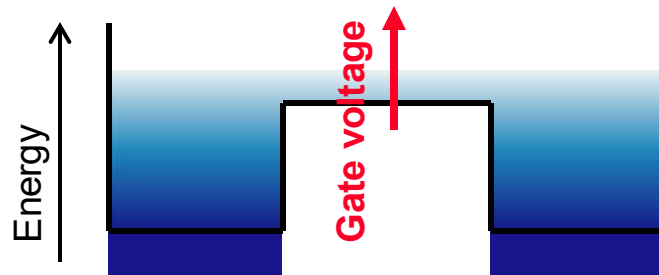
– *Electron* transport between source and drain

– Gate controls energy barrier for electrons across the channel

– Boltzmann distribution of *electron energy* produces exponential *increase* in channel conductance with gate voltage

nMOS transistor circuit symbol

Cross-section of nMOS transistor in 0.18μm CMOS process (Intel, 2002)

Physics of Computation

CMOS Silicon Technology

pMOS transistor circuit symbol

Voltage-dependent *p*-channel

- *Hole* transport between source and drain
- Gate controls energy barrier for holes across the channel
- Boltzmann distribution of *hole energy* produces exponential *decrease* in channel conductance with gate voltage

Physics of Neural Computation

Silicon and Lipid Membranes
Mead, 1989
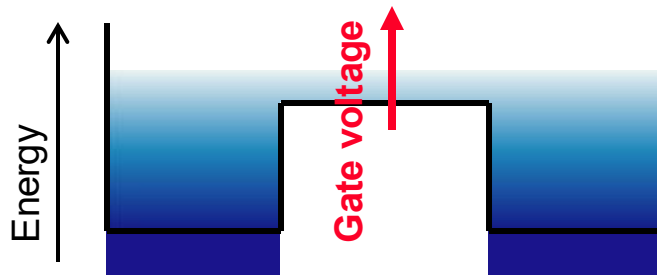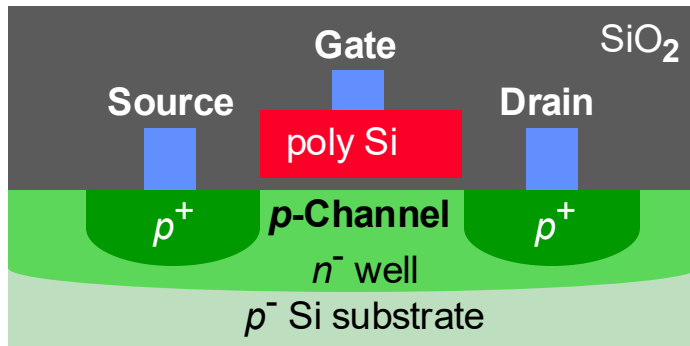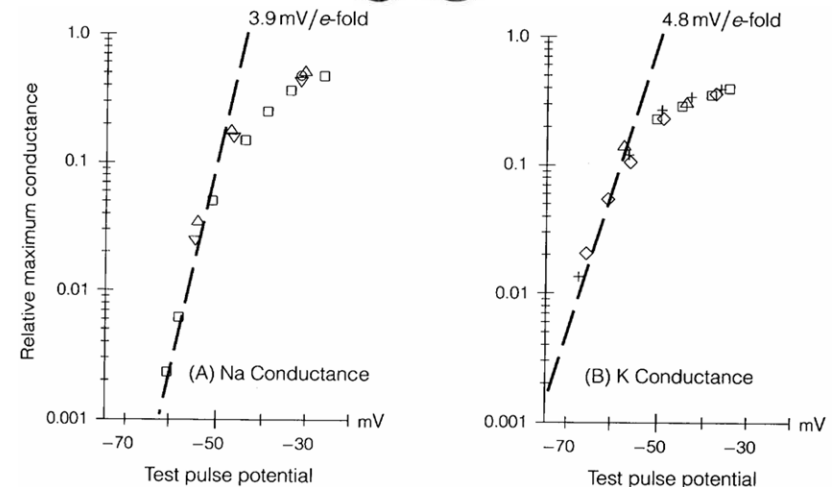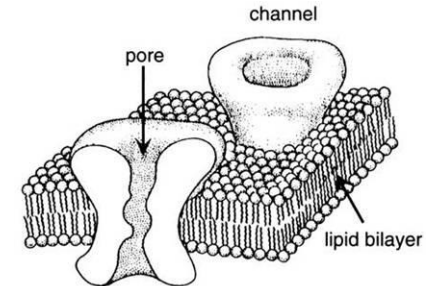

Squid giant axon (Hodgkin and Huxley, 1952)

Voltage-dependent *p*-channel

- *Hole* transport between source and drain
- Gate controls energy barrier for holes across the channel
- Boltzmann distribution of *hole energy* produces exponential *decrease* in channel conductance with gate voltage
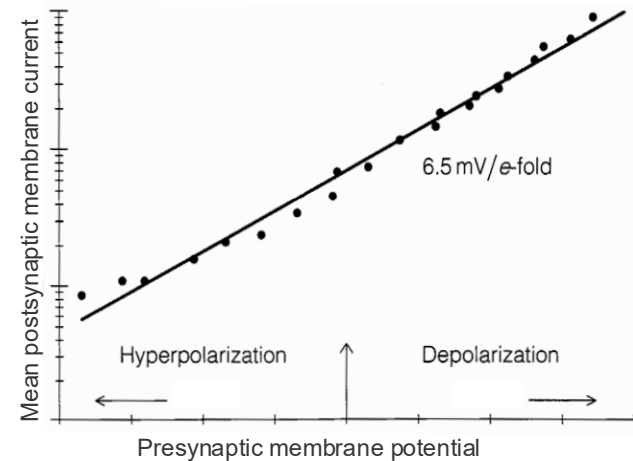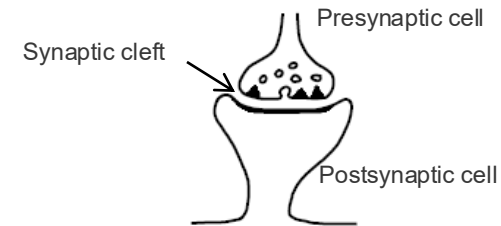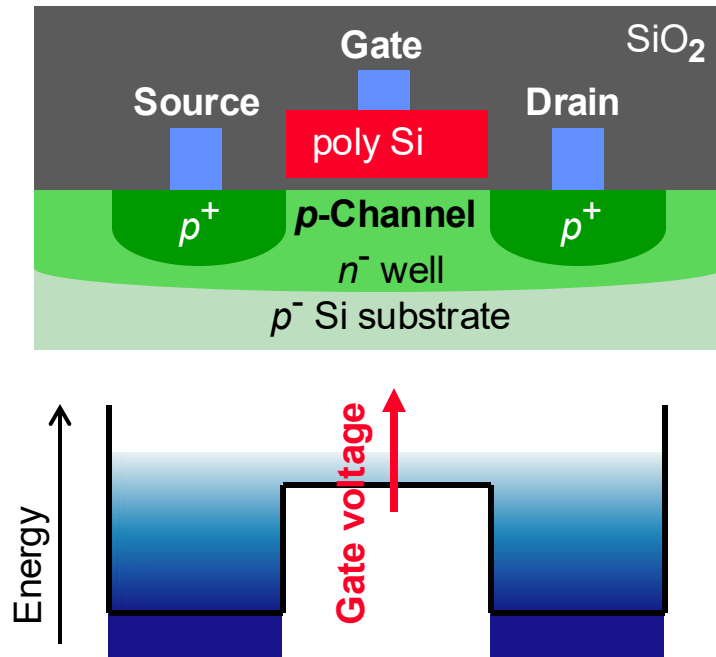
Voltage-dependent conductance

- K^+/Na^+ transport across lipid bilayer
- Membrane voltage controls energy barrier for opening of ion-selective channels
- Boltzmann distribution of *channel energy* produces exponential increase in K^+/Na^+ conductance with membrane voltage

Physics of Neural Computation

Silicon and Biochemical Synapses
Mead, 1989

(from Shepherd 1979)

Voltage-dependent *p*-channel

– *Hole* transport between source and drain

– Gate controls energy barrier for holes across the channel

– Boltzmann distribution of *hole energy* produces exponential *decrease* in channel conductance with gate voltage

Voltage-dependent quantal release

– K^+/Na^+ through postsynaptic membrane

– Presynaptic membrane voltage controls energy barrier for neurotransmitter release

– Boltzmann distribution in *quantal release energy* produces exponential dependence of postsynaptic K^+/Na^+ conductance

Why Develop "Neural" Silicon Chips?

Biology Motives:

- *In silico* emulation of neural and sensory-motor systems
  - *Real-time computational power*
  - *Accounts for noise and imprecision in neural elements*
- Analysis by synthesis
  - *Emulating form and structure of neural systems provides better understanding, accounting for physical and architectural constraints*
- Interfacing silicon with neurons and synapses *in vivo*
  - *Allows to observe and control neural and synaptic activity*

Engineering Motives:

- Efficiency of implementation
  - *Lower power, smaller size*
- Real-world interface
  - *Integrated sensors and actuators*
  - *Analog, continuous-time dynamics*
  - *Intelligent brain-machine interfaces!*

Neuromorphic Systems Design Flow

Neural Model

Circuit Design and Simulation

Chip Layout

Microfabrication

Microchip(s)

http://www.mosis.org

Chip Testing

System Integration

Neuromorphic System
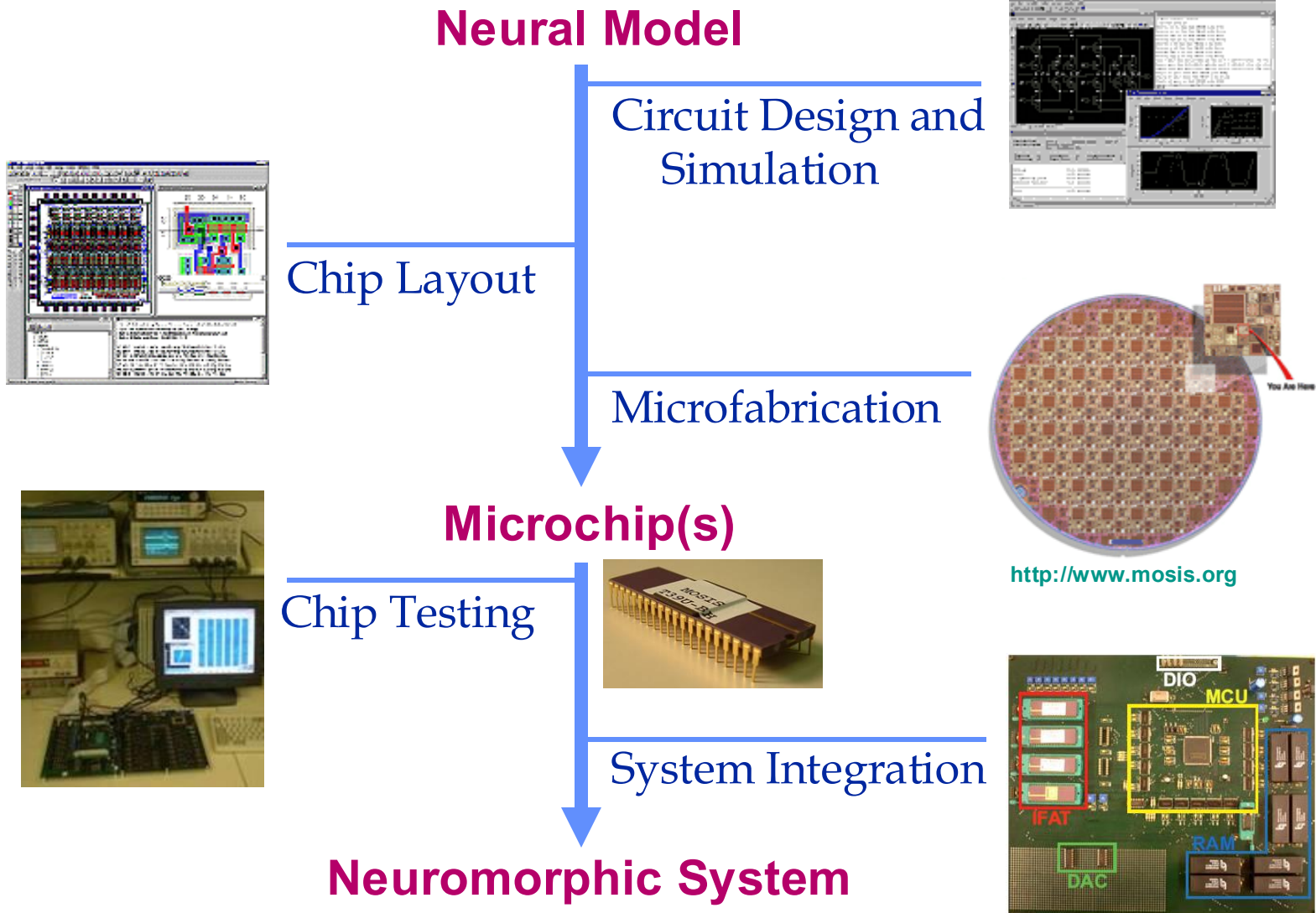
Silicon Model of Visual Cortical Processing

V2

6

Bipole cells (diffusive network)

2

3

V1

4

Complex and hypercomplex cells (lateral inhibition)

6

LGN

Optic Nerve

C_z C_y

I_z I_y
I_0 I_0

C_x I_x C_0 I_0 C_x
I_0 I_0

I_y I_0 I_0 I_x

C_y L_z C_z

88 transistors/pixel (including photodetector)
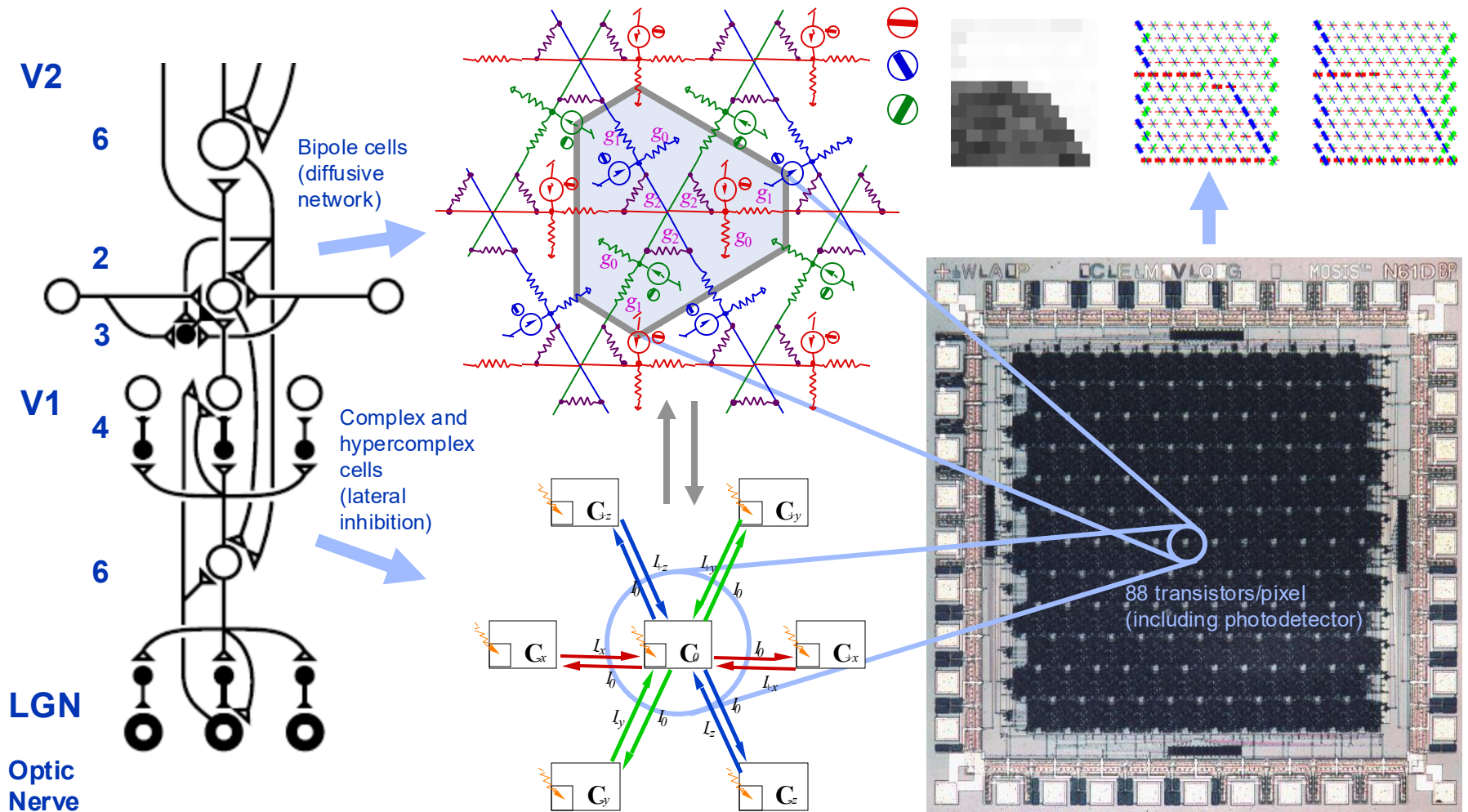
Neural model of boundary contour representation in V1, one orientation shown (Grossberg, Mingolla, and Williamson, 1997)

Single-chip focal-plane implementation (Cauwenberghs and Waskiewicz, 1999)

# Event-Coding Silicon Retina
Zaghloul and Boahen, 2006
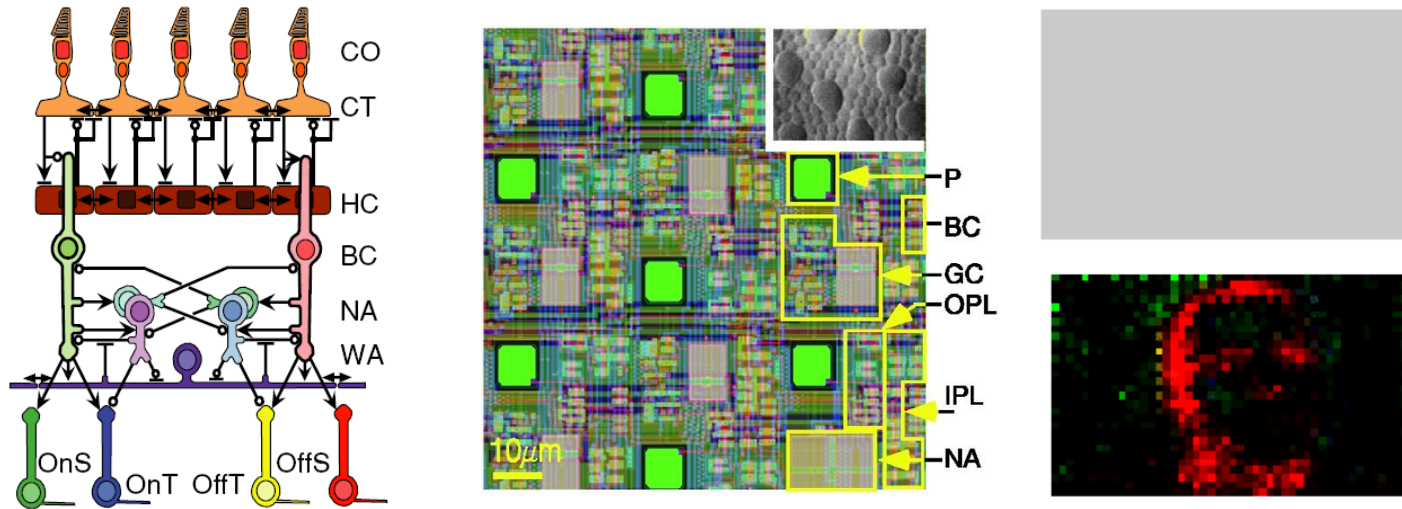
- – Models coding and communication of visual events in the mammalian retina and optic nerve
  - *Integrated photosensors (rods)*
  - *On and off transient and sustained ganglia cell outputs*
    - *Spatiotemporal compressed coding and communication in optic nerve*
    - *Address-event coding of spikes*

Change Threshold Detection APS CMOS Imager

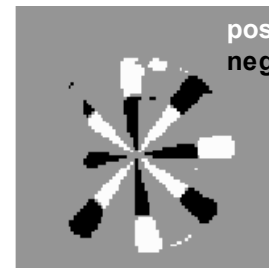*Chi, Mallik, Clapp, Choi, Cauwenberghs and Etienne-Cummings (2007)*

DDS / Event Coding

90 x 90
TD-APS
Array

FIFO
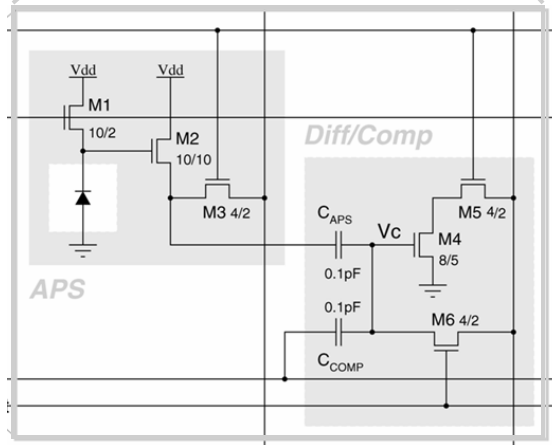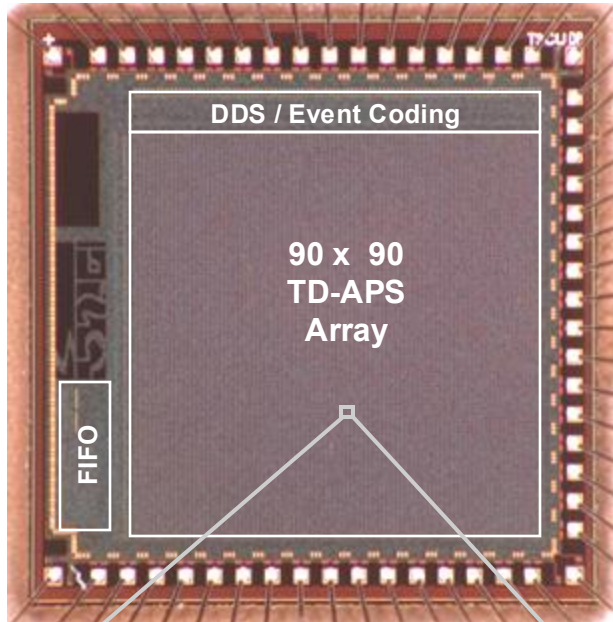
– Event-driven video compression

  • *Change detection and threshold encoding on the focal plane*

– 6T pixel combines APS and change event coding
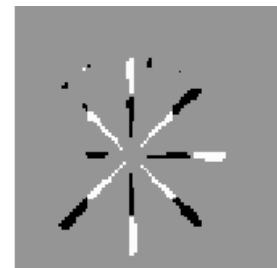
– 4.3mW power at 3V and 30fps

Diff/Comp

Vdd Vdd

M1
10/2

M2
10/10

M3 4/2

M5 4/2

C_APS   Vc

M4
8/5

0.1pF

0.1pF

M6 4/2

C_COMP

APS

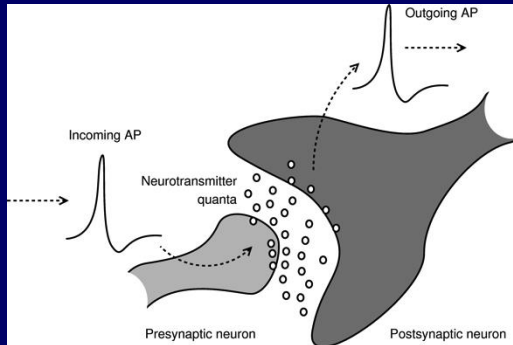*Fast Rotation*   *Slow Rotation*

pos.
neg.

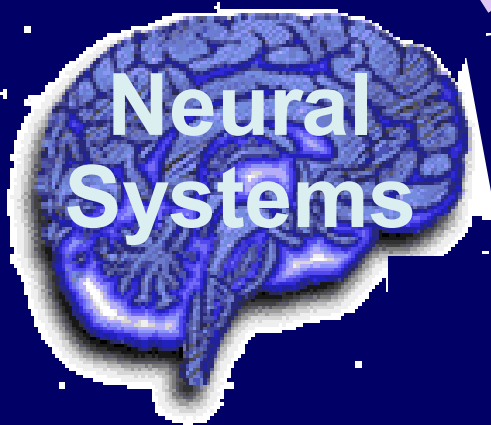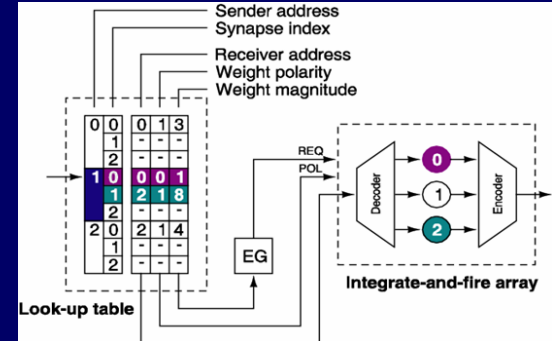*Video Out*   *Change Events Out*

Reconfigurable Synaptic Connectivity and Plasticity
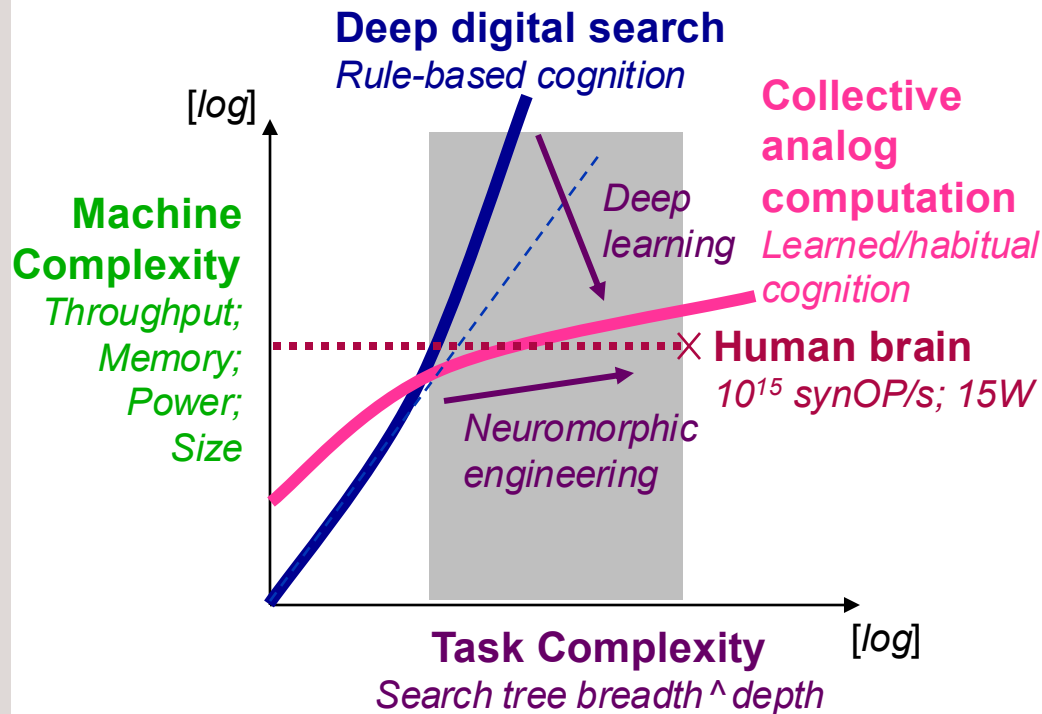## *From Microchips to Large-Scale Neural Systems*

Address-Event Representation

Neural Systems

Synaptic Plasticity & Wiring

Multi-Chip Systems
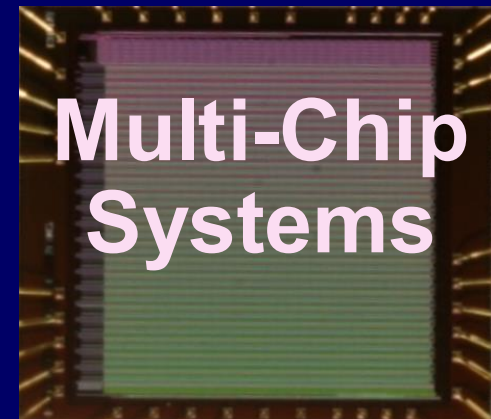
Scaling of Task and Machine Complexity

Deep digital search
Rule-based cognition

[*log*]

Machine Complexity
Throughput; Memory; Power; Size

Deep learning

Collective analog computation
Learned/habitual cognition

× **Human brain**
10^{15} synOP/s; 15W

Neuromorphic engineering
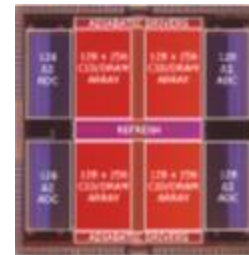
Task Complexity
Search tree breadth ^ depth

[*log*]

G. Cauwenberghs, "Reverse Engineering the Cognitive Brain," *PNAS*, 2013

Task Energy Efficiency:

$$\frac{Energy}{Task} =$$

$$\frac{Energy}{Operation} \quad , \quad \frac{Operations}{Task}$$

$$\frac{1\ fJ}{SynOp} \quad vs. \quad \frac{10\ pJ}{MAC}$$

$$\frac{10^{10}\ SynOps \ vs. \ 10^{11}\ MACs}{MNIST\ @\ 95\%}$$

Adiabatic CID-DRAM SVM (Kerneltron)
R. Karakiewicz et al, 2013
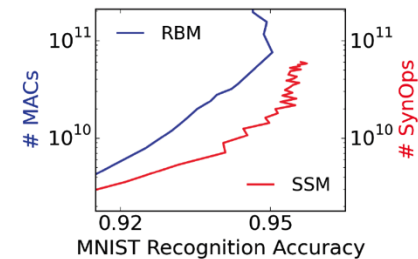
Synaptic Sampling Machine (SSM)
E. Neftci et al, 2016

Achieving (or surpassing) human-level machine intelligence requires a convergence between:

- *Advances in computing resources approaching connectivity and energy efficiency levels of computing and communication in the brain;*

- *Advances in deep learning methods, and supporting data, to adaptively reduce algorithmic complexity.*

Scaling and Complexity Challenges

- **Scaling the event-based neural systems to performance and efficiency approaching that of the human brain will require:**

  - Scalable advances in silicon integration and architecture

    EE NanoE Phys

    - *Scalable, locally dense and globally sparse interconnectivity*
      - *Hierarchical address-event routing*
    - *High density (10^{12} neurons, 10^{15} synapses within 5L volume)*
      - *Silicon nanotechnology and 3-D integration*
    - *High energy efficiency (10^{15} synOPS/s at 15W power)*
      - *Adiabatic switching in event routing and synaptic drivers*

  - Scalable models of neural computation and synaptic plasticity

    Neuro CS CogSci

    - *Convergence between cognitive and neuroscience modeling*
    - *Modular, neuromorphic design methodology*
    - *Data-rich, environment driven evolution of machine complexity*

Large-Scale Reconfigurable Neuromorphic Computing
Technology and Performance Metrics

	Stromatias 2013 SpiNNaker Manchester	Davies 2018 Loihi Intel	Merolla 2014 TrueNorth IBM	Schemmel 2010 FACETS/BrainScaleS Heidelberg	Benjamin 2014 NeuroGrid Stanford	Park 2014 IFAT UCSD
Technology (nm)	130	14	28	180	180	90
Die Size (mm^2)	102	60	430	50	168	16
Neuron Type	Digital Arbitrary	Digital Conductance Integrate & Fire	Digital Accumulate & Fire	Analog Conductance Integrate & Fire	Analog Shared-Dendrite Conductance I&F	Analog 2-Compartment Conductance I&F
# Neurons	5216 [1]	128k [2]	1M [2]	512	65k	65k
Neuron Area (μm^2)	N/A [1]	240 (240k) [2]	14 (3325) [2]	1500	1800	140
Peak Throughput (Events/s)	5M	3.4G	1G	65M	91M	73M
Energy Efficiency (J/SynEvent)	8n	24p	26p	N/A	31p	22p

[1] Software-instantiated neuron model
[2] Time-multiplexed neuron processor

Benjamin, B., P. Gao, E. McQuinn, S. Choudhary, A. Chandrasekaran, J. Bussat, R. Alvarez-Icaza, J. Arthur, P. Merolla, and K. Boahen, "Neurogrid: A mixed analog-digital multichip system for large-scale neural simulations," *Proc. IEEE*, 102(5):699–716, 2014.

Davies, M. et al., "Loihi: A Neuromorphic Manycore Processor with On-Chip Learning," *IEEE Micro*, vol. 38 (1), pp. 82-99, 2018.

Merolla, P.A., J.V. Arthur, R. Alvarez-Icaza, A S. Cassidy, J. Sawada, F. Akopyan, B.L. Jackson, N. Imam, C. Guo, Y. Nakamura, B. Brezzo, I. Vo, S.K. Esser, R. Appuswamy, B. Taba, A. Amir, M.D. Flickner, W.P. Risk, R. Manohar, and D. S. Modha, "A million spiking-neuron integrated circuit with a scalable communication network and interface," *Science*, 345(6197):668–673, 2014.

Park, J., S. Ha, T. Yu, E. Neftci, and G. Cauwenberghs, "65k-neuron 73-Mevents/s 22-pJ/event asynchronous micro-pipelined integrate-and-fire array transceiver," *Proc. 2014 IEEE Biomedical Circuits and Systems Conf. (BioCAS)*, 2014.

Schemmel, J., D. Bruderle, A. Grubl, M. Hock, K. Meier, and S. Millner, "A waferscale neuromorphic hardware system for large-scale neural modeling," *Proc. 2010 IEEE Int. Symp. Circuits and Systems (ISCAS)*, 1947–1950, 2010.

Stromatias, E., F. Galluppi, C. Patterson, and S. Furber, "Power analysis of largescale, real-time neural networks on SpiNNaker," *Proc. 2013 Int. Joint Conf. Neural Networks (IJCNN)*, 2013.
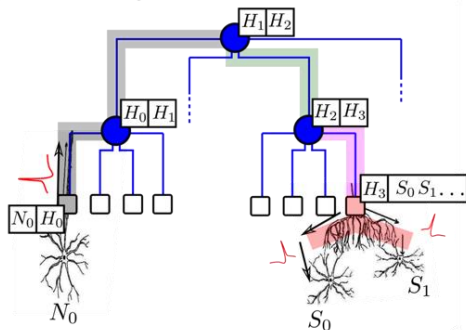
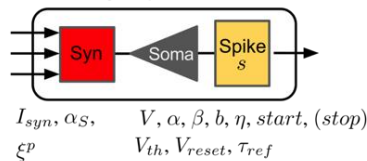# Large-Scale Reconfigurable Neuromorphic Computing

Provides open access to large-scale reconfigurable neuromorphic computing hardware and software as an experimental testbed and development platform with up to 128M neurons and 32B synapses for the research community at large.

(b) Connectivity Model

(c) HiAER Tree

(d) HiAER Node

(a) Neuron and Synapse Model

$I_{syn}, \alpha_S, \qquad V, \alpha, \beta, b, \eta, start, (stop)$
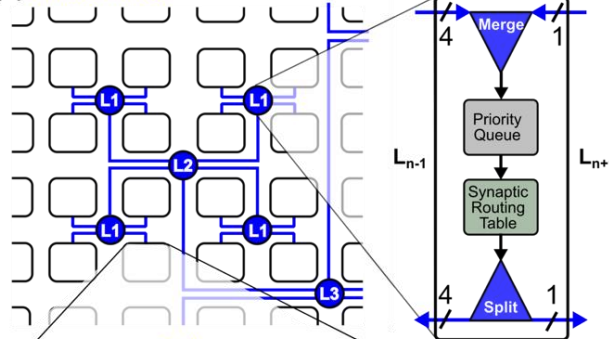$\xi^p \qquad\qquad V_{th}, V_{reset}, \tau_{ref}$

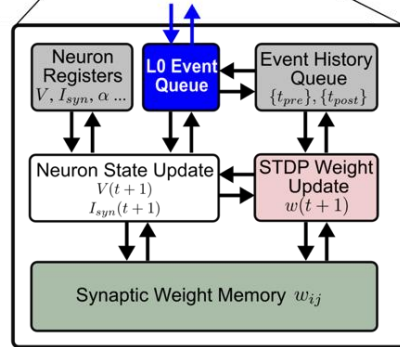$$V_i(t+1) = \alpha V_i(t) + \beta(b_i + I_{syn,i}(t) + \sigma_i \eta_i(t)),$$

$$I_{syn,i}(t+1) = \alpha_S I_{syn,i}(t) + \sum_j \xi_{ij}^p w_{ij} s_j (t - \theta_{ij}),$$

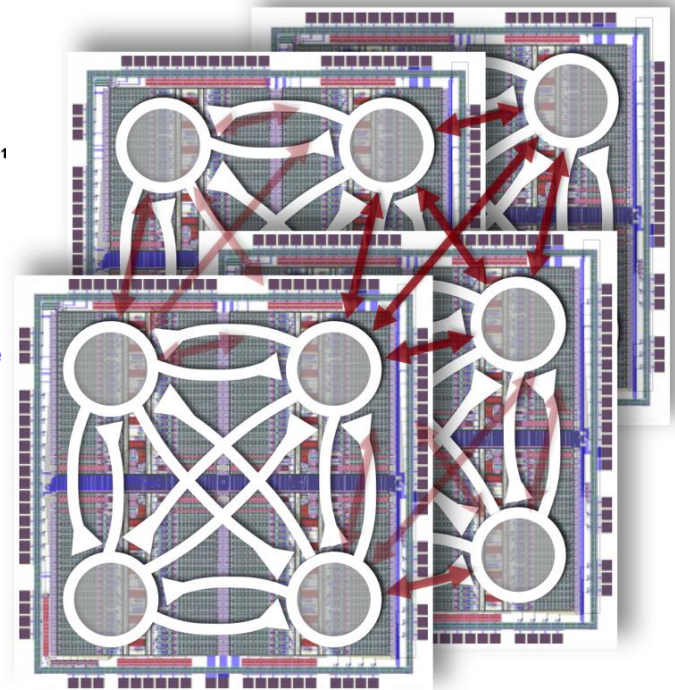$$\Delta w_{ij}(t) = g(t) \left(s_j(t) e_i^{post}(t) + s_i(t) e_j^{pre}(t) \right)$$

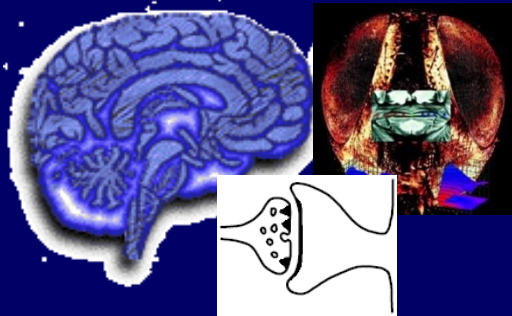**(e) NSAT Core**

Neural-Synaptic Array Transceiver (Detorakis et al, Frontiers in Neuroscience, 2018)
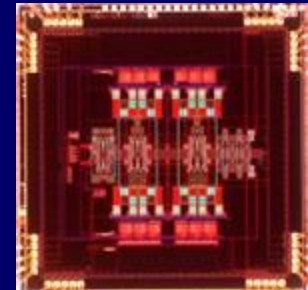
NeuroDyn (2021 Telluride Neuromorphic Workshop)

Closing the Loop: Interactive Neural/Artificial Intelligence
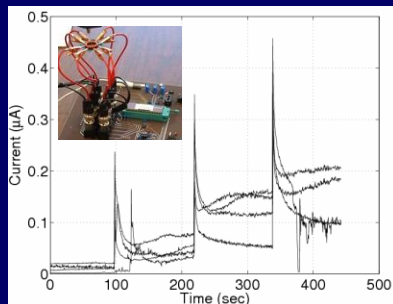

Neuromorphic Engineering

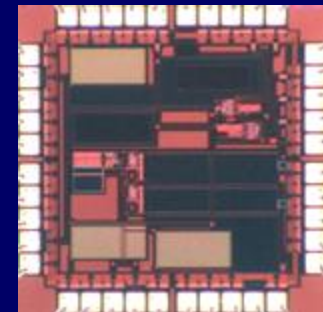Adaptive Sensory Feature Extraction and Pattern Recognition

Neuro Bio

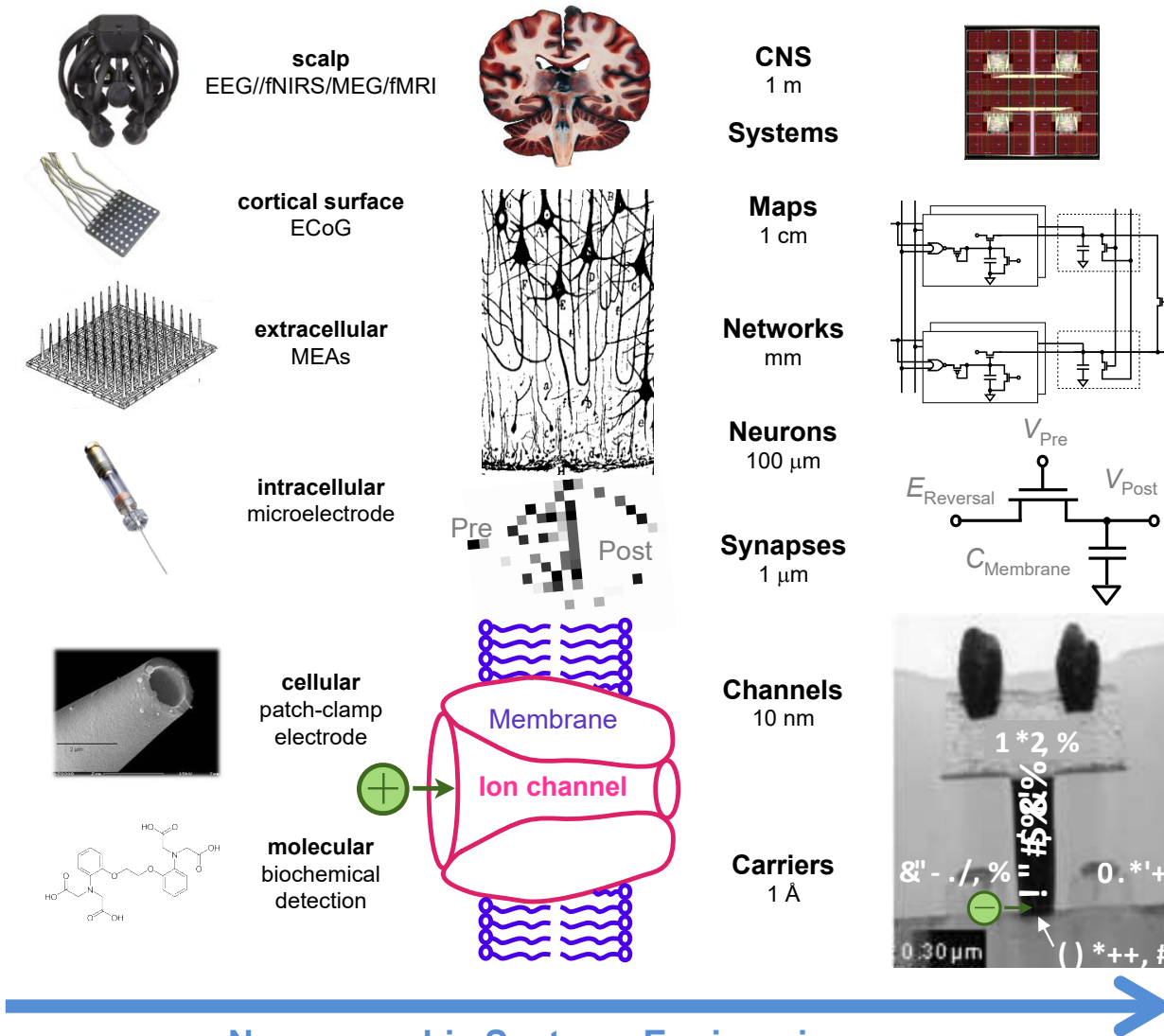Learning & Adaptation

Micropower Mixed-Signal VLSI

Neurosystems Engineering

Biosensors, Neural Prostheses and Brain Interfaces

Computational Systems Neuroscience

Analysis

Synthesis

scalp EEG//fNIRS/MEG/fMRI	**CNS** 1 m	
	Systems	
cortical surface ECoG	**Maps** 1 cm	
extracellular MEAs	**Networks** mm	
intracellular microelectrode	**Neurons** 100 μm	
Pre Post	**Synapses** 1 μm	
cellular patch-clamp electrode	**Channels** 10 nm	
molecular biochemical detection	**Carriers** 1 Å	

Membrane

Ion channel

V_{Pre}

$E_{Reversal}$ V_{Post}

$C_{Membrane}$

1 *2, %

&" - ./, % = . #$%&' i

0. *'+%

0.30 μm

() *++, #%

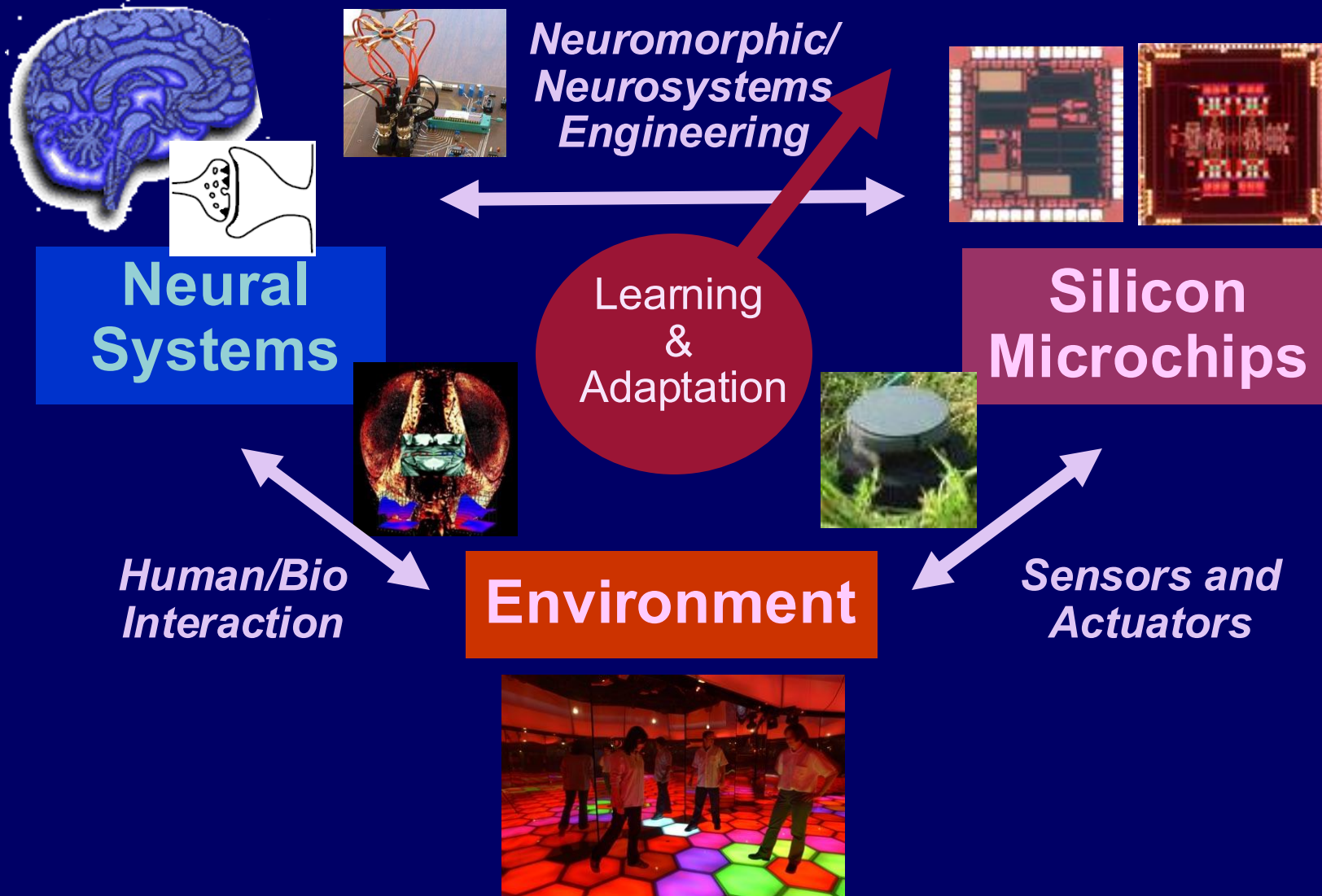**Neuromorphic Systems Engineering**

F. Broccard, S. Joshi, J. Wang and G Cauwenberghs, "Neuromorphic neural interfaces: from neurophysiological inspiration to biohybrid coupling with nervous systems," *JNE*, 2017

Integrated Systems Neuroengineering

*Neuromorphic/ Neurosystems Engineering*

Neural Systems

Learning & Adaptation

Silicon Microchips

Human/Bio Interaction

Environment

Sensors and Actuators

Silicon Neurons

Hodgkin-Huxley neuronal dynamics

Integrate-and-fire models

Action potentials as address events

Nernst Potentials

intracellular — extracellular

$[K^+]_i$ $[K^+]_o$

V_i V_o

$$V_m = V_i - V_o$$

membrane potential
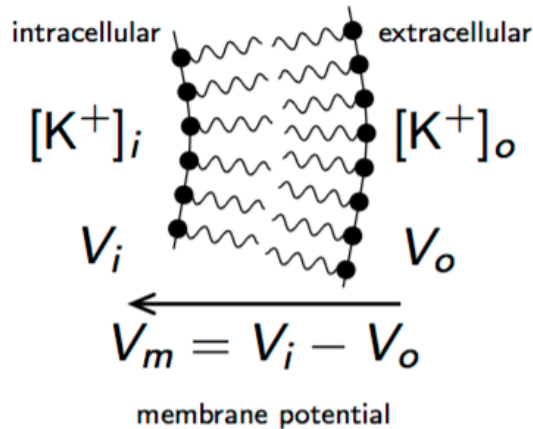
density ratio / energies per molecule / energies per mol

$$\frac{[K^+]_o}{[K^+]_i} = \frac{n_o}{n_i} = e^{-\frac{\mathcal{E}_o - \mathcal{E}_i}{kT}} \quad \left(= e^{-\frac{U_o - U_i}{RT}}\right)$$

Boltzman constant   absolute temperature   gas constant

$$= e^{-\frac{V_o - V_i}{kT/q}}$$

charge per molecule
$= 1.6 \ 10^{-19} C$ per valence index

$$\Rightarrow E_{rest} = V_m|_{equilibrium} = \underbrace{\frac{kT}{q}}_{\text{25mV @ room T}} \ln \frac{[K^+]_o}{[K^+]_i}$$

$$= \underbrace{\frac{kT}{q} \ln 10}_{\text{62mV @ room T}} \ \log_{10} \frac{[K^+]_o}{[K^+]_i}$$

$\mathcal{E}$ energy — Boltzman "tail" — T — Fermi level — n density
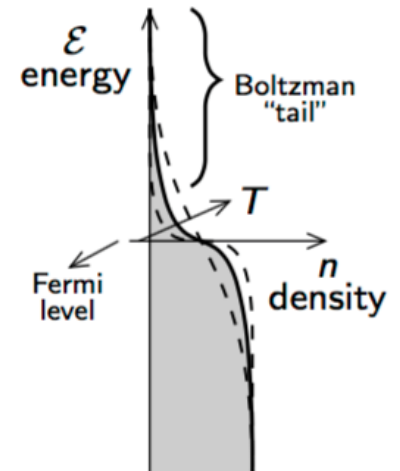
Ion	Extracellular concentration (mM)	Intracellular concentration (mM)	$\frac{Ion_o}{Ion_i}$	Equilibrium potential[a] (mV)
Na^+	145	12	12	+67
K^+	4	155	0.026	−98
Ca^{2+}	1.5	100 nM	15,000	+129
Cl^-	123	4.2[b]	29[b]	−90[b]

Nernst-Planck Equilibrium
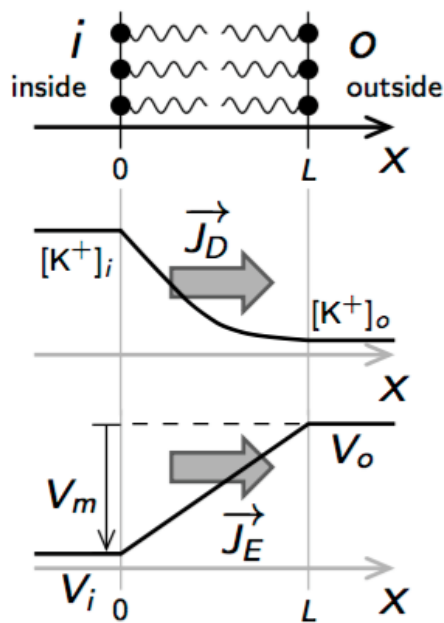
Equilibrium between **diffusion** and **drift**:

(chemical)   (electrical)

Diffusion: $\vec{J_D} = qD \cdot \left(-\vec{\nabla}[\text{K}^+]\right)$

Drift: $\vec{J_E} = q[\text{K}^+]\mu \cdot \vec{E} = q\mu[\text{K}^+]\left(-\vec{\nabla}V\right)$

$$\Rightarrow \vec{J_{\text{K}^+}} = \vec{J_D} + \vec{J_E} = 0 \quad \text{equilibrium}$$

$$\Rightarrow -qD\frac{d[\text{K}^+]}{dx} - q\mu[\text{K}^+]\frac{dV}{dx} = 0 \Rightarrow \frac{D}{\mu}\underbrace{\left(\frac{d[\text{K}^+]}{[\text{K}^+]}\right)}_{d\left(\ln[\text{K}^+]\right)} = -dV$$

$$\Rightarrow \frac{D}{\mu}\ln\frac{[\text{K}^+]_o}{[\text{K}^+]_i} = -(V_o - V_i) = V_m = E_{rest} \text{ with } \frac{D}{\mu} = \frac{kT}{q}$$

indeed, $D = \frac{kT}{q} \cdot \mu$

Dissipation-fluctuation

(Einstein)

BENG 260 Neurodynamics — http://isn.ucsd.edu/courses/beng260

Membrane Capacitance

capacitance = differential charge accumulation with voltage across insulator (membrane)

Charge Density ρ

Electric Field $\vec{E}$

$$\vec{\nabla} \cdot \vec{E} = \frac{\rho}{\varepsilon} \text{ , or } \frac{dE}{dx} = \frac{\rho}{\varepsilon}$$

Potential V

$$V_m = \frac{L}{\varepsilon} \frac{Q}{A} \qquad \vec{\nabla} V = -\vec{E} \text{ , or } \frac{dV}{dx} = -E$$

$$Q = C_m \cdot V_m \text{ with } C_m = \varepsilon \cdot \frac{A}{L} \qquad \frac{\varepsilon}{L} \approx 0.01 \text{ F/m}^2$$

Dynamics: I or $: C_m \frac{dV_m}{dt} = -I(V_m, \ldots)$
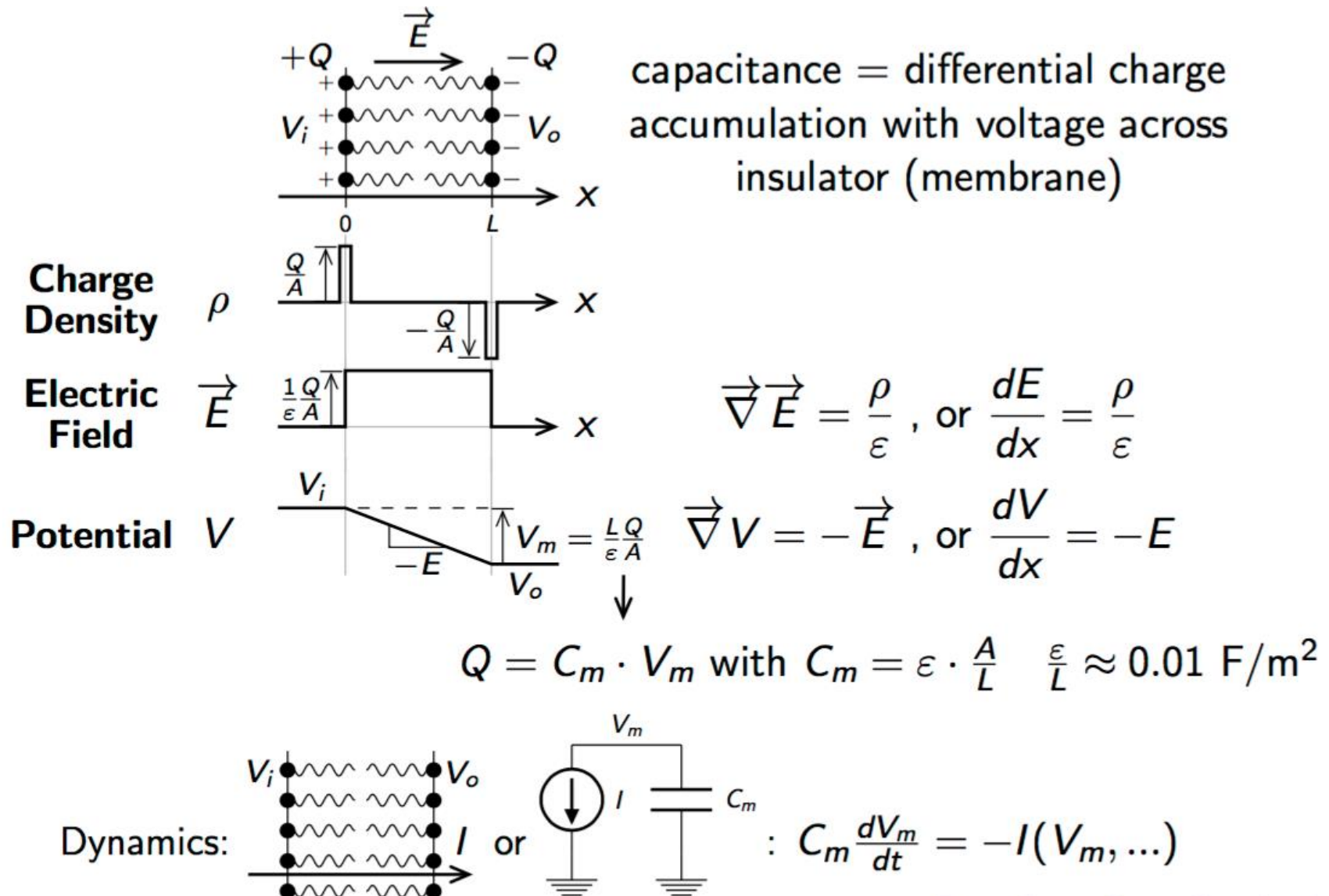
Membrane Conductance

K^+: current density $\vec{J_K} = -q\mu[K]\left(\frac{kT}{q}\vec{\nabla}\ln[K] + \vec{\nabla}V\right)$

$$\Downarrow$$

current $I_K \approx -q\mu\overline{[K]}\frac{A}{L}\left(\frac{kT}{q}\ln\frac{[K]_o}{[K]_i} + V_o - V_i\right) = g_K\left(V_m - E_K\right)$
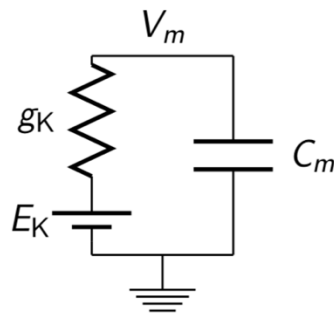
average concentration   membrane thickness   effective cross-section

$$\begin{cases} g_K = q\mu\overline{[K]}\frac{A}{L} \\ E_K = \frac{kT}{q}\ln\frac{[K]_o}{[K]_i} \end{cases}$$

Ohmic approximation

K^+, Na^+:
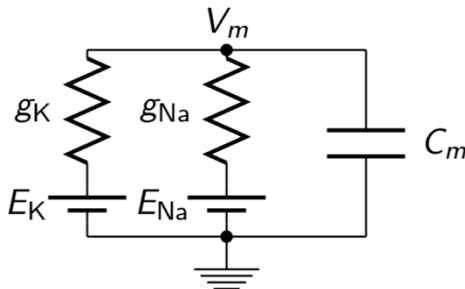
Equilibrium: $E_{rest} = V_m = \dfrac{g_K E_K + g_{Na} E_{Na}}{g_K + g_{Na}}$

Not quite...

$$E_{rest} = V_m = \frac{kT}{q}\ln\frac{\mu_K[K]_o + \mu_{Na}[Na]_o}{\mu_K[K]_i + \mu_{Na}[Na]_i}$$

BENG 260 Neurodynamics — http://isn.ucsd.edu/courses/beng260

Voltage Gated Ion Channels

n: *slow K+ activation;* **m**: *fast Na+ activation;* **h**: *slow Na+ inactivation*
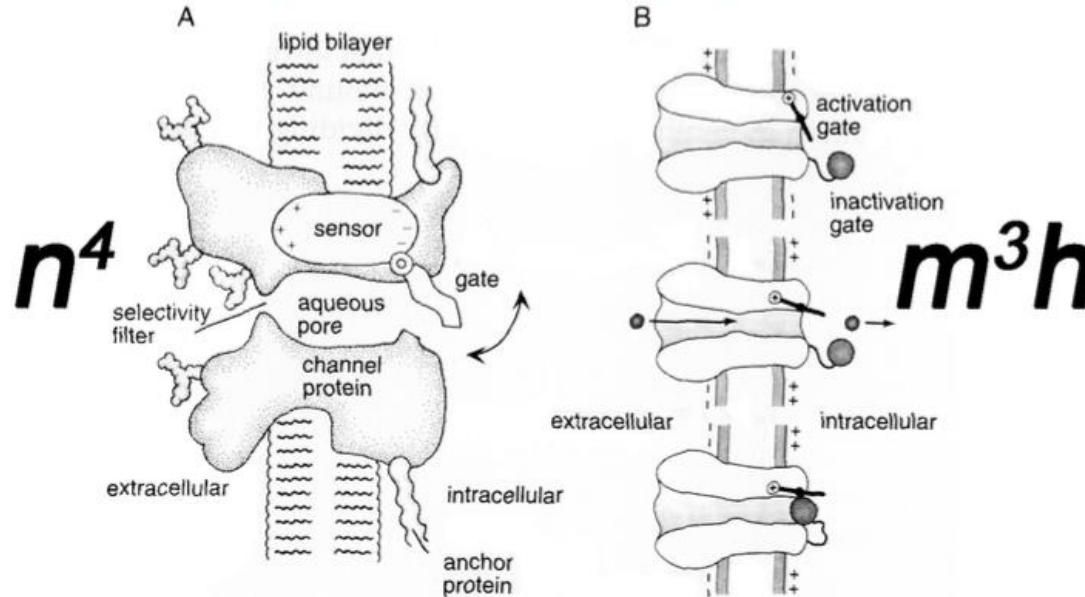
Figure 5.8 Gating of membrane channels. In both figures, the interior of the neuron is to the right of the membrane, and the extracellular medium is to the left. **(A)** A cartoon of gating of a persistent conductance. A gate is opened and closed by a sensor that responds to the membrane potential. The channel also has a region that selectively allows ions of a particular type to pass through the channel, for example, K+ ions for a potassium channel. **(B)** A cartoon of the gating of a transient conductance. The activation gat is coupled to a voltage sensor (denoted by a circled +) and acts like the gate in A. A second gate, denoted by the ball, can block that channel once it is open. The top figure shows the channel in a deactivated (and deinactivated) state. The middle panel shows an activated channel, and the bottom panel shows an inactivated channel. Only the middle panel corresponds to an open, ion-conducting state. (A from Hille, 1992; B from Kandel et al., 1991.)

Dayan & Abbott 2001, p. 169

Hodgkin-Huxley Model

Squid axon:

$$C_m \frac{dV_m}{dt} = I_{ext} \underbrace{- \bar{g}_K n^4 (V_m - E_K)}_{I_K} \underbrace{- \bar{g}_{Na} m^3 h (V_m - E_{Na})}_{I_{Na}} \underbrace{- g_L (V_m - E_L)}_{I_L}$$

$C_m = 1 \mu F / cm^2$

$E_K = -12\,mV$ $E_{Na} = 120\,mV$ $E_L = 10.6\,mV$

$\bar{g}_K = 36\,mS/cm^2$ $\bar{g}_{Na} = 120\,mS/cm^2$ $g_L = 0.3\,mS/cm^2$

$(mS = \mu A / mV)$

$$\frac{dn}{dt} = \alpha_n (1 - n) - \beta_n n = \frac{n_\infty - n}{\tau_n}; \quad \alpha_n (V_m) = \frac{10 - V_m}{100 \left(e^{1 - V_m/10} - 1 \right)}; \quad \beta_n (V_m) = \frac{1}{8} e^{-V_m/80}$$

$$\frac{dm}{dt} = \alpha_m (1 - m) - \beta_m m = \frac{m_\infty - m}{\tau_m}; \quad \alpha_m (V_m) = \frac{25 - V_m}{100 \left(e^{2.5 - V_m/10} - 1 \right)}; \quad \beta_m (V_m) = 4 e^{-V_m/18}$$

$$\frac{dh}{dt} = \alpha_h (1 - h) - \beta_h h = \frac{h_\infty - h}{\tau_h}; \quad \alpha_h (V_m) = \frac{7}{100} e^{-V_m/20}; \quad \beta_h (V_m) = \frac{1}{1 + e^{3 - V_m/10}}$$

α_x and β_x in units $1/ms$; V_m in units mV

* V_m slightly shifted by $65 mV$ so that $E_{rest} \equiv 0 mV$

Hodgkin & Huxley, 1952

Hodgkin-Huxley Model
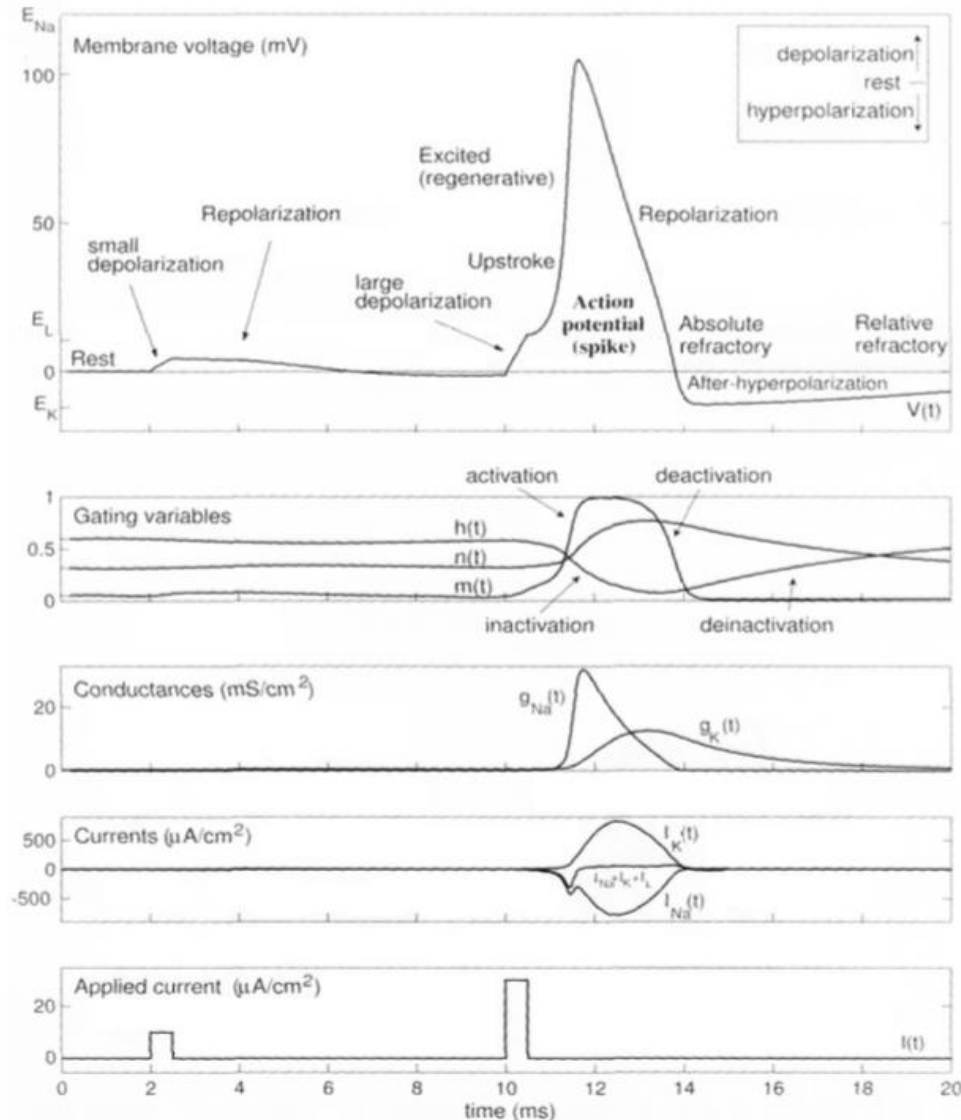
Izhikevich 2007,
p. 40

Postsynaptic Conductance

Postsynaptic membrane current and voltage:

$$C_m \frac{dV_m}{dt} = I_{ext} - I_\text{K} - I_\text{Na} - I_L - \sum_i I_{syn_i}$$

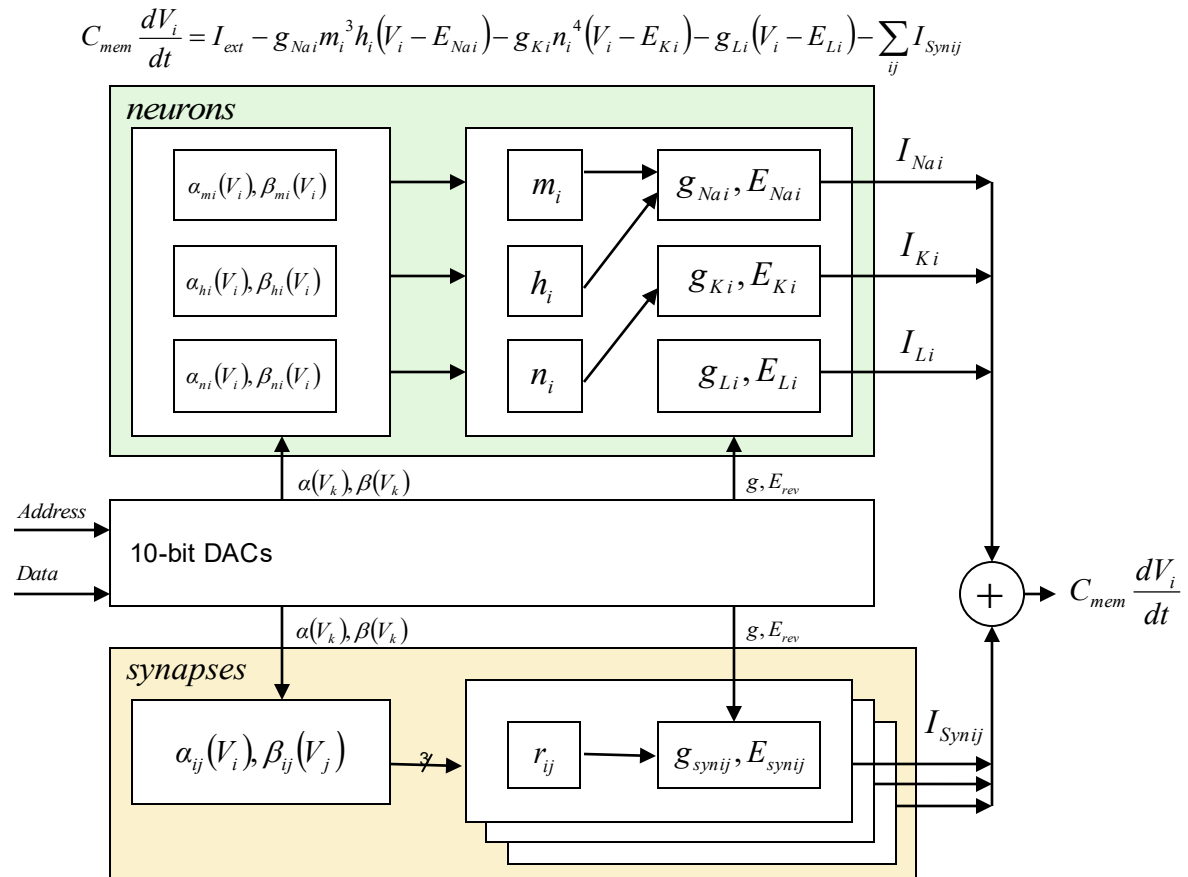$$I_{syn_i} = g_{syn_i}(t) \cdot (V_m - E_{syn_i})$$
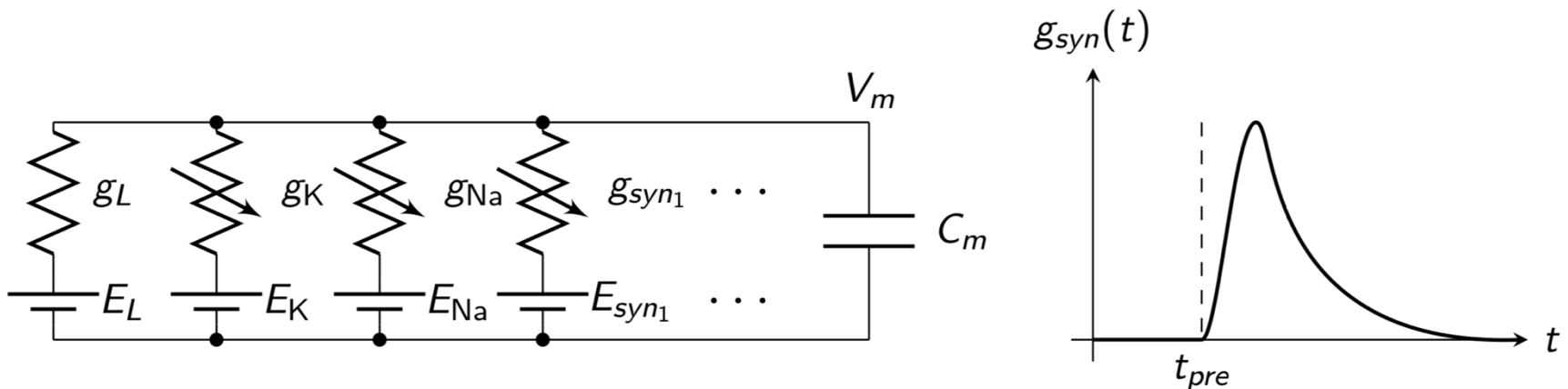
NeuroDyn: **Biophysical Neurodynamics in Analog VLSI**
Yu and Cauwenberghs 2009

Generalized Hodgkin-Huxley neural and conductance-based synapse membrane dynamics *in silico*:

$$C_{mem}\frac{dV_i}{dt} = I_{ext} - g_{Nai}m_i^3 h_i\left(V_i - E_{Nai}\right) - g_{Ki}n_i^4\left(V_i - E_{Ki}\right) - g_{Li}\left(V_i - E_{Li}\right) - \sum_{ij} I_{Synij}$$

opening rate

$$1-n \quad \overset{\alpha_n(V)}{\underset{\beta_n(V)}{\rightleftharpoons}} \quad n$$

Fraction of gates closed   *closing rate*   Fraction of gates open

$$\frac{dn}{dt} = \alpha_n(1-n) - \beta_n n$$

channel
pore
lipid bilayer
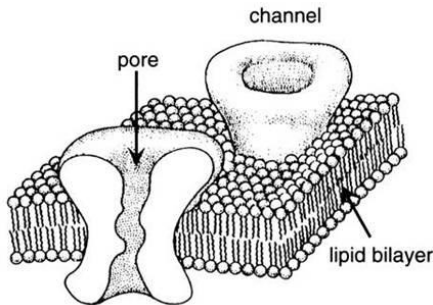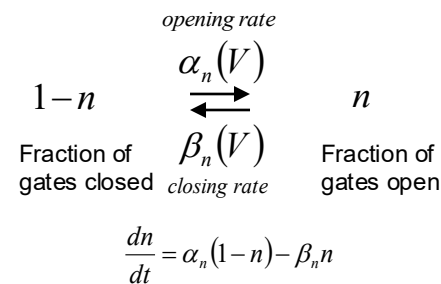
The *NeuroDyn* chip emulates detailed neural and synaptic dynamics in silicon by implementing rate-based models of voltage-gated and ligand-gated channel kinetics.

neurons

$\alpha_{mi}(V_i), \beta_{mi}(V_i)$	$\rightarrow$	m_i	$\rightarrow$	g_{Nai}, E_{Nai}	I_{Nai}
$\alpha_{hi}(V_i), \beta_{hi}(V_i)$	$\rightarrow$	h_i		g_{Ki}, E_{Ki}	I_{Ki}
$\alpha_{ni}(V_i), \beta_{ni}(V_i)$	$\rightarrow$	n_i		g_{Li}, E_{Li}	I_{Li}

$\alpha(V_k), \beta(V_k)$ g, E_{rev}

Address → **10-bit DACs**
Data →

$\alpha(V_k), \beta(V_k)$ g, E_{rev}

synapses

$\alpha_{ij}(V_i), \beta_{ij}(V_j)$ → γ → r_{ij} → g_{synij}, E_{synij} I_{Synij}

$$+ \rightarrow C_{mem}\frac{dV_i}{dt}$$

Each parameter is individually addressable and programmable through 10-bit DACs.

NeuroDyn: Biophysical Neurodynamics in Analog VLSI
Yu and Cauwenberghs 2009
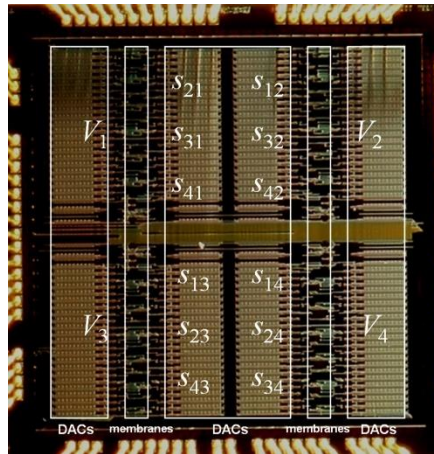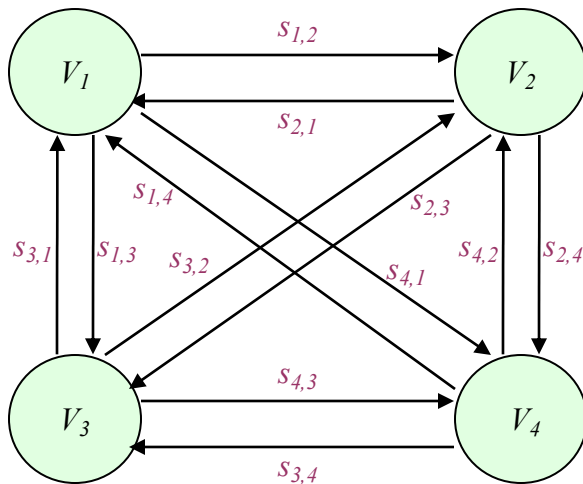
Programmable Parameters: 384 total

Neurons V_i

$\alpha_{n_i}(V)$	$\beta_{n_i}(V)$	g_{Na_i}	E_{Na_i}
m_i	m_i	K_i	K_i
h_i	h_i	L_i	L_i
4x3x7*	4x3x7*	4x3	4x3

Synapses s_{ij}

$\alpha_{r_{ij}}(V_{pre})$	$\beta_{r_{ij}}(V_{post})$	$g_{syn_{ij}}$	$E_{syn_{ij}}$
12x7*	12x7*	12	12

*All rates α, β are 7-point sigmoidal spline regression functions
$\alpha_.(V_k), \beta_.(V_k), \quad k = 1,\dots 7$

The *NeuroDyn* Board consists of 4 neurons fully connected through 12 synapses. All parameters are individually programmable and have biophysically-based parameters governing the conductances, reversal potentials, and voltage-dependance of the channel kinetics.
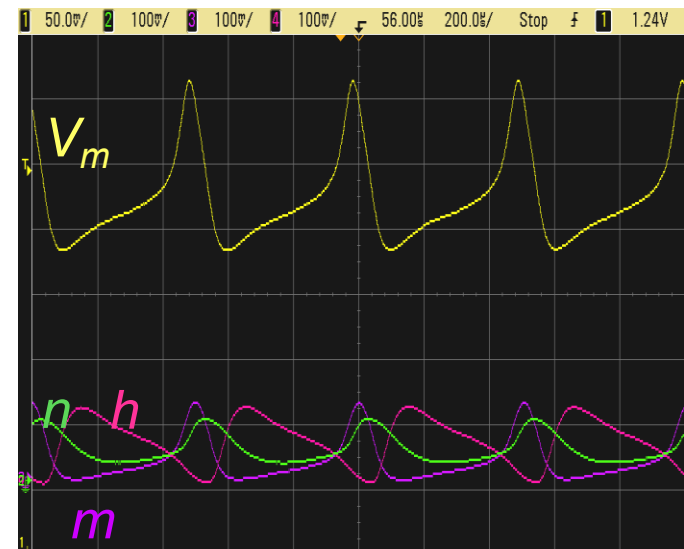
Recorded dynamics of action potential and channel kinetics for one HH neuron.

NeuroDyn Synaptic Coupling
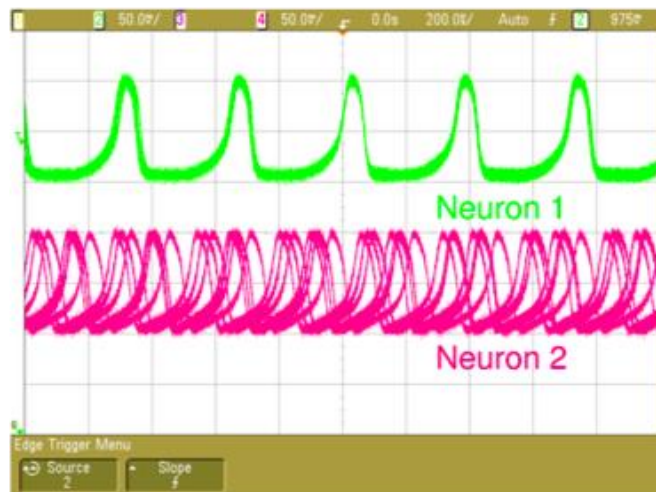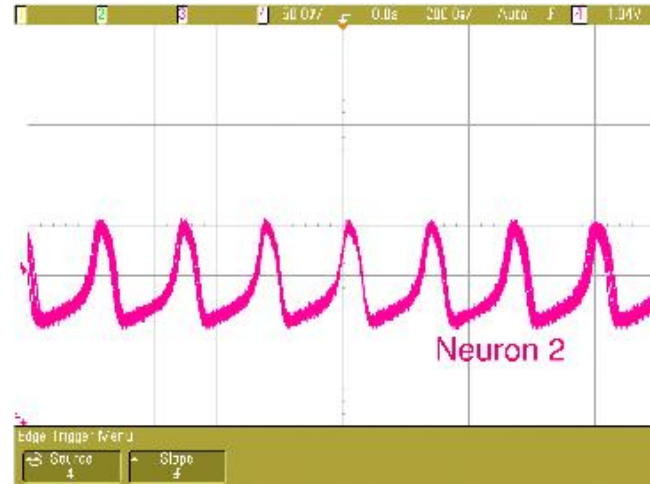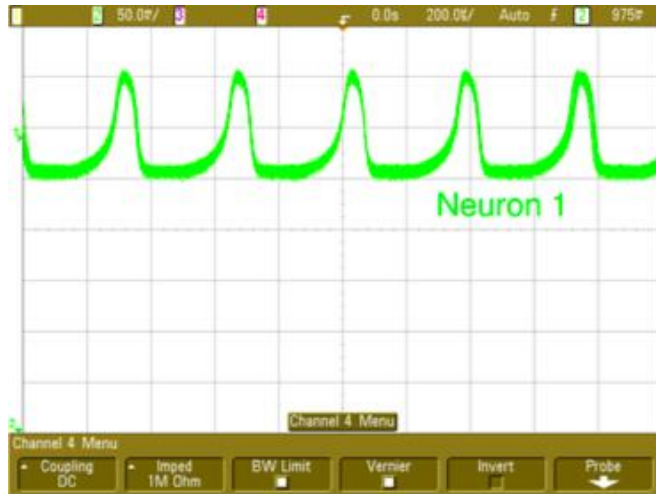
Uncoupled
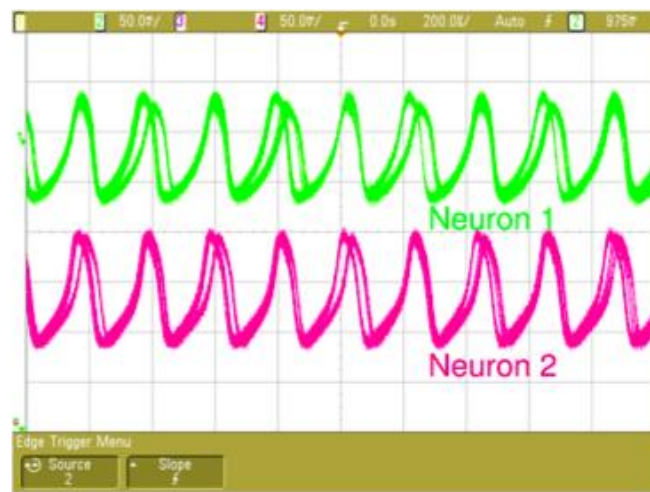
Mutual inhibitory synaptic coupling

Generalized Map-Based I&F Neural Dynamics

Izhikevich 2003; Rulkov, Timofeev & Bazhenov 2004; Mihalas & Niebur 2009

$$v' = 0.04v^2 + 5v + 140 - u + I$$
$$u' = a(bv - u)$$

if $v = 30$ mV,
then $v \leftarrow c$, $u \leftarrow u + d$

peak 30 mV

reset c

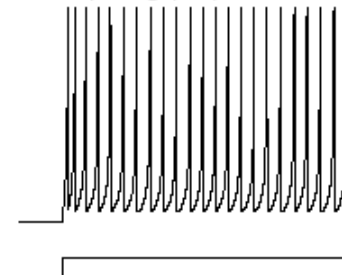reset d

decay with rate a

sensitivity b

parameter b / parameter a

parameter d / parameter c

RZ, LTS,TC, RS,IB,CH, FS

RS, IB, FS,LTS,RZ, CH, TC
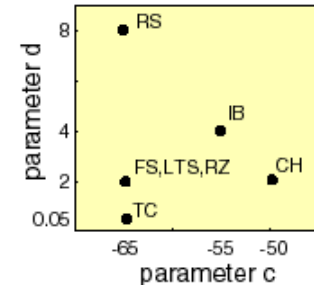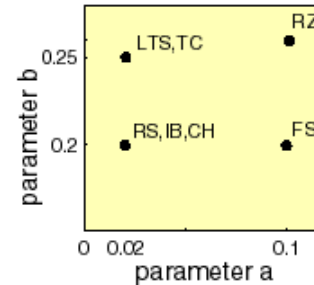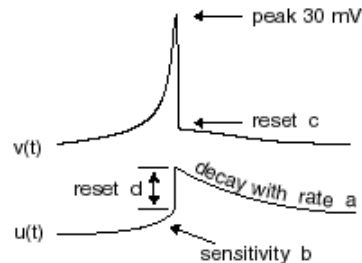
regular spiking (RS)
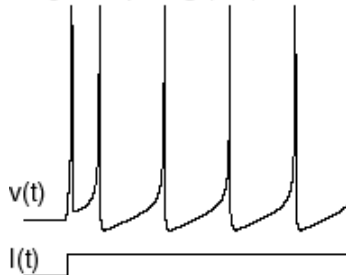
intrinsically bursting (IB)
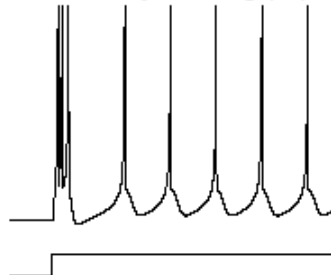
chattering (CH)
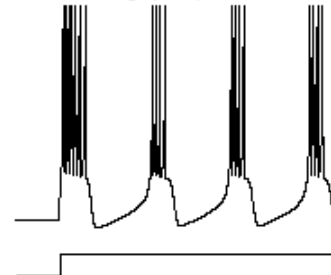
fast spiking (FS)

thalamo-cortical (TC)
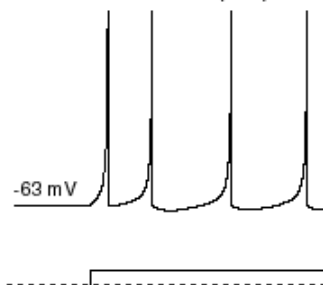
thalamo-cortical (TC)
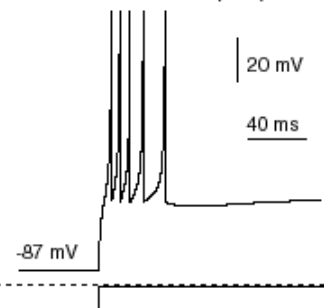
resonator (RZ)
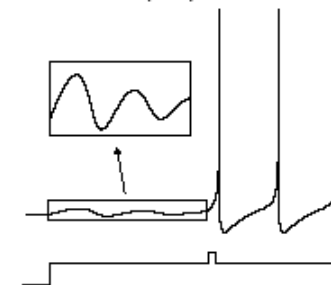
low-threshold spiking (LTS)

-63 mV

-87 mV

20 mV

40 ms
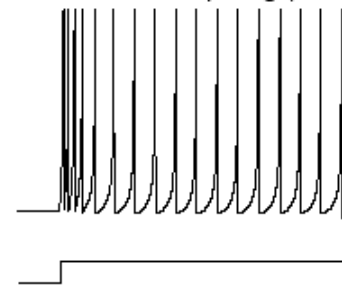
Electronic version of the figure and reproduction permissions are freely available at www.izhikevich.com

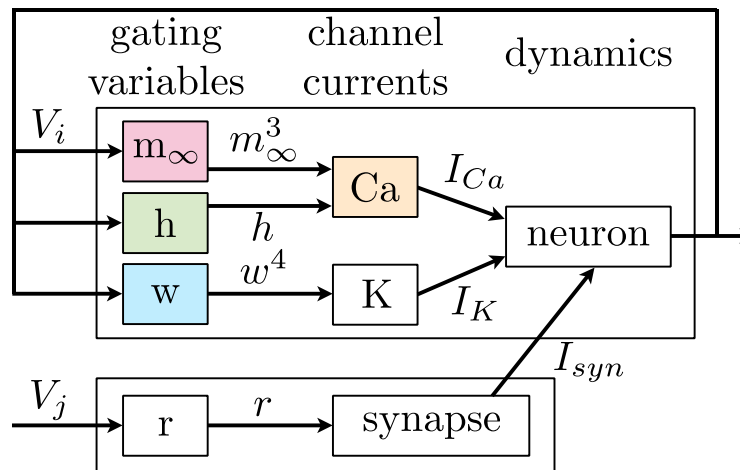# Generalized HH/ML Neural Dynamics
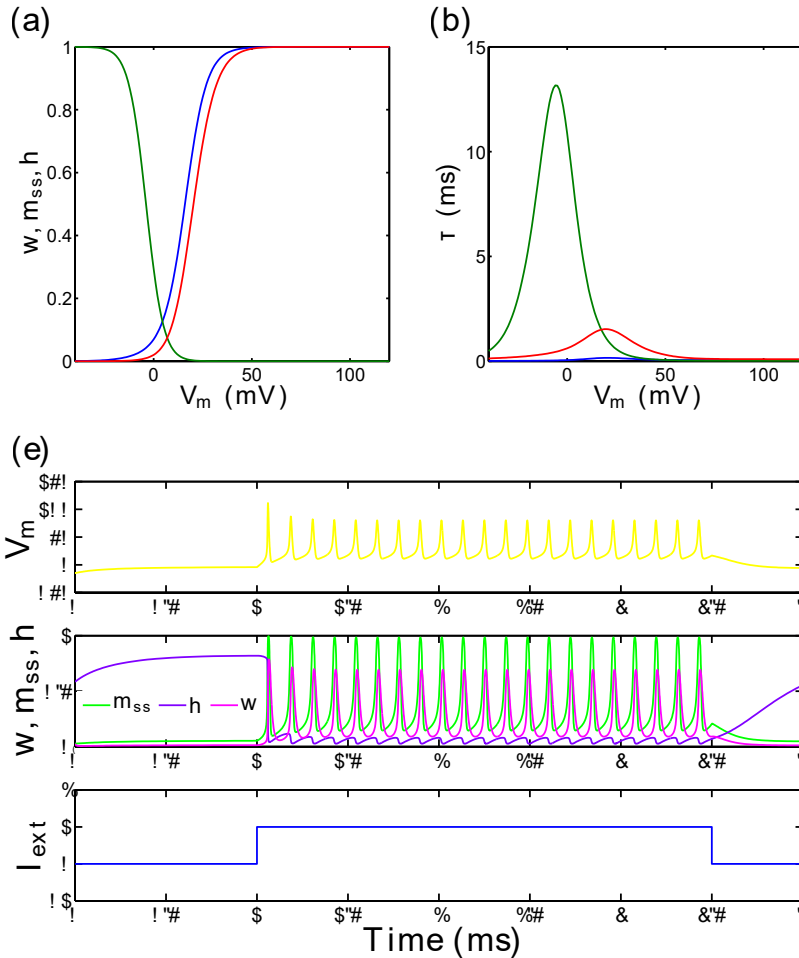
Yu, Sejnowski, and Cauwenberghs 2010
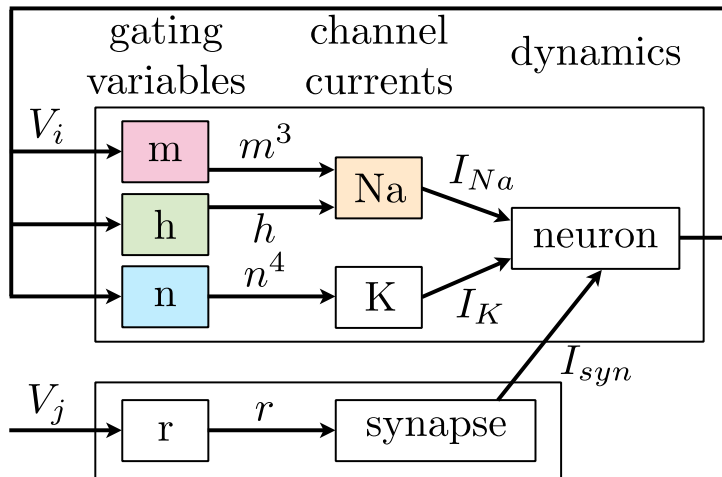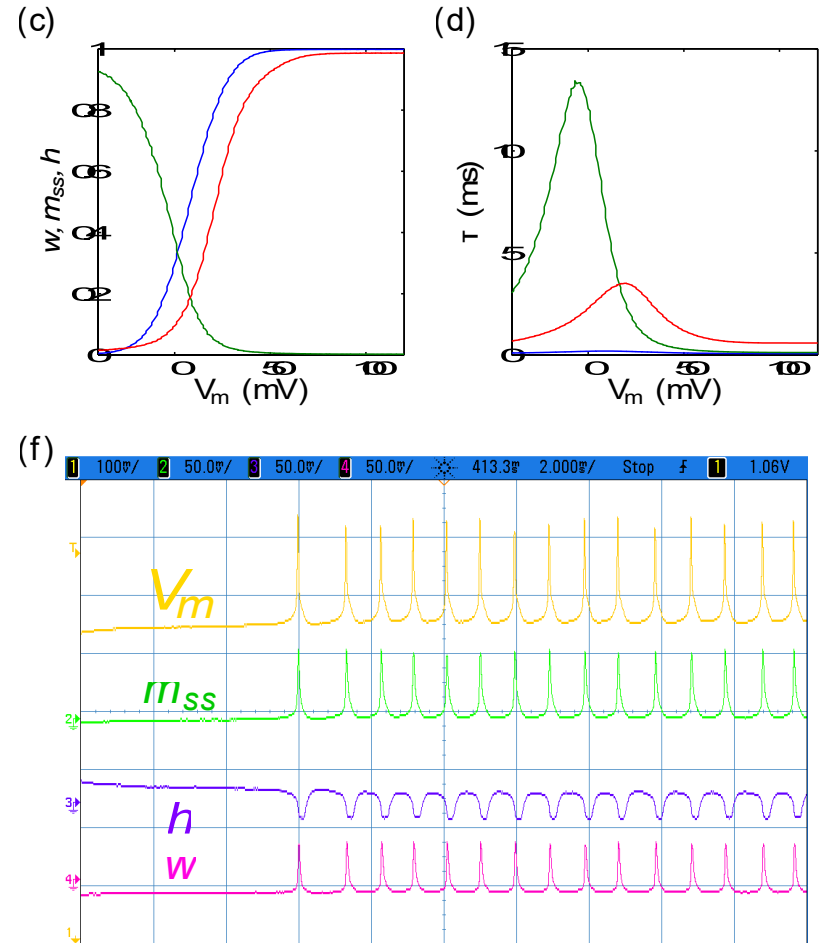

(a) Hodgkin Huxley
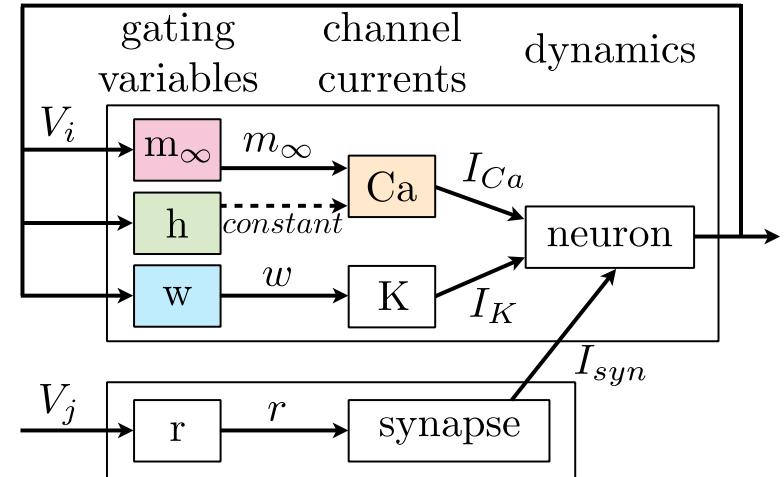
(b) Morris Lecar

(c) Extended Morris Lecar

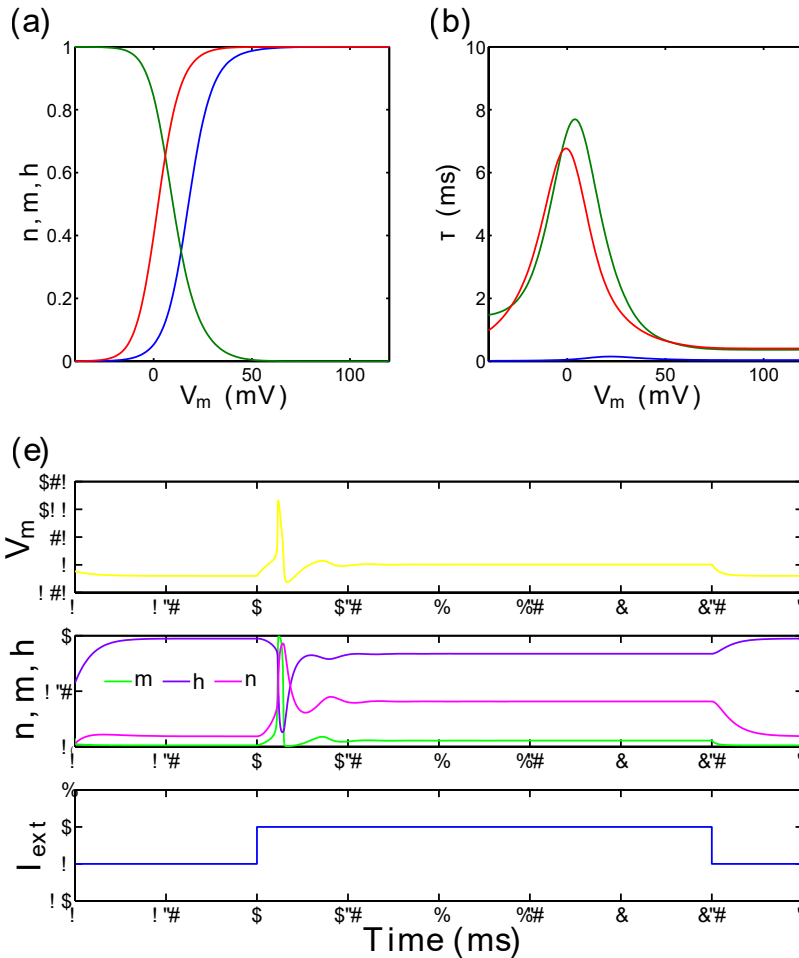# *NeuroDyn* Tonic Spiking

Matlab digital simulation
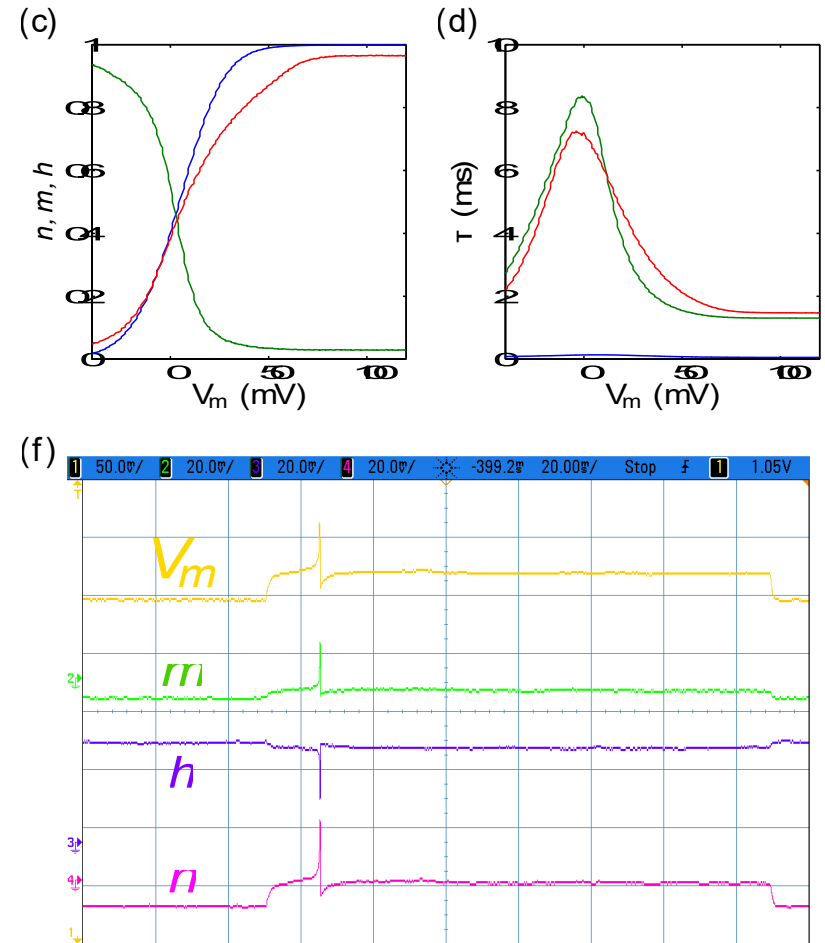
NeuroDyn analog emulation

Yu, Sejnowski, and Cauwenberghs 2011

NeuroDyn Phasic Spiking
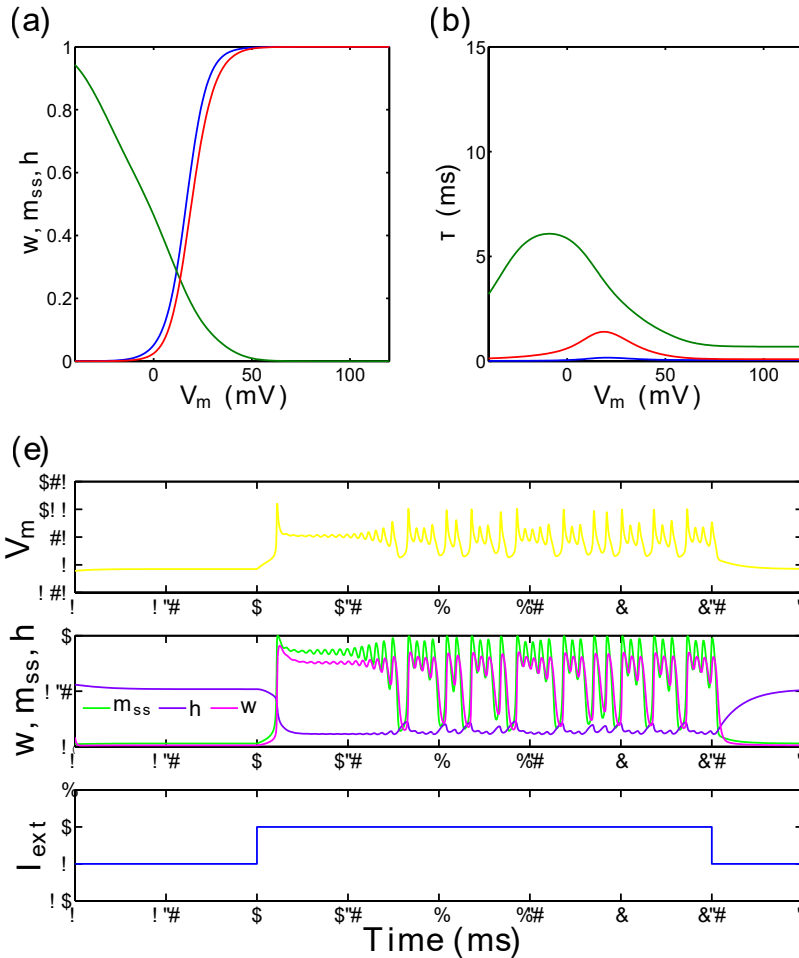
Matlab digital simulation
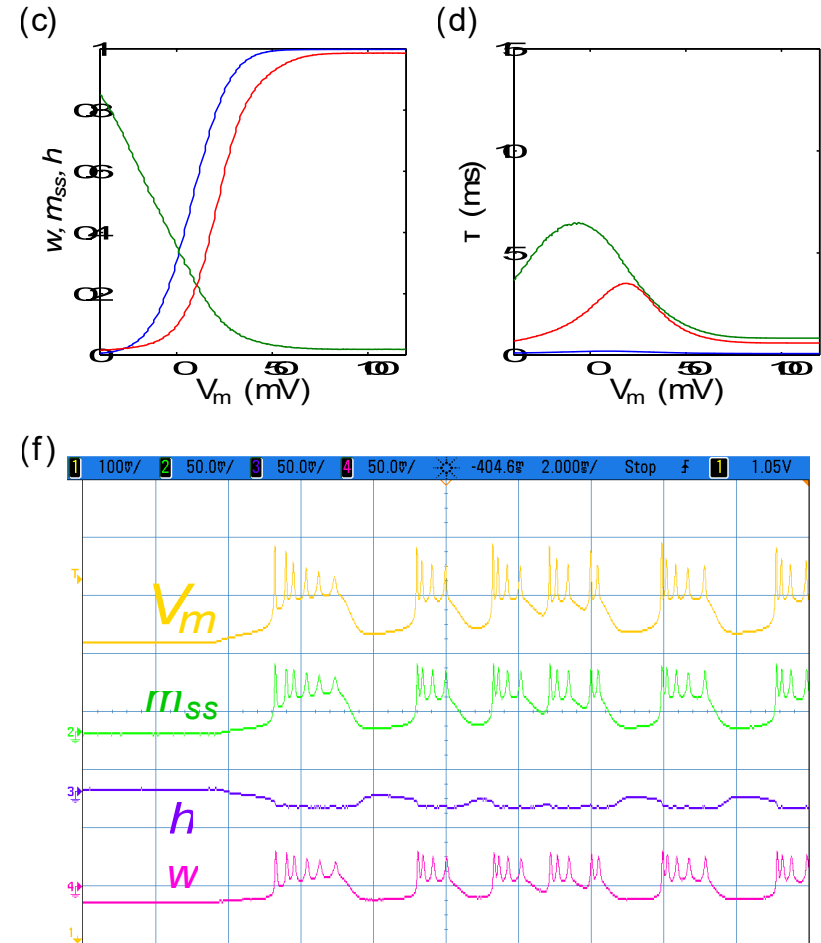
NeuroDyn analog emulation

Yu, Sejnowski, and Cauwenberghs 2011

NeuroDyn Tonic Bursting
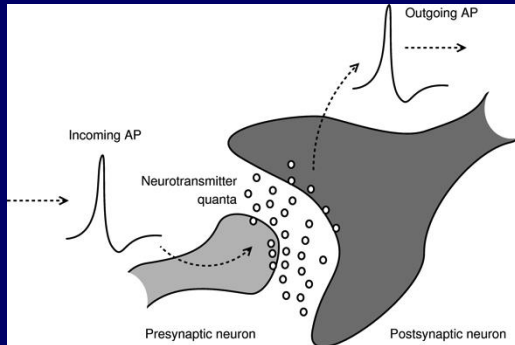
Matlab digital simulation

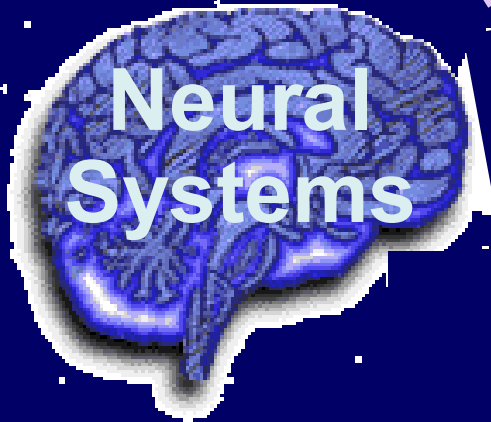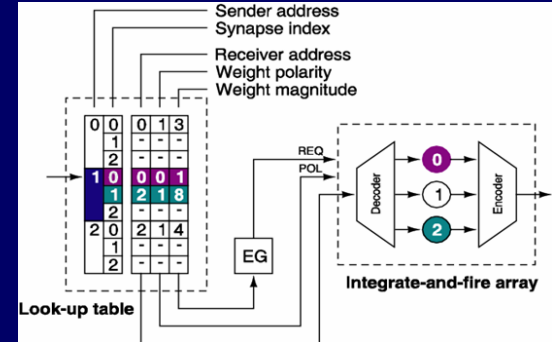*NeuroDyn* analog emulation

Yu, Sejnowski, and Cauwenberghs 2011
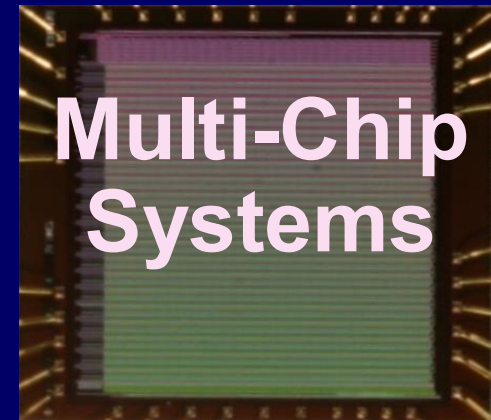
Reconfigurable Synaptic Connectivity and Plasticity
From Microchips to Large-Scale Neural Systems

Address-Event Representation

Neural Systems

Synaptic Plasticity & Wiring

Multi-Chip Systems
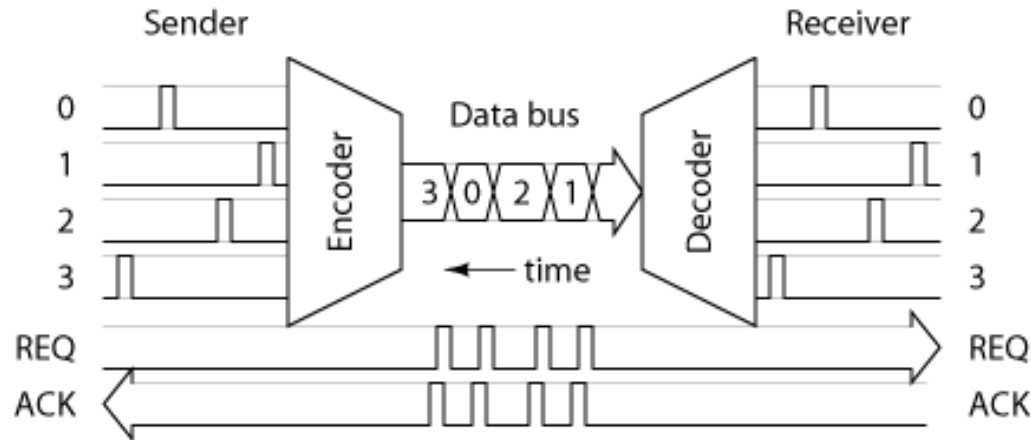
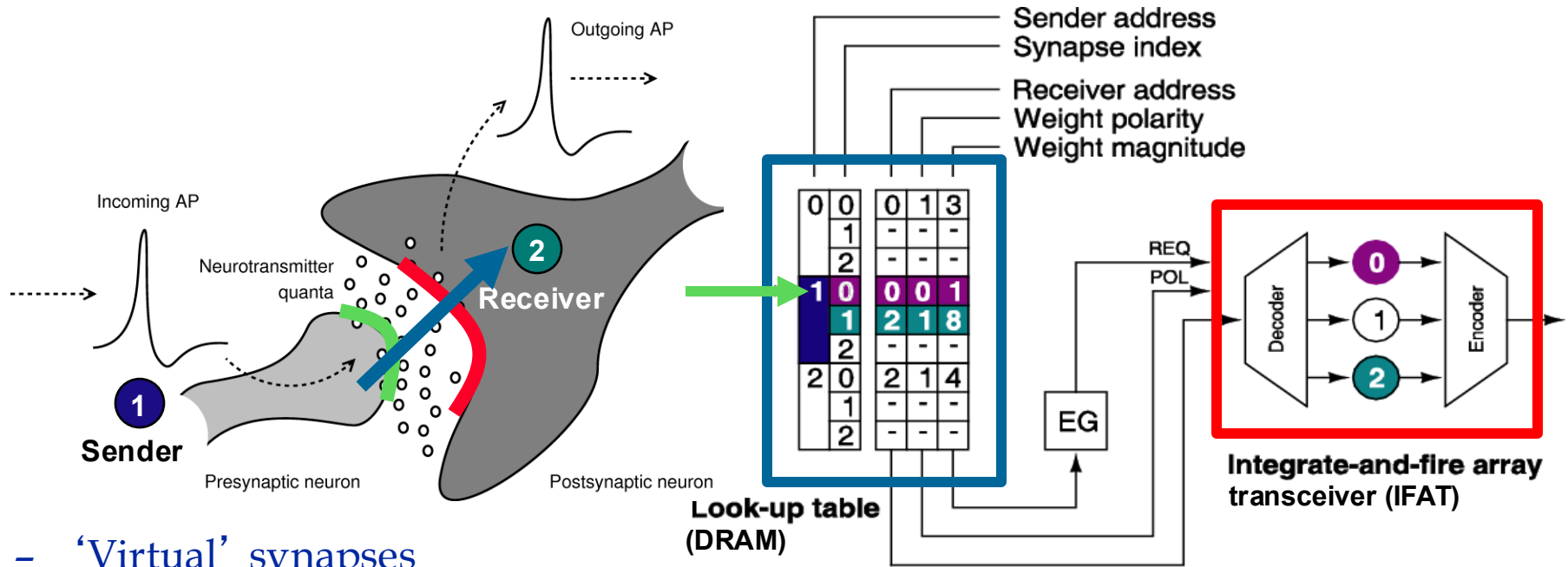# Address-Event Representation (AER)

Lazzaro et al., 1993; Mahowald, 1994; Deiss 1994; Boahen 2000

- AER emulates extensive connectivity between neurons by communicating spiking events time-multiplexed on a shared data bus.

- Spikes are represented by two values:
  - *Cell location (address)*
  - *Event time (implicit)*

- All events within Δt are "simultaneous"

Address-Event Synaptic Connectivity
Goldberg, Cauwenberghs and Andreou, 2000

Outgoing AP

Incoming AP

Neurotransmitter quanta

2
Receiver

1
Sender

Presynaptic neuron

Postsynaptic neuron

Sender address
Synapse index

Receiver address
Weight polarity
Weight magnitude

REQ
POL

Decoder

Encoder

EG

Look-up table (DRAM)
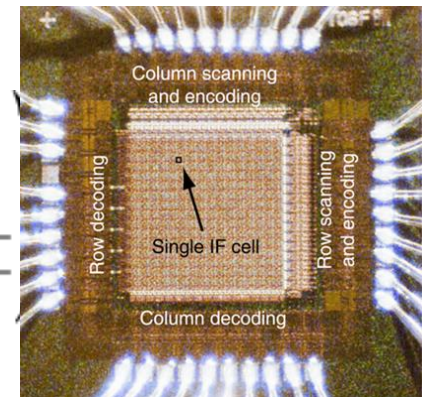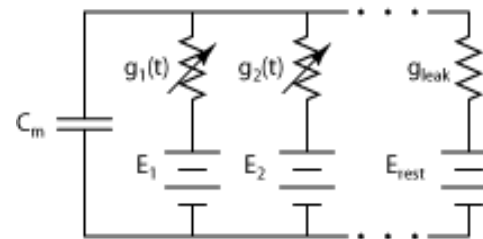
Integrate-and-fire array transceiver (IFAT)

- 'Virtual' synapses
  - *Dynamically reconfigurable*
  - *Wide-ranging connectivity*
  - *Rewiring and synaptic plasticity*
- Quantal release: $R = n\,p\,q$
  - *n: multiplicity* (repeat event)
  - *p: probability of release* (toss a coin)
  - *q: quantity released* (set amplitude)

$g_1(t)$ $g_2(t)$ g_{leak}

C_m

E_1 E_2 E_{rest}

Column scanning and encoding

Row decoding

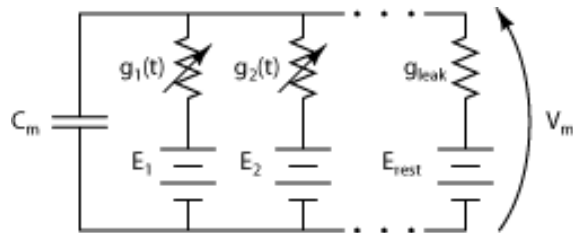Single IF cell

Row scanning and encoding

Column decoding

IFAT2 (2000)

Silicon Membrane Array Transceiver
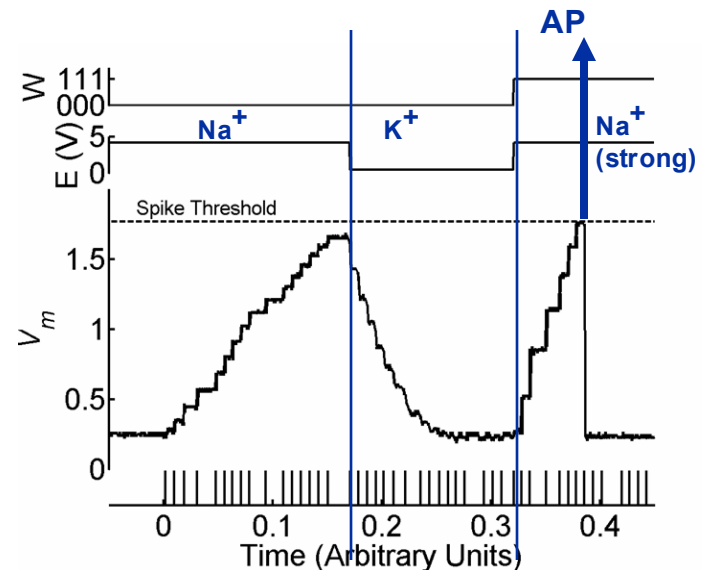
Vogelstein, Mallik and Cauwenberghs, 2004

– Voltage-controlled membrane conductance

- *Event-driven activation*
- *Dynamically reconfigurable:*
  - *conductance g*
  - *driving potential E*

60 x 40 IFAT Array

Event Arbitration

Event Coding/Decoding

IFAT3 (2004)

– Address-event encoding of pre-and post-synaptic action potentials
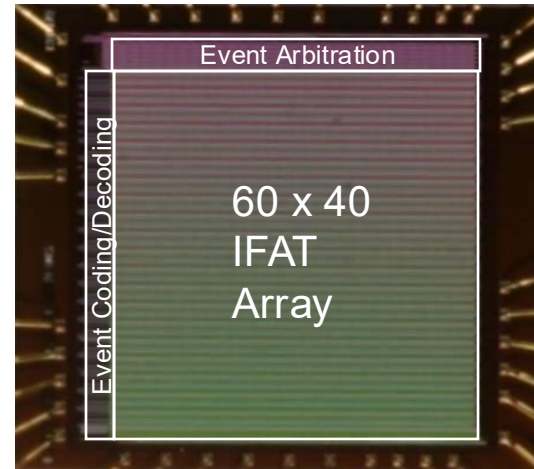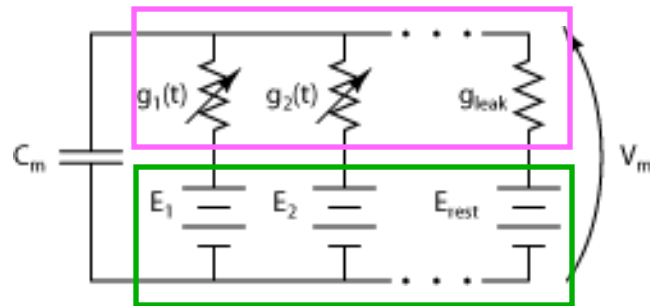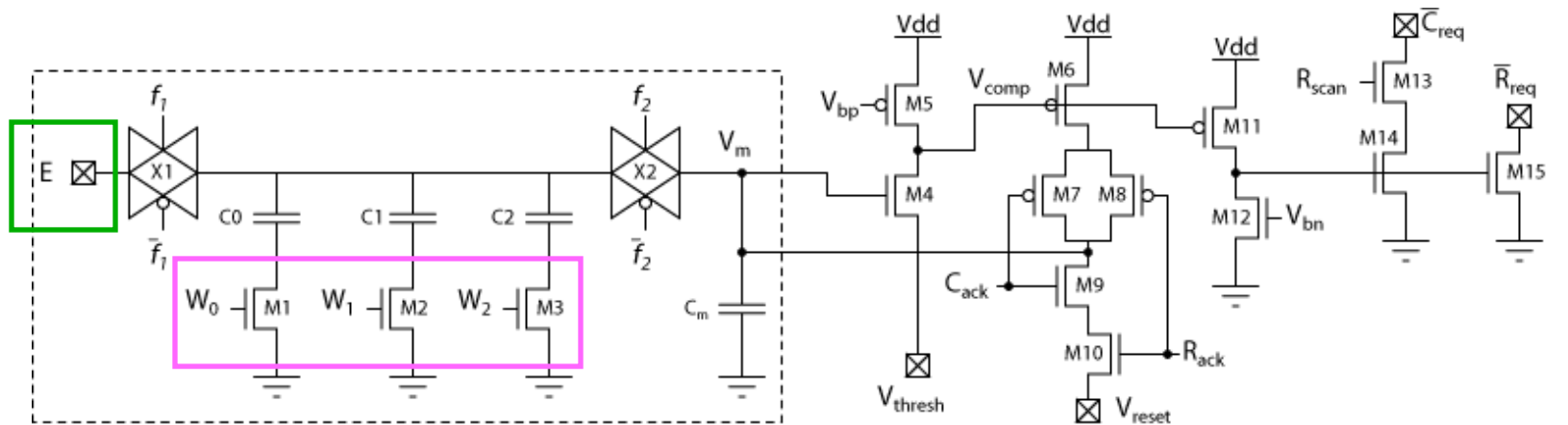
Silicon Membrane Circuit

Goldberg, Cauwenberghs and Andreou, 2000
Vogelstein, Mallik and Cauwenberghs, 2004

$g_i(t)$ *ion-specific* membrane conductance

E_i *ion-specific* reversal potential
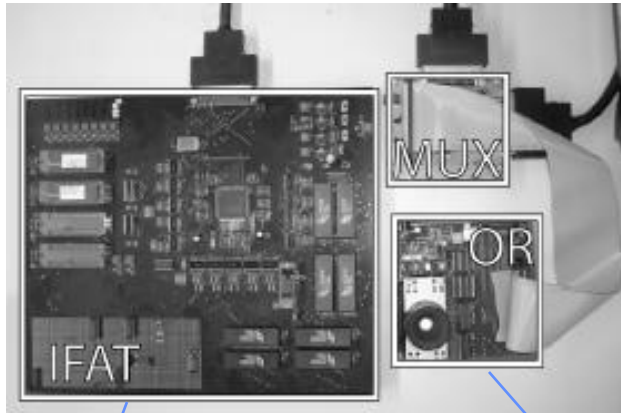
Synapse subcircuit

Action potential generation and AER handshaking

Hierarchical Vision and Saliency-Based Acuity Modulation

Vogelstein, Mallik, Culurciello, Cauwenberghs, and Etienne-Cummings, NECO 2007
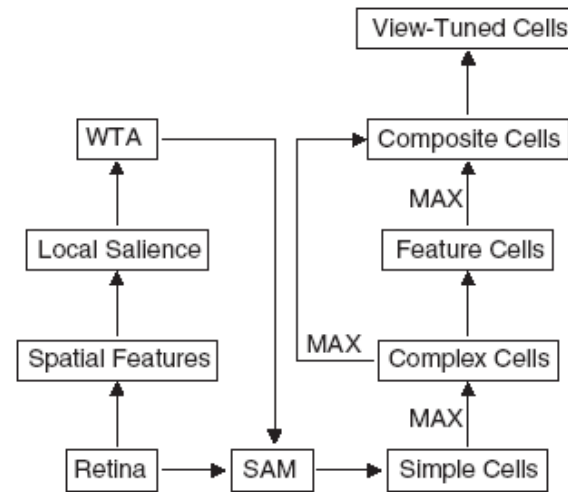

IFAT Cortical Model
4800 silicon neurons
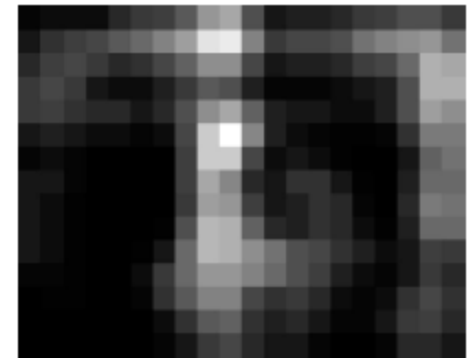4,194,304 synapses

Octopus Silicon Retina
80 x 60 pixels
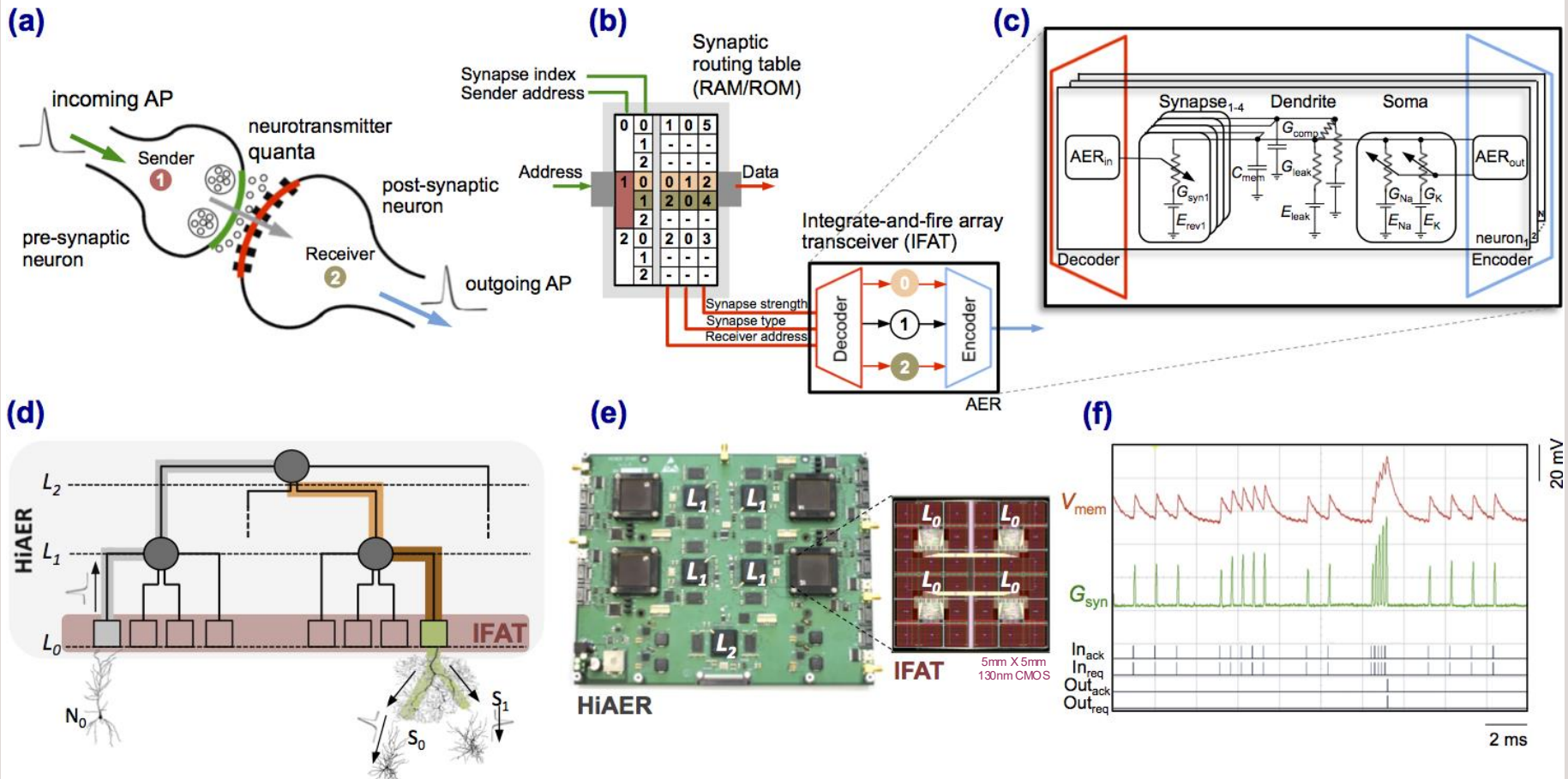AER spiking output

OR image

Simple cell response

Saliency map

Large-Scale Reconfigurable Neuromorphic Computing

Hierarchical Address-Event Routing (HiAER) Integrate-and-Fire Array Transceiver (IFAT) for scalable and reconfigurable neuromorphic neocortical processing. (a) Biophysical model of neural and synaptic dynamics. (b) Dynamically reconfigurable synaptic connectivity is implemented across IFAT arrays of addressable neurons by routing neural spike events locally through DRAM synaptic routing tables. (c) Each neural cell models conductance based membrane dynamics in proximal and distal compartments for synaptic input with programmable axonal delay, conductance, and reversal potential. (d) Multiscale global connectivity through a hierarchical network of HiAER routing nodes. (e) HiAER-IFAT board with 4 IFAT custom silicon microchips, serving 256k neurons and 256M synapses, and spanning 3 HiAER levels (L0-L2) in connectivity hierarchy. (f) The IFAT neural array multiplexes and integrates (top traces) incoming spike synaptic events to produce outgoing spike neural events (bottom traces). The latest IFAT microchip measured energy consumption is 22 pJ per spike event, several orders of magnitude more efficient than emulation on CPU/GPU platforms.

Yu et al, BioCAS 2012; Park et al, BioCAS 2014; Park et al, TNNLS 2017; Broccard et al, JNE 2017

BENG 216 Neuromorphic Integrated Bioelectronics

Date	Topic
9/29, 10/1	Biophysical foundations of natural intelligence in neural systems. Subthreshold MOS silicon models of membrane excitability. Silicon neurons. Hodgkin-Huxley and integrate-and-fire models of spiking neuronal dynamics. Action potentials as address events.
10/6, 10/8	Silicon retina. Low-noise, high-dynamic range photoreceptors. Focal-plane array signal processing. Spatial and temporal contrast sensitivity and adaptation. Dynamic vision sensors.
10/13, 10/15	Silicon cochlea. Low-noise acoustic sensing and automatic gain control. Continuous wavelet filter banks. Interaural time difference and level difference auditory localization. Blind source separation and independent component analysis.
10/20, 10/22	Silicon cortex. Neural and synaptic compute-in-memory arrays. Address-event decoders and arbiters, and integrate-and-fire array transceivers. Hierarchical address-event routing for locally dense, globally sparse long-range connectivity across vast spatial scales.
10/27, 10/29	Midterm review. Modular and scalable design for neuromorphic and bioelectronic integrated circuits and systems. Design for full testability and controllability.
11/3, 11/5	Low-noise, low-power design. Fundamental limits of noise-energy efficiency, and metrics of performance. Biopotential and electrochemical recording and stimulation, lab-on-a-chip electrophysiology, and neural interface systems-on-chip.
11/10, 11/12	Adaptive offset cancelation and autoranging in dynamic vision sensing. Tobi Delbruck's lecture on silicon retina history with a live demo of event-based dynamic vision systems.
11/17, 11/19	Learning and adaptation to compensate for external and internal variability over extended time scales. Background blind calibration of device mismatch. Correlated double sampling and chopping for offset drift and low-frequency noise cancellation.
11/24, 11/26	Energy conservation. Resonant inductive power delivery and data telemetry. Ultra-high efficiency neuromorphic computing. Resonant adiabatic energy-recovery charge-conserving synapse arrays.
12/1 - 12/5	Project final presentations. All are welcome!