BENG 216 Neuromorphic Integrated Bioelectronics

Week 4: Silicon Cortex

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Date	Торіс				
9/30, 10/2	Biophysical foundations of natural intelligence in neural systems. Subthreshold MOS silicon models of membrane excitability. Silicon neurons. Hodgkin-Huxley and integrate-and-fire models of spiking neuronal dynamics. Action potentials as address events.				
10/7, 10/9	Silicon retina. Low-noise, high-dynamic range photoreceptors. Focal-plane array signal processing. Spatial and temporal contrast sensitivity and adaptation. Dynamic vision sensors.				
10/14, 10/16	Silicon cochlea. Low-noise acoustic sensing and automatic gain control. Continuous wavelet filter banks. Interaural time difference and level difference auditory localization. Blind source separation and independent component analysis.				
10/21, 10/23	Silicon cortex. Neural and synaptic compute-in-memory arrays. Address-event decoders and arbiters, and integrate-and-fire array transceivers. Hierarchical address-event routing for locally dense, globally sparse long-range connectivity across vast spatial scales.				
10/28, 10/30	Midterm review. Modular and scalable design for neuromorphic and bioelectronic integrated circuits and systems. Design for full testability and controllability.				
11/4, 11/6	Low-noise, low-power design. Fundamental limits of noise-energy efficiency, and metrics of performance. Biopotential and electrochemical recording and stimulation, lab-on-a-chip electrophysiology, and neural interface systems-on-chip.				
11/13	Learning and adaptation to compensate for external and internal variability over extended time scales. Background blind calibration of device mismatch. Correlated double sampling and chopping for offset drift and low-frequency noise cancellation.				
11/18, 11/20	Adaptive offset cancelation and autoranging in dynamic vision sensing. Tobi Delbruck's lecture on silicon retina history with a live demo of event-based dynamic vision systems.				
11/25, 11/27	Energy conservation. Resonant inductive power delivery and data telemetry. Ultra-high efficiency neuromorphic computing. Resonant adiabatic energy-recovery charge-conserving synapse arrays.				
12/2 - 12/6	Project final presentations. All are welcome!				

Reconfigurable Synaptic Connectivity and Plasticity From Microchips to Large-Scale Neural Systems



Address-Event Representation (AER)

Lazzaro et al., 1993; Mahowald, 1994; Deiss 1994; Boahen 2000



- AER emulates extensive connectivity between neurons by communicating spiking events time-multiplexed on a shared data bus.
- Spikes are represented by two values:
 - Cell location (address)
 - Event time (implicit)
- All events within Δt are "simultaneous"



Silicon Membrane Array Transceiver

Vogelstein, Mallik and Cauwenberghs, 2004

- Voltage-controlled membrane conductance
 - Event-driven activation
 - Dynamically reconfigurable:
 - *conductance g*
 - driving potential E



 Address-event encoding of pre-and post-synaptic action potentials



Silicon Membrane Circuit

Goldberg, Cauwenberghs and Andreou, 2000 Vogelstein, Mallik and Cauwenberghs, 2004



g_i(t) ion-specific membrane conductance

E_i ion-specific reversal potential



Hierarchical Vision and Saliency-Based Acuity Modulation

Vogelstein, Mallik, Culurciello, Cauwenberghs, and Etienne-Cummings, NECO 2007



OR image

Simple cell response

Saliency map

Spike Timing-Dependent Plasticity



Bi and Poo, 1998

Spike Timing-Dependent Plasticity

in the Address Domain



Spike Timing-Dependent Plasticity on the IFAT

Vogelstein et al, NIPS*2002



Scaling of Task and Machine Complexity



Achieving (or surpassing) human-level machine intelligence requires a convergence between:

- Advances in computing resources approaching connectivity and energy efficiency levels of computing and communication in the brain;
- Advances in deep learning methods, and supporting data, to adaptively reduce algorithmic complexity.

Scaling and Complexity Challenges

- Scaling the event-based neural systems to performance and efficiency approaching that of the human brain will require:
 - Scalable advances in silicon integration and architecture
 - Scalable, locally dense and globally sparse interconnectivity
 - Hierarchical address-event routing
 - High density (10¹² neurons, 10¹⁵ synapses within 5L volume)
 - Silicon nanotechnology and 3-D integration
 - High energy efficiency (10¹⁵ synOPS/s at 15W power)
 - Adiabatic switching in event routing and synaptic drivers
 - Scalable models of neural computation and synaptic plasticity
- **Neuro** Convergence between cognitive and neuroscience modeling
 - Modular, neuromorphic design methodology
- CogSci Data-rich, environment driven evolution of machine complexity

EE NanoE Phys

CS

Large-Scale Reconfigurable Neuromorphic Computing Technology and Performance Metrics

	Stromatias 2013 SpiNNaker Manchester	Davies 2018 Loihi Intel	Merolla 2014 TrueNorth IBM	Schemmel 2010 FACETS/BrainScaleS Heidelberg	Benjamin 2014 NeuroGrid Stanford	Park 2014 IFAT UCSD	Qiao 2015 ROLLS ETHZ-INI
Technology (nm)	130	14	28	180	180	90	180
Die Size (mm ²)	102	60	430	50	168	16	51
Neuron Type	Digital Arbitrary	Digital Conductance Integrate & Fire	Digital Accumulate & Fire	Analog Conductance Integrate & Fire	Analog Shared-Dendrite Conductance I&F	Analog 2-Compartment Conductance I&F	Analog Conductance Integrate & Fire
# Neurons	5216 ¹	128k ²	1M ²	512	65k	65k	256
Neuron Area (μm²)	N/A ¹	240 (240k) ²	14 (3325) ²	1500	1800	140	918
Peak Throughput (Events/s)	5M	3.4G	1G	65M	91M	73M	100M
Energy Efficiency (J/SynEvent)	8n	24p	26p	N/A	31p	22p	50p

¹ Software-instantiated neuron model. ² Time-multiplexed neuron processor

Benjamin, B., P. Gao, E. McQuinn, S. Choudhary, A. Chandrasekaran, J. Bussat, R. Alvarez-Icaza, J. Arthur, P. Merolla, and K. Boahen, "Neurogrid: A mixed analogdigital multichip system for large-scale neural simulations," *Proc. IEEE*, 102(5):699–716, 2014.

Davies, M. et al., "Loihi: A Neuromorphic Manycore Processor with On-Chip Learning," IEEE Micro, vol. 38 (1), pp. 82-99, 2018.

Merolla, P.A., J.V. Arthur, R. Alvarez-Icaza, A S. Cassidy, J. Sawada, F. Akopyan, B.L. Jackson, N. Imam, C. Guo, Y. Nakamura, B. Brezzo, I. Vo, S.K. Esser, R. Appuswamy, B. Taba, A. Amir, M.D. Flickner, W.P. Risk, R. Manohar, and D. S. Modha, "A million spiking-neuron integrated circuit with a scalable communication network and interface," *Science*, 345(6197):668–673, 2014.

Park, J., S. Ha, T. Yu, E. Neftci, and G. Cauwenberghs, "65k-neuron 73-Mevents/s 22-pJ/event asynchronous micro-pipelined integrate-and-fire array transceiver," *Proc. 2014 IEEE Biomedical Circuits and Systems Conf. (BioCAS)*, 2014.

Qiao, N., H. Mostafa, F. Corradi, M. Osswald, F. Stefanini, D. Sumislawska, and G. Indiveri, "A reconfigurable on-line learning spiking neuromorphic processor comprising 256 neurons and 128k synapses," *Front. Neurosci.*, 9:141. doi: 10.3389/fnins.2015.00141, 2015.

Schemmel, J., D. Bruderle, A. Grubl, M. Hock, K. Meier, and S. Millner, "A waferscale neuromorphic hardware system for large-scale neural modeling," *Proc. 2010 IEEE Int. Symp. Circuits and Systems (ISCAS)*, 1947–1950, 2010.

Stromatias, E., F. Galluppi, C. Patterson, and S. Furber, "Power analysis of largescale, real-time neural networks on SpiNNaker," *Proc. 2013 Int. Joint Conf. Neural Networks (IJCNN)*, 2013.

Long-Range Configurable Synaptic Connectivity



Comparison of synaptic connection topologies for several recent large-scale event-driven neuromorphic systems and the proposed hierarchical addressevent routing (HiAER), represented diagrammatically in two characteristic dimensions of connectivity: expandability (or extent of global reach), and flexibility (or degrees of freedom in configurability). Expandability, measured as distance traveled across the network for a given number of hops *N*, varies from linear and polynomial in *N* for linear and mesh grid topologies to exponential in *N* for hierarchical tree-based topologies. Flexibility, measured as the number of target destinations reachable from any source in the network, ranges from unity for point-to-point (P2P) connectivity and constant for convolutional kernel (Conv.) connectivity to the entire network for arbitrary (Arb.) connectivity. MMAER: Multicasting Mesh AER; WS: Wafer-Scale.

Park et al, "Hierarchical Address Event Routing for Reconfigurable Large-Scale Neuromorphic Systems," IEEE TNNLS, 2017

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Hierarchical Address-Event Routing (HiAER)



 $L3^1$ $L2^2$ L12: L1 (2)(3) (1)(2)(3) 1 2 (3) 4 4 4 2 3 1

Example network with 16 neurons and weighted synaptic connections.

Example partitioning into hierarchical neural network with ascending and descending projections through inserted relay neurons.



Corresponding edge-vertex-dual HiAER implementation with synaptic routing tables (SRT) at each level in the hierarchy.

Joshi et al, 2010; Park et al, 2011, 2017

Large-Scale Reconfigurable Neuromorphic Computing



Hierarchical Address-Event Routing (HiAER) Integrate-and-Fire Array Transceiver (IFAT) for scalable and reconfigurable neuromorphic neocortical processing. (a) Biophysical model of neural and synaptic dynamics. (b) Dynamically reconfigurable synaptic connectivity is implemented across IFAT arrays of addressable neurons by routing neural spike events locally through DRAM synaptic routing tables. (c) Each neural œll models conductance based membrane dynamics in proximal and distal compartments for synaptic input with programmable axonal delay, conductance, and reversal potential. (d) Multiscale global connectivity through a hierarchical network of HiAER routing nodes. (e) HiAER-IFAT board with 4 IFAT custom silicon microchips, serving 256k neurons and 256M synapses, and spanning 3 HiAER levels (L0-L2) in connectivity hierarchy. (f) The IFAT neural array multiplexes and integrates (top traces) incoming spike synaptic events to produce outgoing spike neural events (bottom traces). The IFAT microchip measured energy consumption is 22 pJ per spike event, several orders of magnitude more efficient than emulation on CPU/GPU platforms.

Yu et al, BioCAS 2012; Park et al, BioCAS 2014; Park et al, TNNLS 2017; Broccard et al, JNE 2017; Park et al, Front. Neurosci. 2023

IFAT Thermodynamics of Neural Excitability

Yu, Park, Joshi, Maier, Cauwenberghs, BioCAS 2012

Large-Scale Reconfigurable Neuromorphic Computing

- Integrate-and-fire array transceiver (IFAT) as digitally programmable analog neural supercomputer
- Biophysical detail in neural and synaptic continuoustime dynamics
- Record high density: 65k
 two-compartment neurons
 with 65M reconfigurable
 conductance-based
 synapses
- Record low energy: 22 pJ per synaptic event
- Real-time at 73M spikes per second

J. Park *et al*, "A 65k-Neuron 73-Mevents/s 22-pJ/event Asynchronous Micro-Pipelined Integrate-and-Fire Array Transceiver", Proc. IEEE BioCAS 2014.

Memristive Synapse Arrays for Neuromorphic Processing-in-Memory

Intel/STmicroelectronics (Numonyx) 256Mb multi-level phase-change memory (PCM) [Bedeschi et al, 2008]. Die size is 36mm2 in 90nm CMOS/Ge2Sb2Te5, and cell size is 0.097μm2. (a) Basic storage element schematic, (b) active region of cell showing crystalline and amorphous GST, (c) SEM photograph of array along the wordline direction after GST etch, (d) I-V characteristic of storage element, in set and reset states, (e) programming characteristic, (f) I-V characteristic of pnp bipolar selector.

- Scalable to high density and energy efficiency

- < 100nm cell size in 12nm CMOS</p>
- < pJ energy per synapse operation
- Vertically stacked integration in Intel-Micron 3D Xpoint/Optene SSD persistent memory

Memristive Synapse Arrays for Neuromorphic Processing-in-Memory

Hybridization and nanoscale integration of CMOS neural arrays with phase change memory (PCM) synapse crossbar arrays. (a)Nanoelectronic PCM synapse with spike-timing dependent plasticity (STDP) [Kuzum *et al*, 2011]. Each PCM element implements a synapse with conductance modulated through phase transition as controlled by timing of voltage pulses. (b) CMOS IFAT array vertically interfacing with nanoscale PCM synapse crossbar array by interleaving via contacts to crossbar rows. The integration of IFAT neural and PCM synapse arrays externally interfacing with HiAER neural event communication combines the advantages of highly flexible and reconfigurable HiAER-IFAT neural computation and long-range connectivity with highly efficient (fJ/synOP range energy cost) local synaptic transmission.

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CMOS-RRAM Reconfigurable Neurosynaptic Array

Wan et al, ISSCC 2020

- Integration of CMOS neurons and resistive random-access memory (RRAM) memristive synapses with *in-situ* revertible dataflow at record efficiency

W. Wan, R. Kubendran, S. B. Eryilmaz, W. Zhang, Y. Liao, D. Wu, S. Deiss, B. Gao, P. Raina, S. Joshi, H. Wu, G. Cauwenberghs, H-S. P. Wong, "33.1: A 74 TMACS/W CMOS-RRAM Neurosynaptic Core with Dynamically Reconfigurable Dataflow and In-situ Transposable Weights for Probabilistic Graphical Models," *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco CA, Febr. 15-19, 2020.

CMOS-RRAM Reconfigurable Neurosynaptic Array Wan et al. ISSCC 2020

- Gibbs stochastic sampling for Bayesian generative inference
 - Alternating between INF erence and GEN eration in transpose datapaths
 - Restricted Boltzmann Machine (RBM) / Variational Autoencoder (VAE)
- Real-time image reconstruction from corrupted/noisy MNIST input

W. Wan, R. Kubendran, S. B. Eryilmaz, W. Zhang, Y. Liao, D. Wu, S. Deiss, B. Gao, P. Raina, S. Joshi, H. Wu, G. Cauwenberghs, H-S. P. Wong, "33.1: A 74 TMACS/W CMOS-RRAM Neurosynaptic Core with Dynamically Reconfigurable Dataflow and In-situ Transposable Weights for Probabilistic Graphical Models," *IEEE Int. Solid-State Circuits Conf. (ISSCC)*, San Francisco CA, Febr. 15-19, 2020.

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CMOS-RRAM Integration for AI on the Edge

- First fully integrated RRAM-based compute-in-memory chip to combine:
 - High *versatility* in configuring cores for diverse model architectures;
 - Superior (>2x) energy *efficiency*;
 - High inference *accuracy* comparable to software.
 - Applications to reconfigurable and heterogeneous AI on the edge.

W. Wan, R. Kubendran, C. Schaefer, S.B. Eryilmaz, W. Zhang, D. Wu, S. Deiss, P. Raina, H. Qian, B. Gao, S. Joshi, H. Wu, H.-S.P. Wong, and G. Cauwenberghs, "A Compute-in-Memory Chip Based on Resistive Random-Access Memory," *Nature, vol. 608, pp. 504–512, 2022.* <u>https://www.nature.com/articles/s41586-022-04992-8</u>

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Neuromorphic Bulk Switching RRAM

Filamentary RRAM

Bulk (Area-type) RRAM

- Bulk switching resistive random-access memory avoids the need for highvoltage forming, provides gradual updates with many closely spaced analog levels, and exhibits uniform distribution with minimal variations.
- Bulk switching devices are compatible with CMOS technology, enabling ultrahigh density on-chip synapses for robust, high-throughput neuromorphic computing with online learning functionality at substantially greater energy efficiency and bandwidth than other deep learning/AI hardware approaches.

Park J, Kumar A, Zhou Y, Oh S, Kim J-H, Shi Y, Jain S, Hota G, Qui E, Nagle A, Schuman C, Cauwenberghs G, Kuzum D. Multi-level, forming and filament free, bulk switching trilayer RRAM for neuromorphic computing at the edge. *Nature Communications*. *15.1 (2024): 3492*

Selector-Less Compute-in-Memory Crossbars

- High-density synapse crossbar arrays
 - Eliminates area-consuming selector elements
 - Efficient switched-capacitor voltage sensing
- Eliminates power-hungry transimpedance amplifiers at array periphery
 - Extended dynamic range
 - Adjustable through pulse shaping

S. Jain, G. Hota, Y. Shi, S. Oh, J. Wu, P. Fowler, D. Kuzum, and G. Cauwenberghs, "A Versatile and Efficient Neuromorphic Platform for Compute-in-Memory with Selector-Less Memristive Crossbars," *IEEE Int. Symp. Circuits and Systems (ISCAS'2023)*, Monterey CA, May 21-25, 2023.

J. Kim, S. Jain, G. Hota, J. Park, A. Kumar, D. Kuzum, and G. Cauwenberghs, "Bio-Plausible Learning-on-Chip with Selector-Less Memristive Crossbars," *IEEE Int. Symp. Circuits and Systems (ISCAS'2024)*, Singapore, May 19-22, 2024.

Learning-in-Memory with RRAM Crossbars

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Incremental outer-product differential weight updates

- Four-phase decomposition of ternary outer-product of input and error
- Each phase implements partial set or ٠ reset for one pair of polarities of the ternary input and ternary error
- Negligible cross-talk owing to $V_{set}/2$ and V_{reset}/3 below set/reset thresholds

J. Kim, S. Jain, G. Hota, J. Park, A. Kumar, D. Kuzum, and G. Cauwenberghs, "Bio-Plausible Learning-on-Chip with Selector-Less Memristive Crossbars," IEEE Int. Symp. Circuits and Systems (ISCAS'2024), Singapore, May 19-22, 2024.

Spiking Synaptic Sampling Machine (S³M) Biophysical Synaptic Stochasticity in Inference and Learning

The S³M requires fewer synaptic operations (SynOps) than the equivalent Restricted Boltzmann Machine (RBM) requires multiply-accumulate (MAC) operations at the same accuracy.

- Stochastic synapses for spike-based Monte Carlo sampling
 - Models biophysical origins of noise in neural systems
 - Activity dependent noise: multiplicative synaptic sampling rather than additive neural sampling
 - Sparsity in neural activity and in synaptic connectivity
- Online unsupervised learning with STDP
 - Biophysical model of spike-based learning
 - Event-driven contrastive divergence

Emre O. Neftci, Bruno U. Pedroni, Siddharth Joshi, Maruan Al-Shedivat, Gert Cauwenberghs, "Stochastic Synapses Enable Efficient Brain-Inspired Learning Machines," *Frontiers in Neuroscience*, vol. 10, pp. 3389:1-16 (DOI: 10.3389/fnins.2016.00241), 2016.

Hierarchical Address-Event Routing Neural and Synaptic Array Transceiver HiAER-NSAT

HBM FPGA Reconfigurable Neuromorphic Computing

- Reconfigurable, high-throughput neuromorphic processing-in-memory (PIM)
 - Xilinx UltraScale+ VU37P field-programmable gate array (FPGA)
- High-Bandwidth Memory (HBM) for extreme PIM throughput
 - Integrated 8GB HBM2.0 DDR4 SDRAM
 - Sustained > 400 GB/s random-access memory bandwidth at 25 ns latency, delivering > 100 GSynOp/s throughput at 32b/Syn weight resolution
 - 32 independent HBM ports aligned with 32 neurosynaptic cores on the FPGA
- Demonstrated record low-latency, high-throughput MNIST image classification
 - 10,000-image MNIST dataset classified, at 94% accuracy, in 720 ms, or 72 μ s/image
 - *Single FPGA core implementing 784* **x** 500 **x** 10 DNN with binary threshold units

B. Pedroni, S. Deiss, N. Mysore, and G. Cauwenberghs (2020). "Design Principles of Large-Scale Neuromorphic Systems Centered on High Bandwidth Memory", *IEEE Int. Conf. on Rebooting Computing* (ICRC'2020), Nov. 2020.

Weight Quantization for Memory-Efficient Inference

- *Dropout* during training improves not only generalization performance, but also resilience to round-off in weight quantization for memory-efficient inference.
- Stochastic rounding of binary mantissa *M* and radix-2 exponent *E* retains nearly full performance with just a total of *N* = 6 bits per signed weight *w*:
 - Resolution given by mantissa M

"Performance Trade-offs in Weight Quantization for Memory-Efficient Inference," P.M. Tostado, B.U. Pedroni and G. Cauwenberghs, *IEEE Int. Conf. Artificial Intelligence Circuits and Systems (AICAS'2019)*, Hsinchu Taiwan, March 18-20, 2019.

 $w = s \ 1.x_1...x_M \ 2^{e_1...e_E}$

N = 1 + M + E

Large-Scale Reconfigurable Neuromorphic Computing

"CRI: CI-NEW: Trainable Reconfigurable Development Platform for Large-Scale Neuromorphic Cognitive Computing," National Science Foundation CNS-1823366, G. Cauwenberghs (PI), E. Neftci, and A. Majumdar, 8/2018-7/2022.

Provides open access to large-scale reconfigurable neuromorphic computing hardware and software as an experimental testbed and development platform with up to **160M** neurons and **40B** synapses for the research community at large.

Neural-Synaptic Array Transceiver (Detorakis et al, Frontiers in Neuroscience, 2018) Lifelong Learning at Scale (L2S, 2022 Telluride Neuromorphic Workshop) Neuromodulatory Control (NMC, 2021 Telluride Neuromorphic Workshop)

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