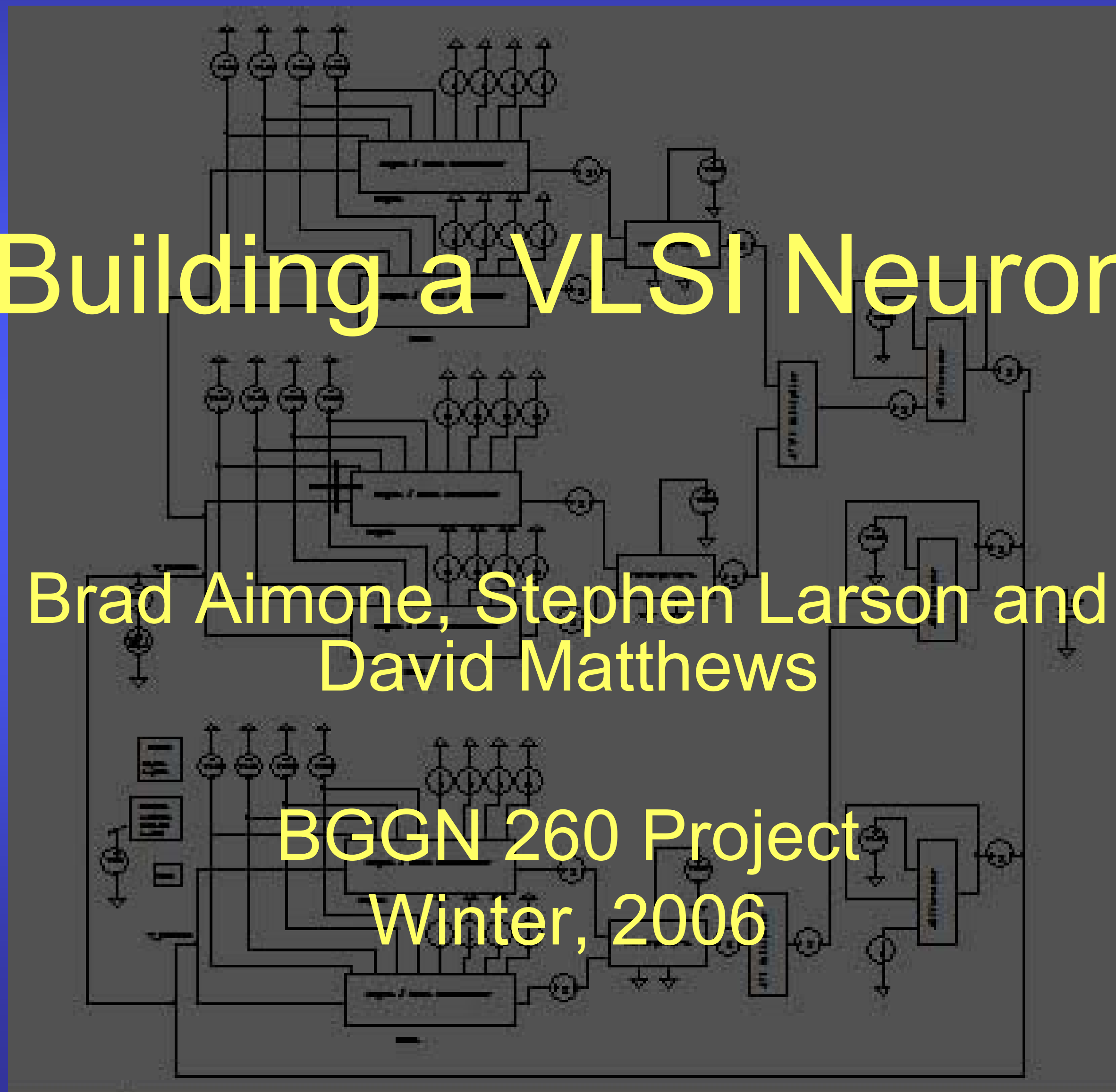
Building a VLSI Neuron



Brad Aimone, Stephen Larson and David Matthews

BGGN 260 Project
Winter, 2006

What is VLSI?

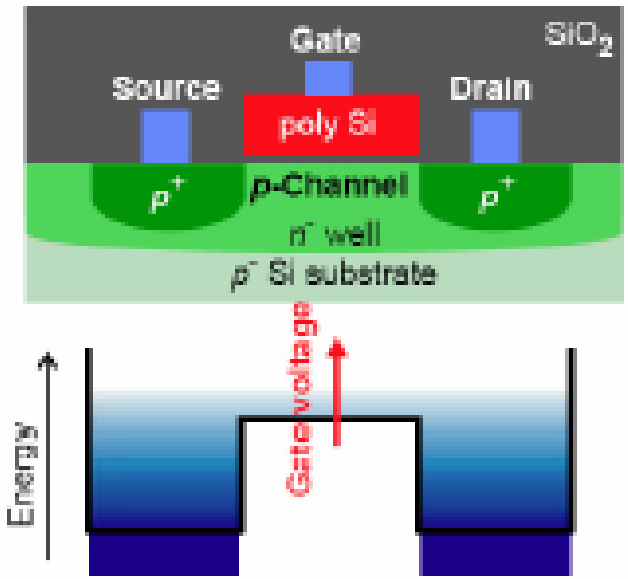
Very-Large-Scale Integrated

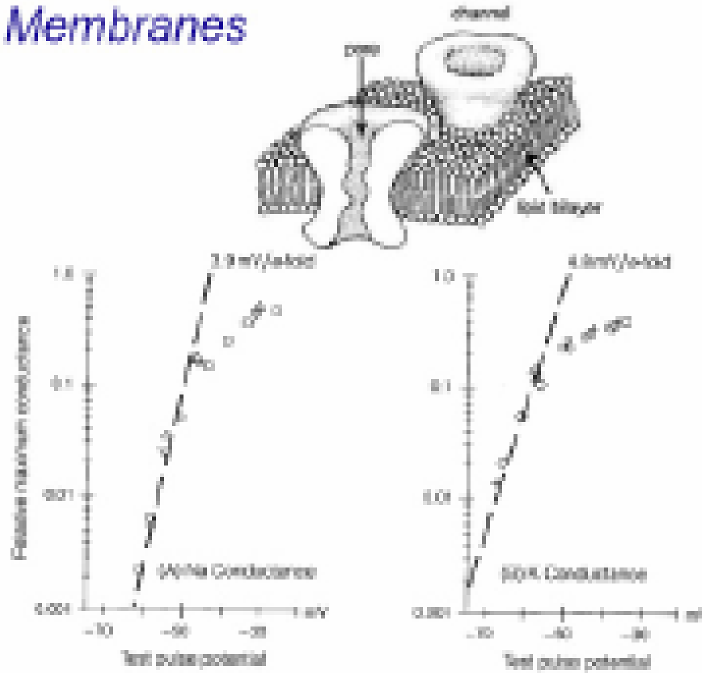
- Generating large circuits on a single chip by creating transistors
- Transistors are created by impurity doping
- Analog vs. Digital

How VLSI works subthreshold

Physics of Neural Computation

Silicon and Lipid Membranes





Squid giant axon (Hodgkin and Huxley, 1952)

Voltage-dependent *p*-channel

- *Hole transport between source and drain*
- Gate controls energy barrier for holes across the channel
- Boltzmann distribution of *hole energy* produces exponential *decrease* in channel conductance with gate voltage

Voltage-dependent conductance

- *K^+/Na^+* transport across lipid bilayer
- Membrane voltage controls energy barrier for opening of ion-selective channels
- Boltzmann distribution of *channel energy* produces exponential increase in *K^+/Na^+* conductance with membrane voltage

courtesy Gert Cauwenberghs

Benefits of VLSI

- Efficient modeling (using single transistors rather than software) allows on-line updating of parameters during real-time modeling
- Inherent system noise
- Involves biologically relevant constraints
  - available space (limited wiring)
  - power is at a premium
  - computations must be reliable and robust

Hodgkin-Huxley Model

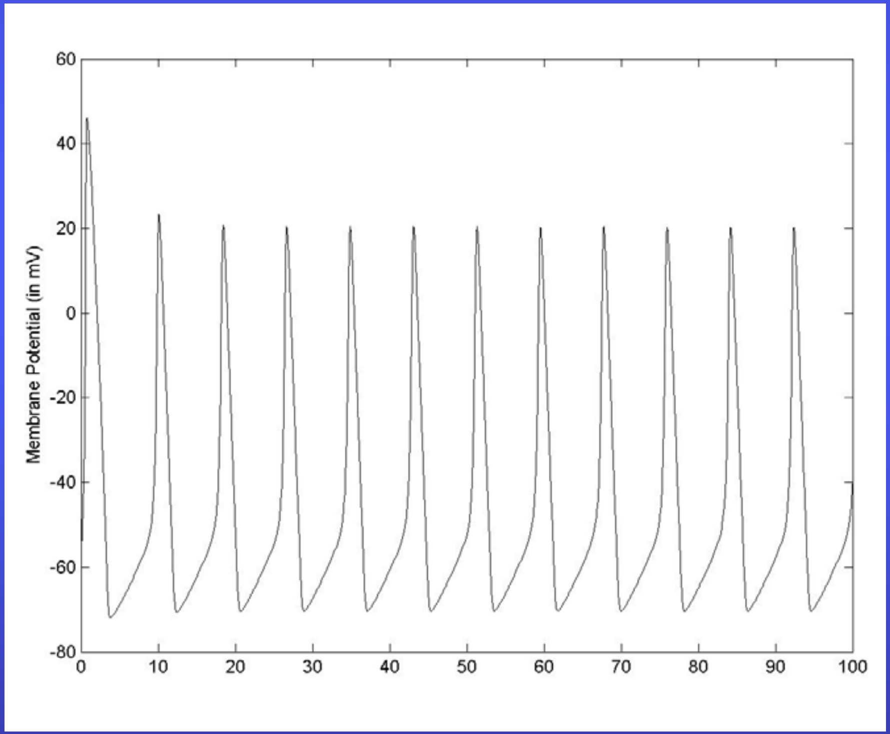
$$C\frac{dV}{dt} = g_{Na} m^3 h\left(E_{Na} - V\right) + g_K n^4 \left(E_K - V\right) + g_{Leak}\left(E_{Leak} - V\right) + I_{DC}$$

$$\frac{dm}{dt} = \alpha_m \left(1 - m\right) + \beta_m m$$

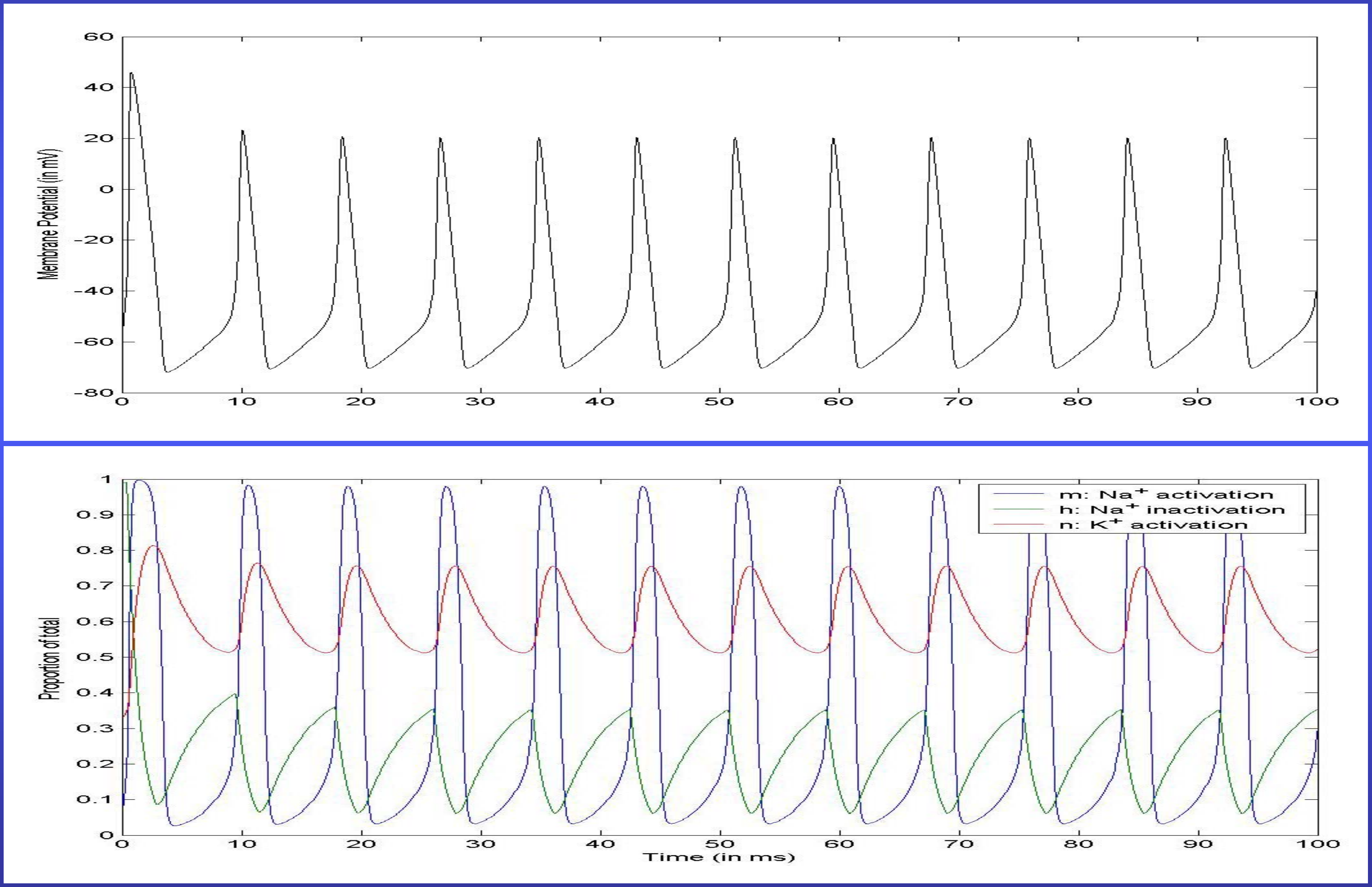
$$\frac{dn}{dt} = \alpha_n \left(1 - n\right) + \beta_n n$$

$$\frac{dh}{dt} = \alpha_h \left(1 - h\right) + \beta_h h$$

…where α's & β's are functions of voltage



HH-Simulated



Goals in designing a HH Neuron

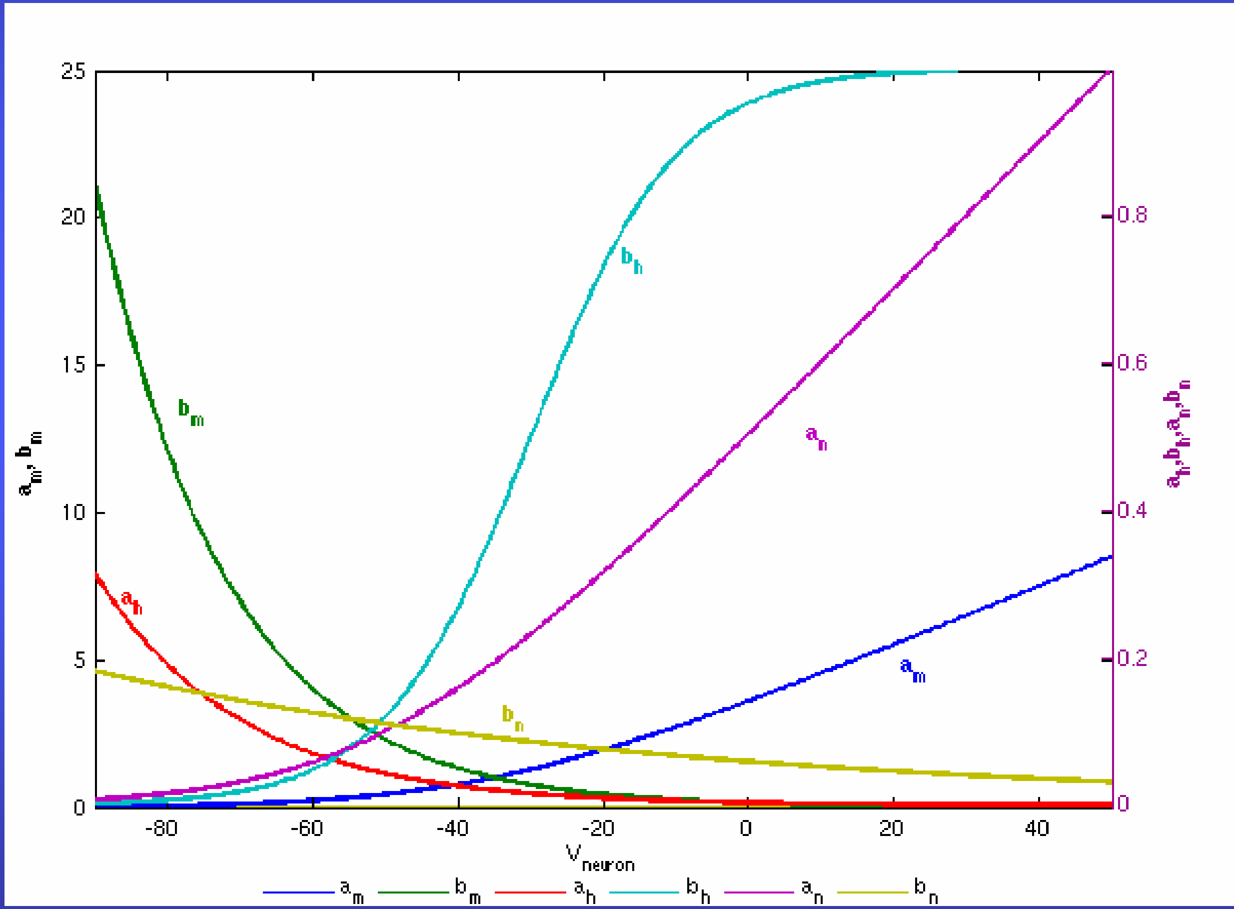
- For any given dynamical state {V,m,h,n}
  - System must calculate and apply instantaneous dynamics to calculate state variables
    - dV/dt = f(V,m,h,n);
    - dm/dt=f(a(V),b(V),m); …
  - Therefore, a(V), b(V)’s must be continuously calculated and fed into dm/dt, dn/dt, dh/dt

Practical considerations

- Transmit information through circuit as voltages or currents?
  - Some math operations are easier in current, others easier in voltage
  - Currents can be ‘mirrored’ and reversed easily
  - Voltage operations are often more precise
- In our system, most circuit subunits output information as current
- Key state – V_{neuron} – is a voltage

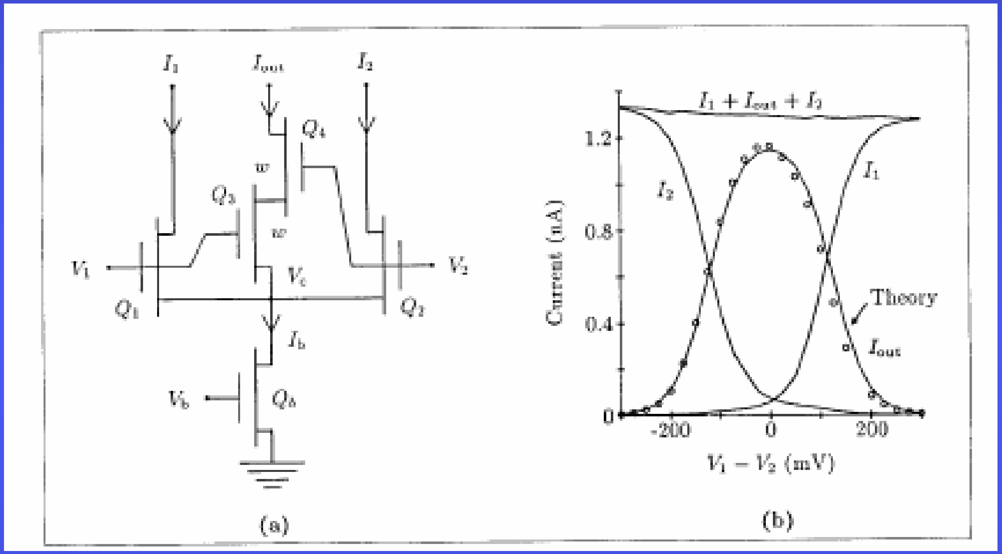
Alpha/Beta Circuit

- Need to fit unique HH equations for α and β for m,h,n
- Input is V_{neuron}
- Circuit should be general



Alpha/Beta Circuit

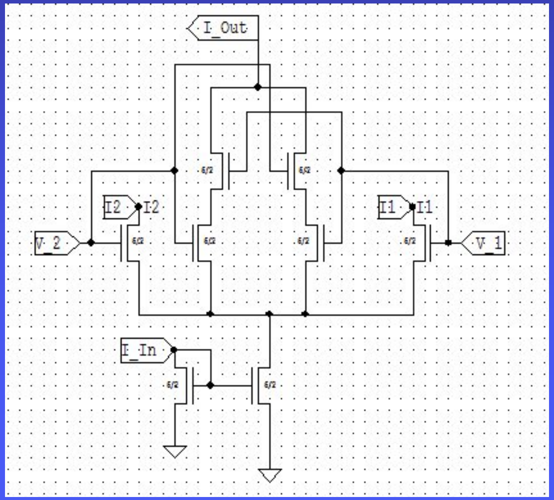
- Can fit with "Bump Circuit"
- Multiple "bumps" can be used to emulate α and β curves
  - Each has different $V_{reference}$ and I_{bias}

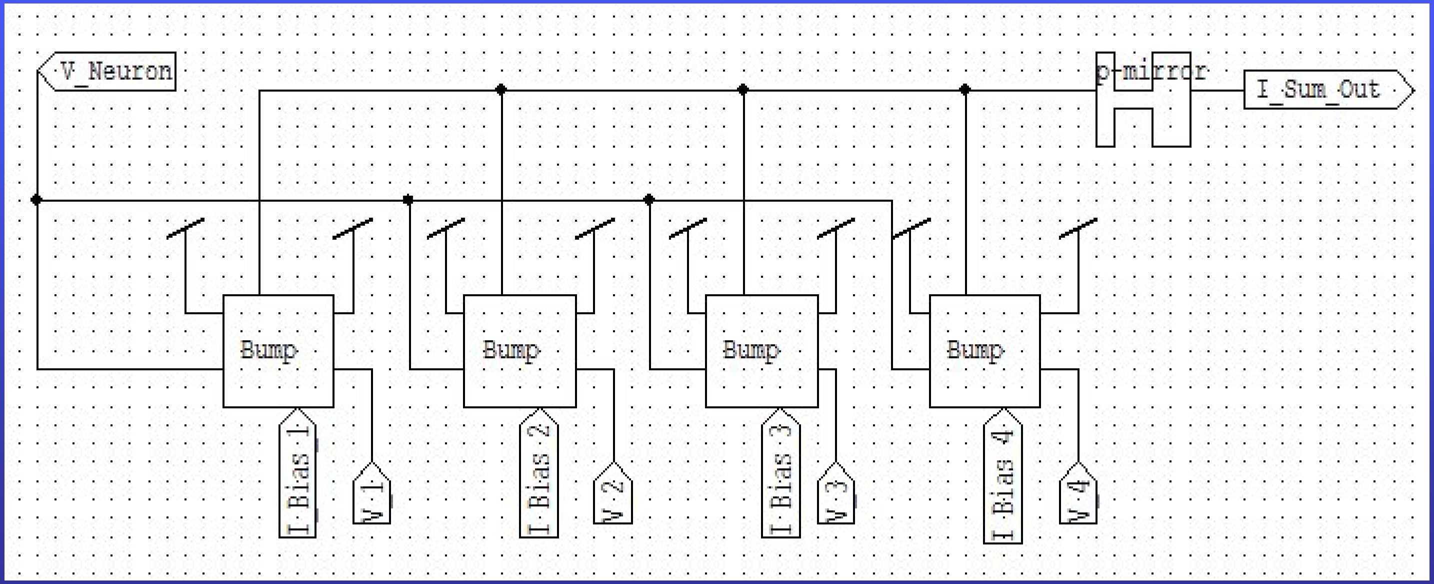


Delbruck, 1991

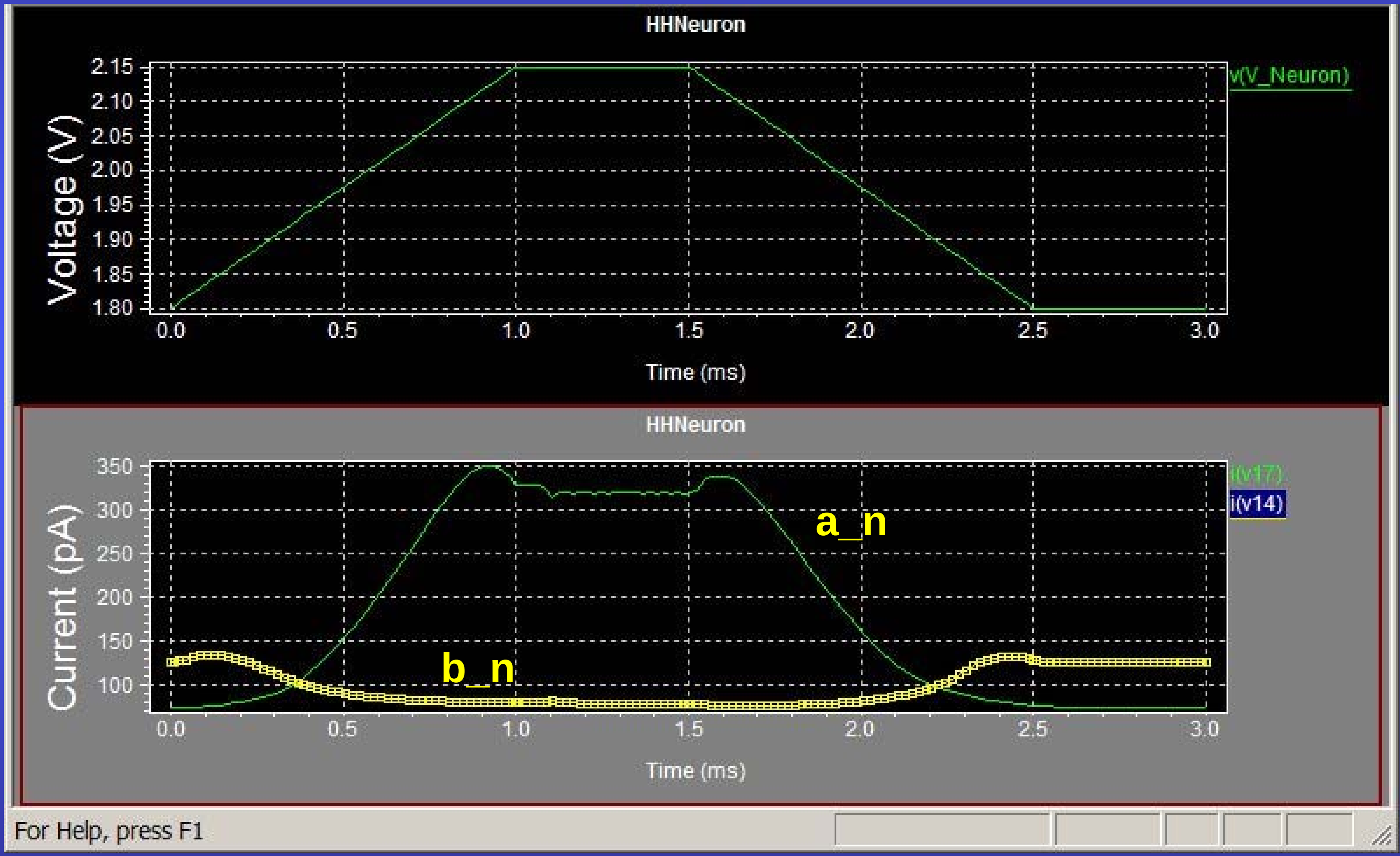
Alpha/Beta Circuit

- Bump circuit implemented
- 4 bumps used to form circuit



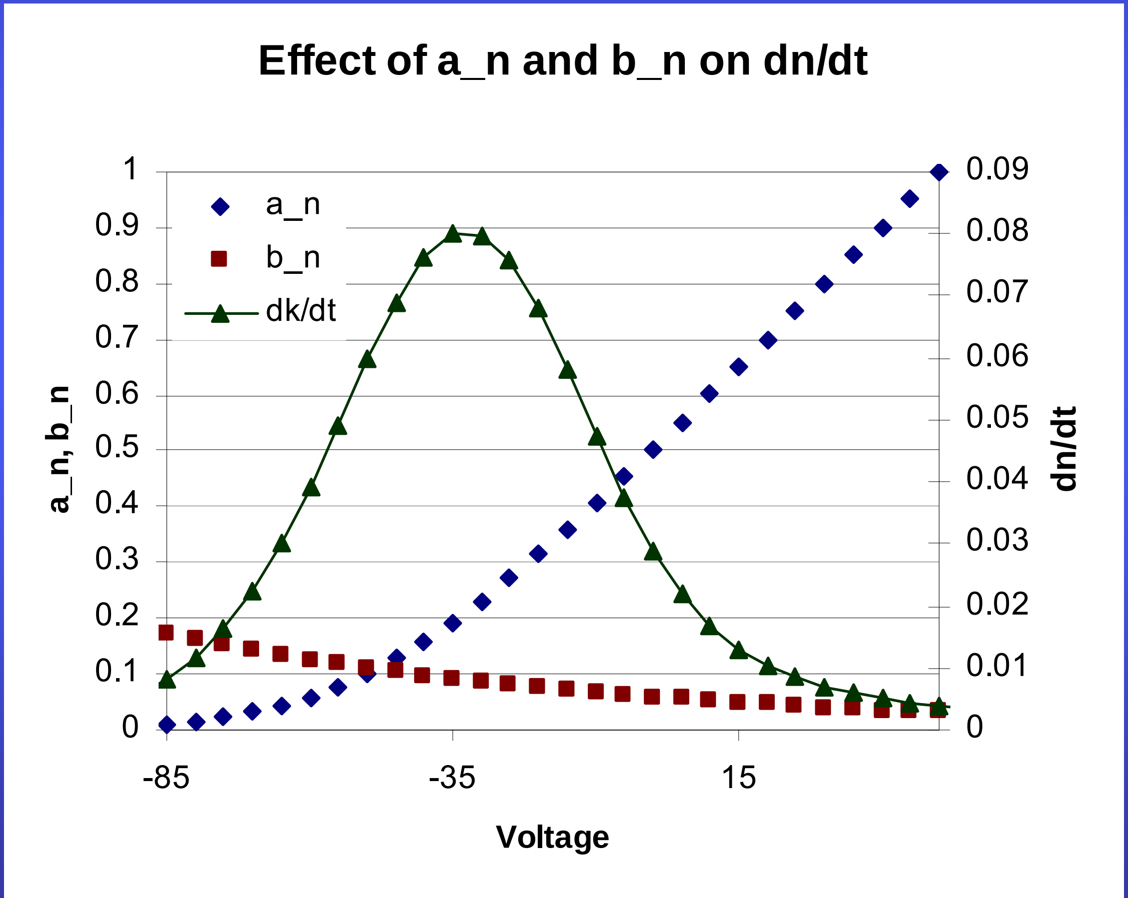


Alpha/Beta Circuit



Alpha/Beta Integrator

- Need to calculate dm/dt=B*m-A*(1-m)
- Input is a’s and b’s
- Output should be ‘m’,’h’, and ‘n’



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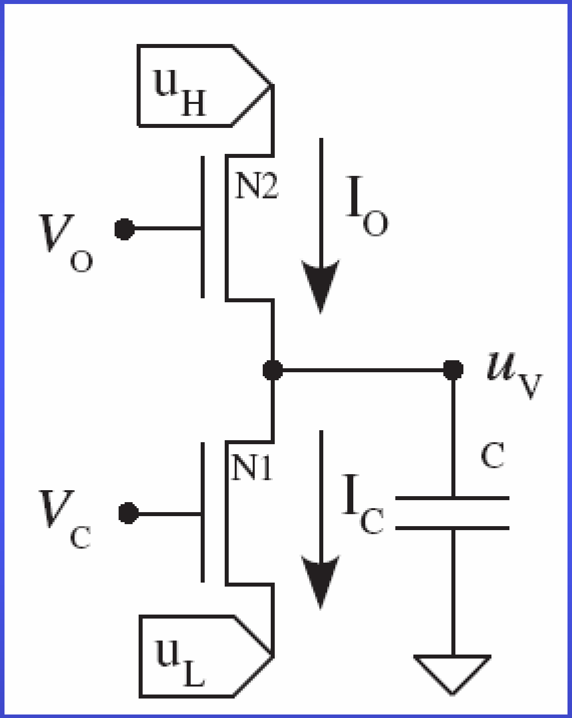

Hynna & Boahen, 2006

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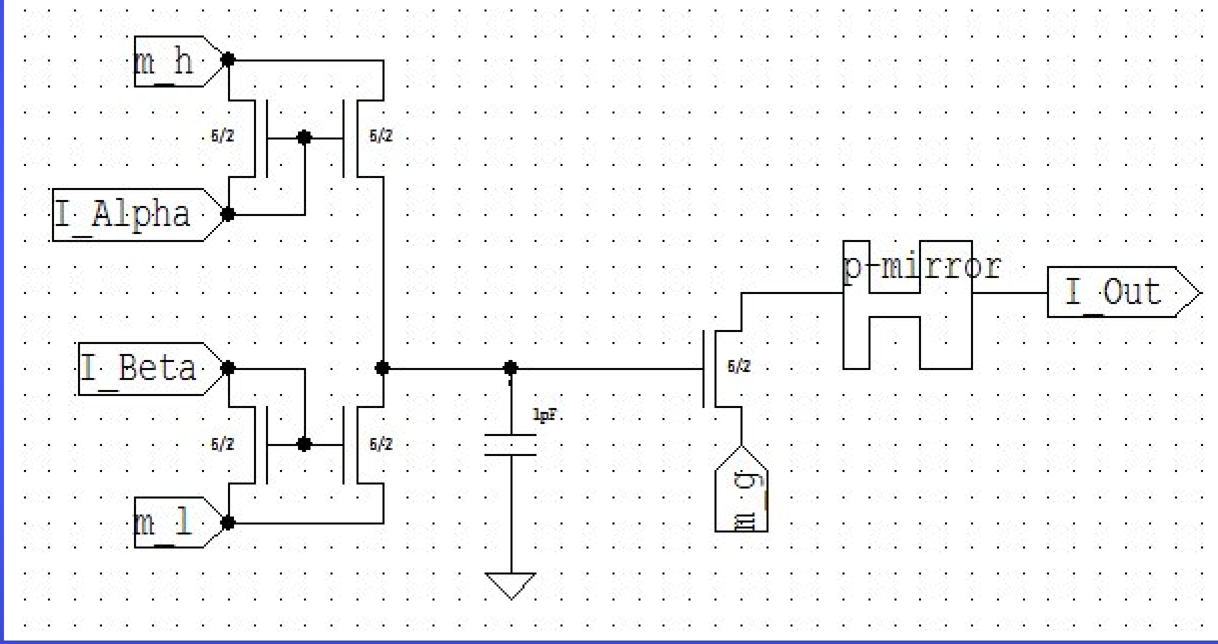

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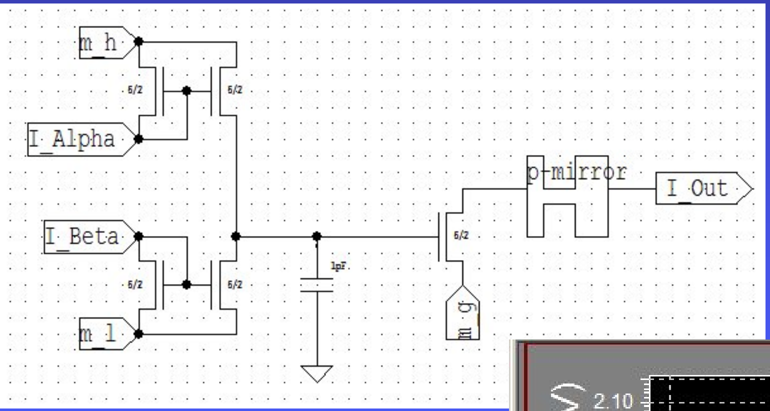
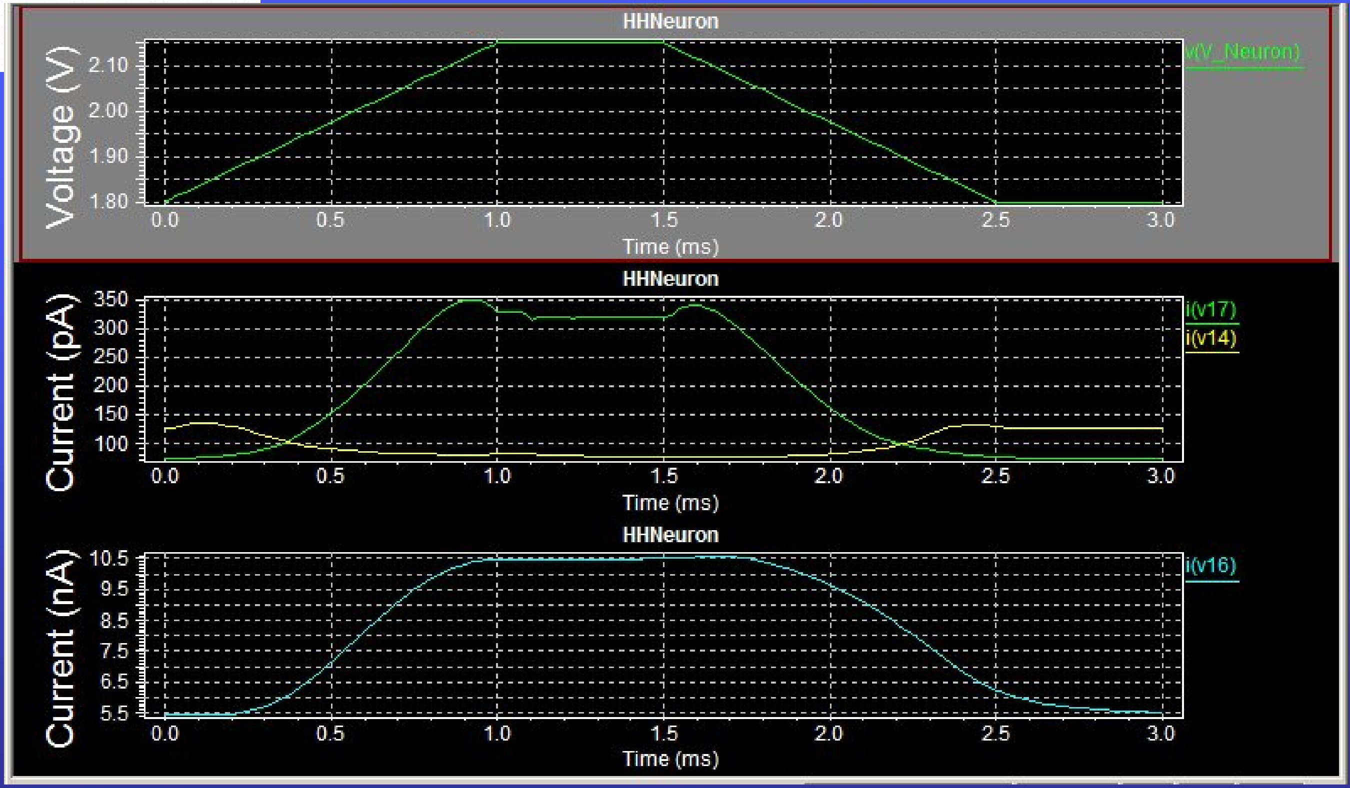
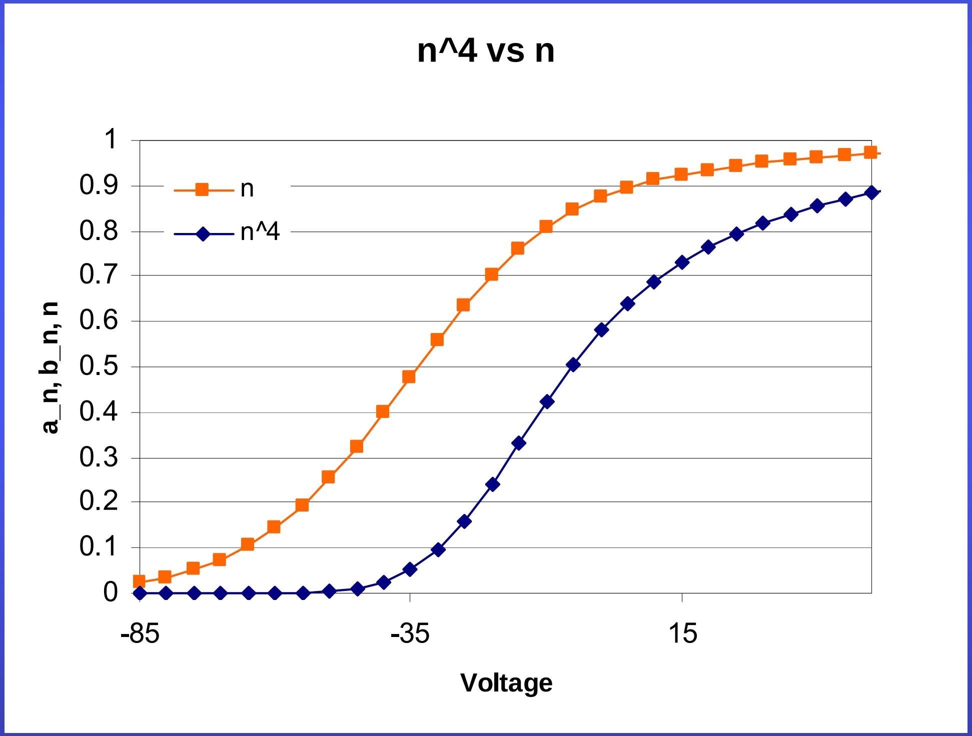




Multiplier circuit

- Need to combine m's, h's and n's into m^3h and n^4



Multiplier circuit

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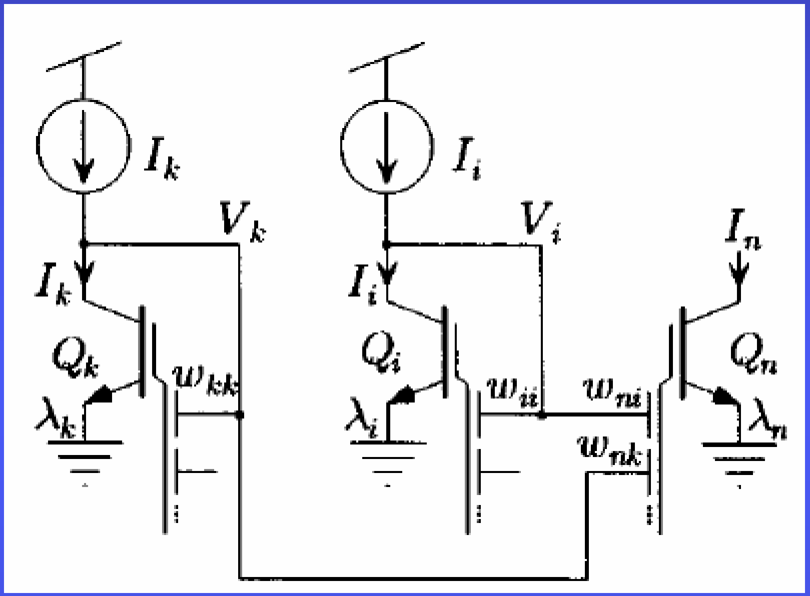
- Can use translinear 'floating gates' to multiply currents

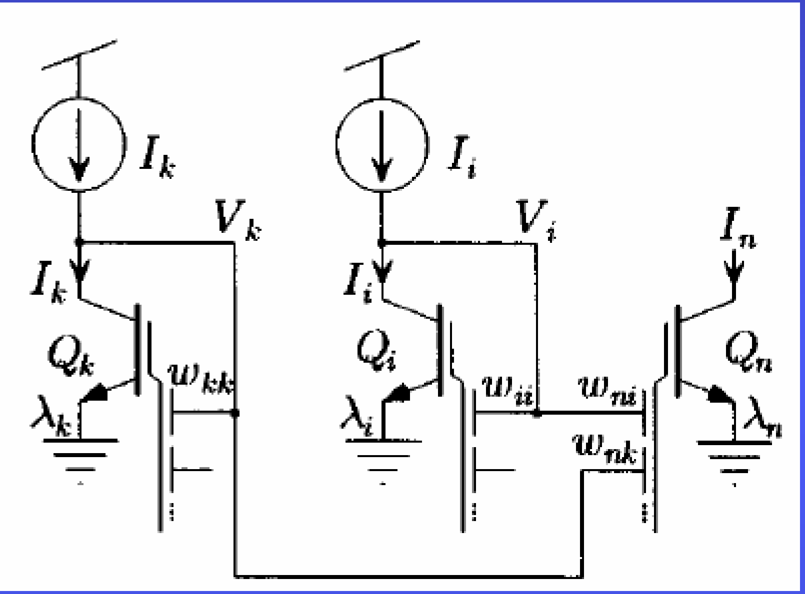


$$I_n \propto I_i^{w_{ni}/w_{ii}} \times I_k^{w_{nk}/w_{kk}}.$$

Minch BA et al., 2001

Multiplier circuit

- Need to combine m's, h's and n's into m^3h and n^4
- Can use translinear 'floating gates' to multiply currents
- diode current charges to capacitors (relative weights are exponents) 'Mirrored' output current is a function of input currents and capacitive differences



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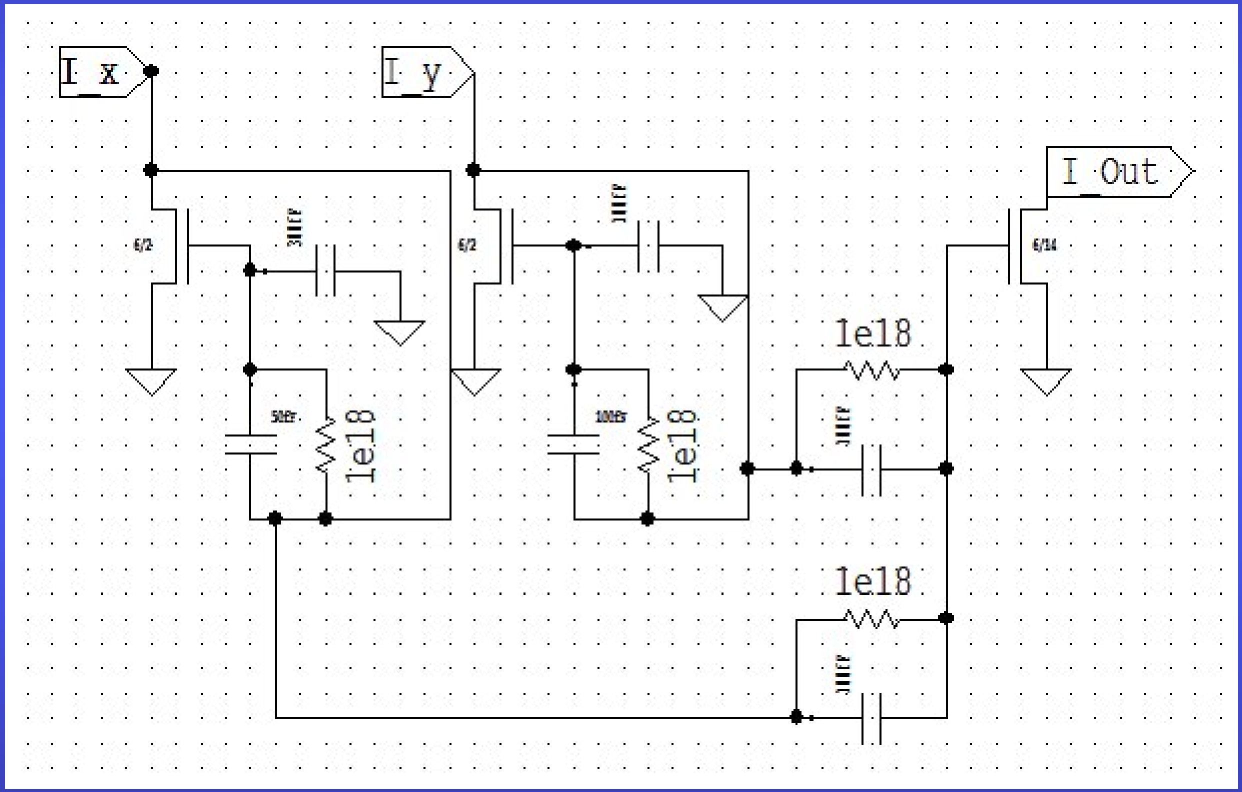

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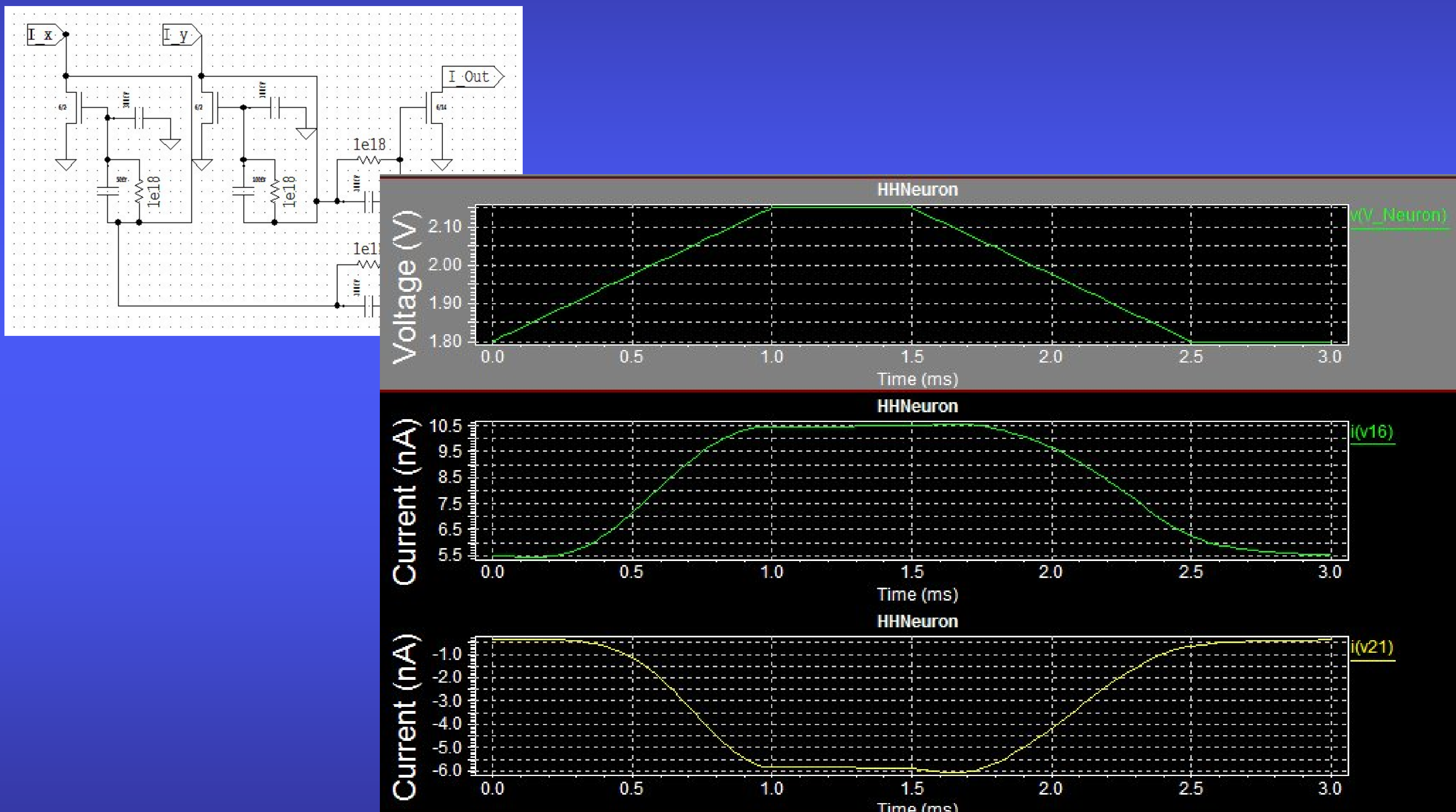
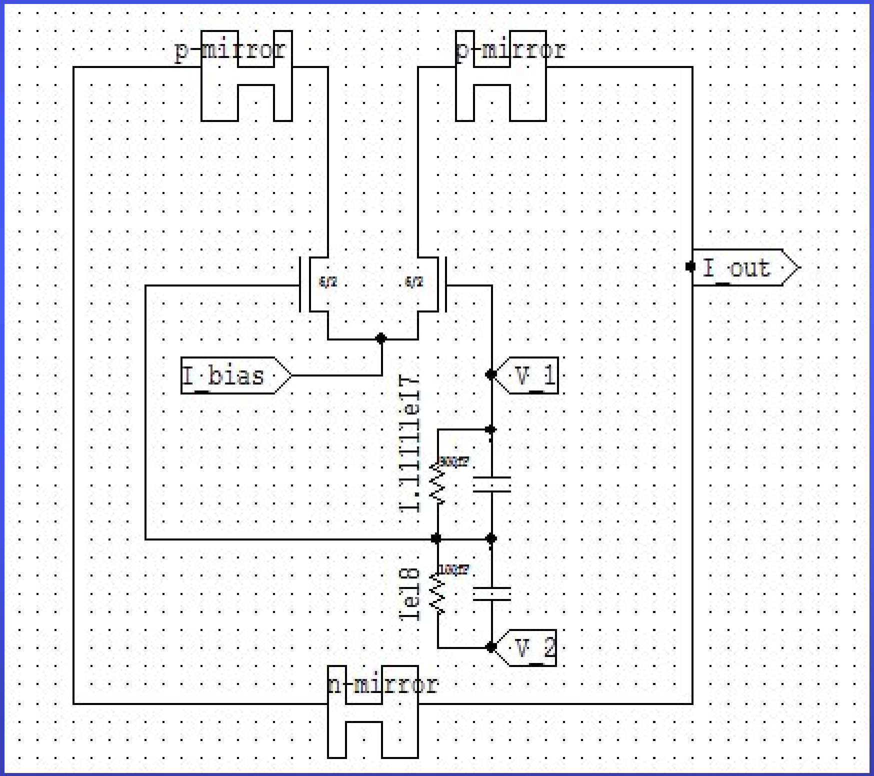
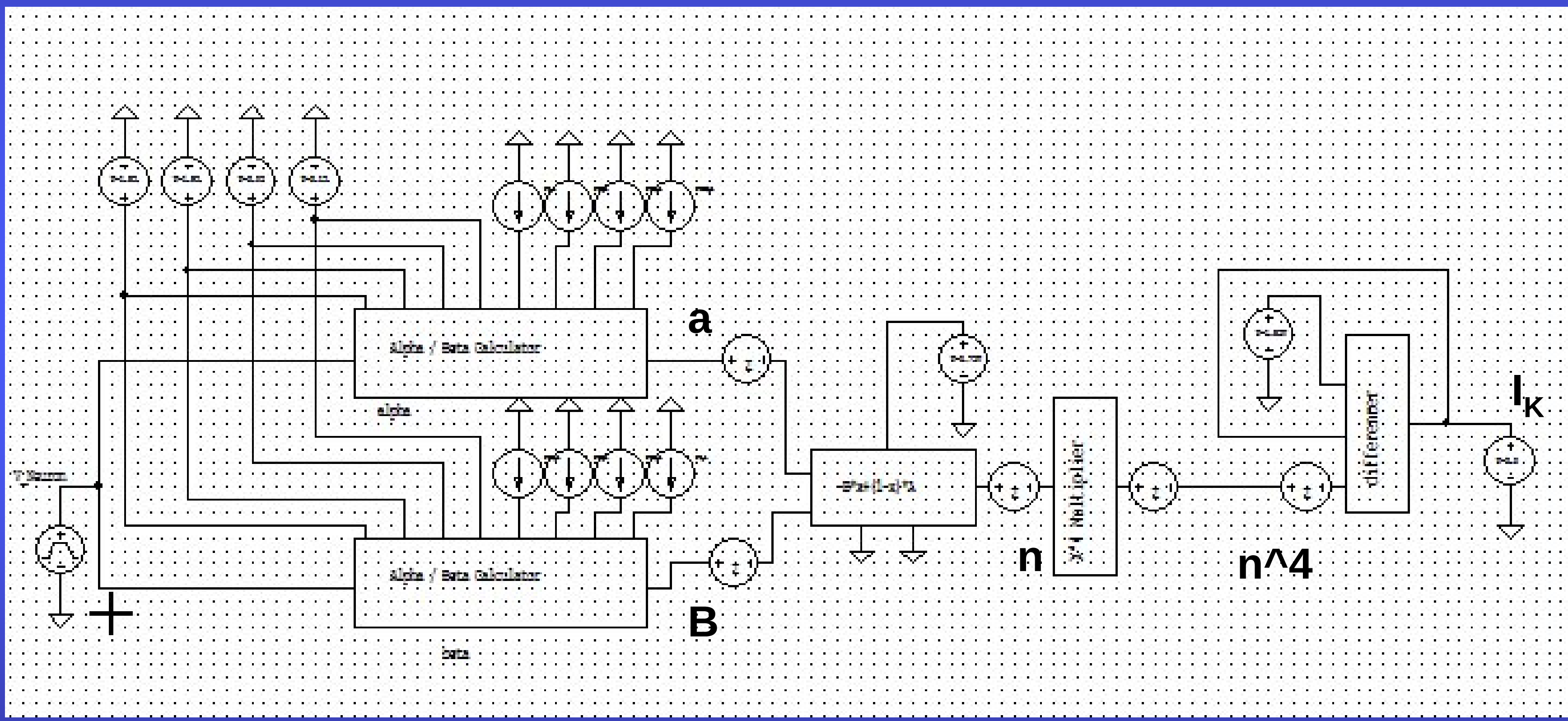


Reversal Potential Scaling

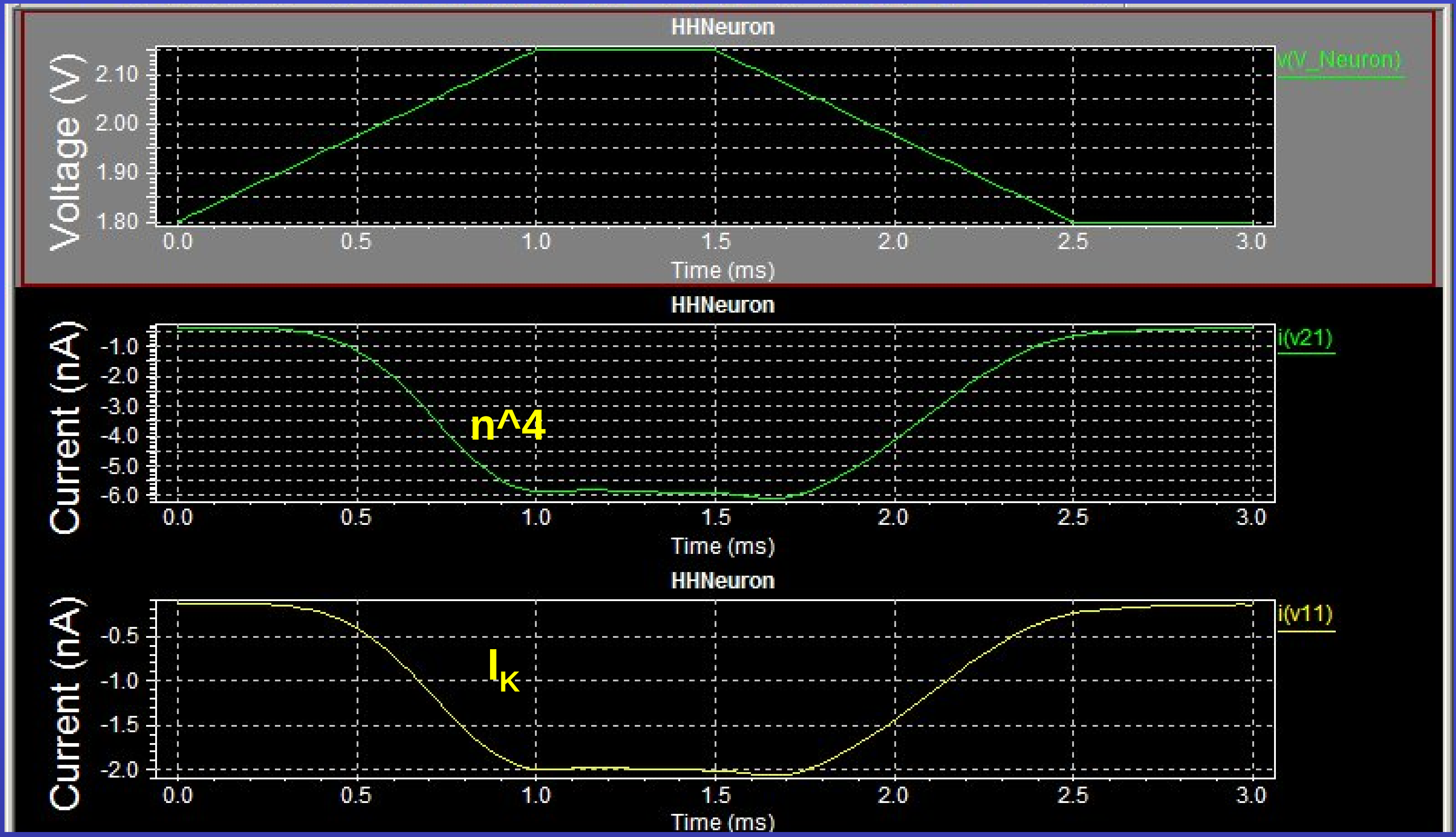
- Current due to conductance and channel states (g_{Na}*m3h and g_K*n^4) weighted by (E_{Rev}-V)
- Implemented by a “transconductance amplifier”



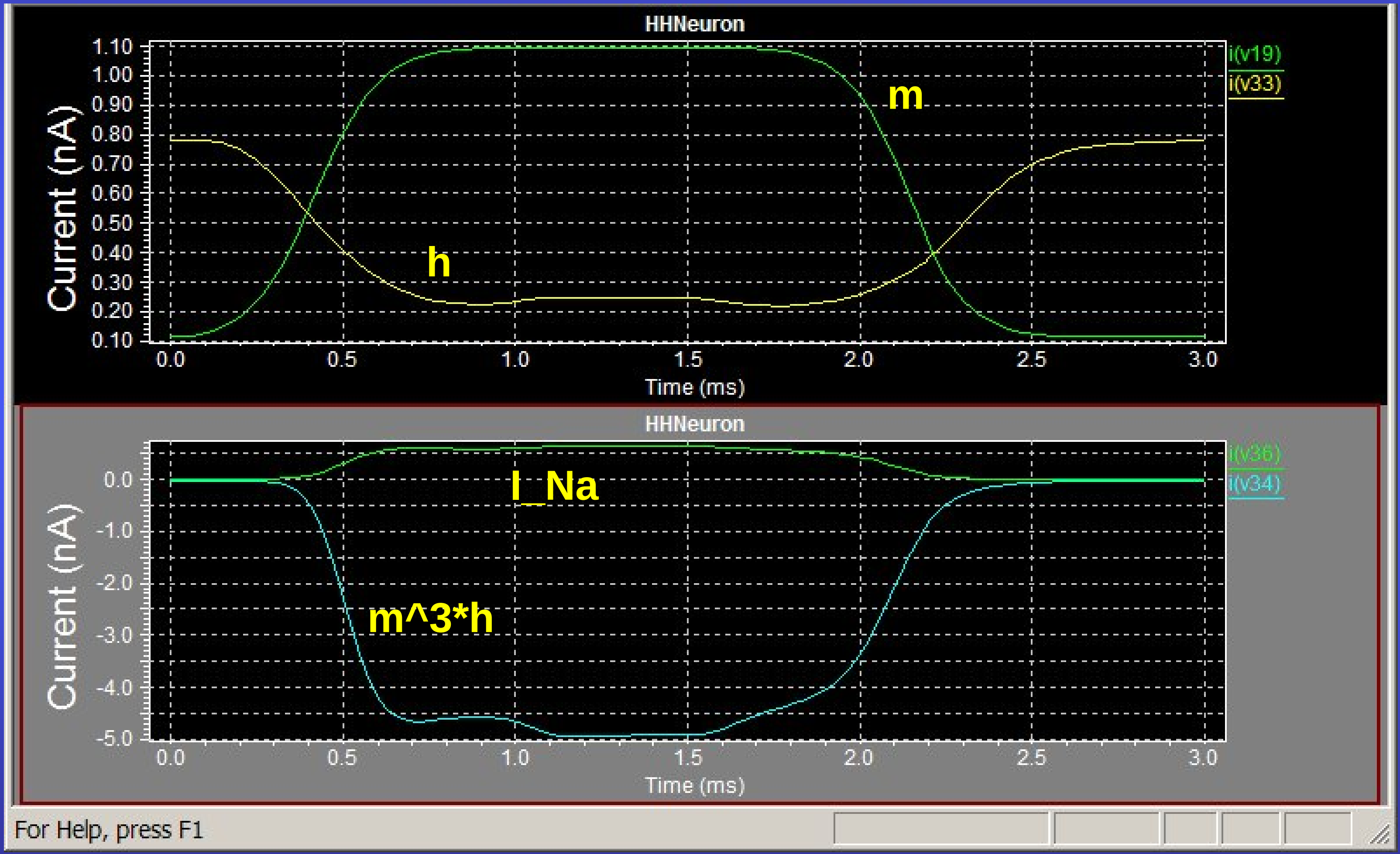
One whole channel



K+ channel simulated

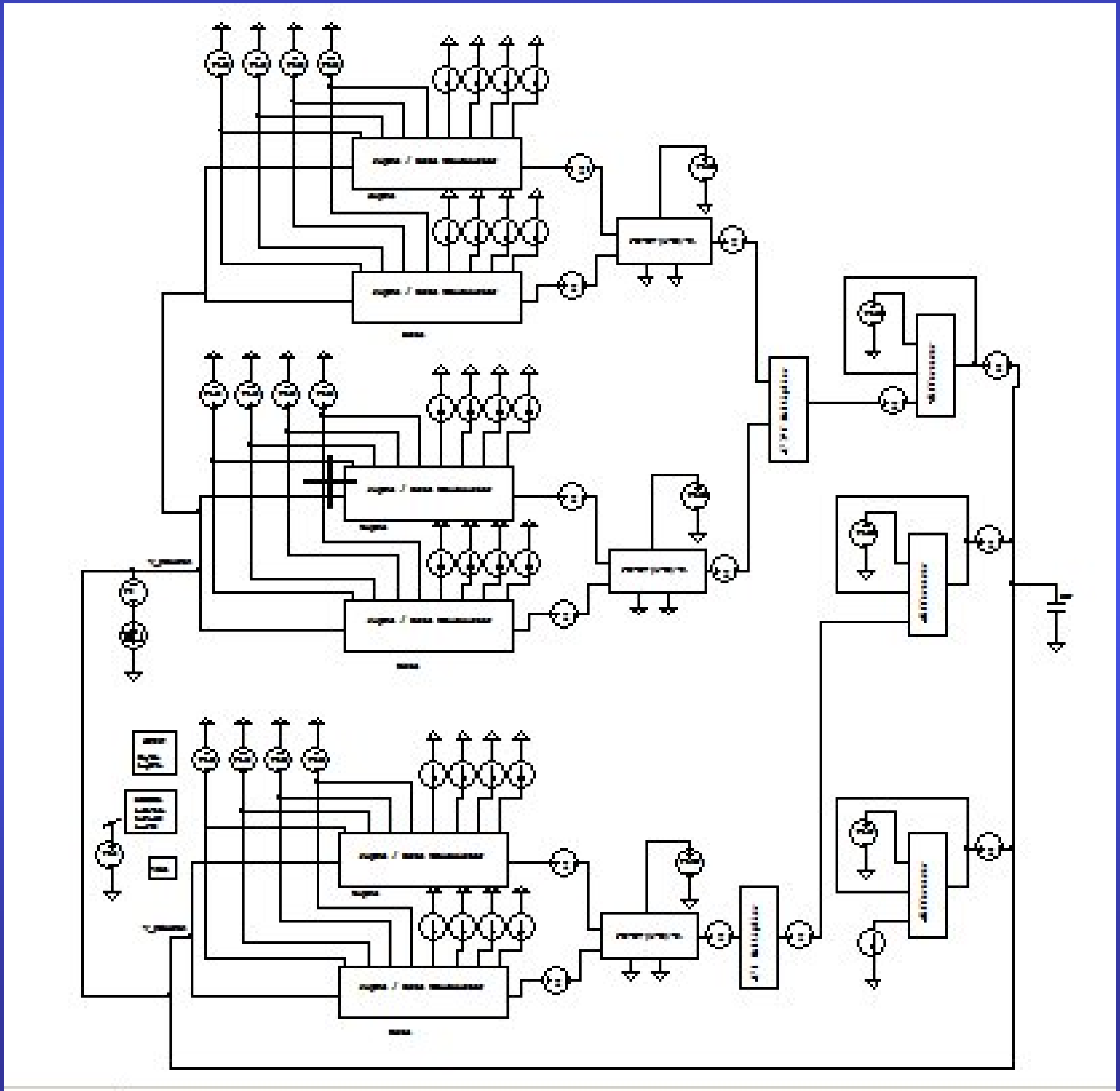


Na+ Channel

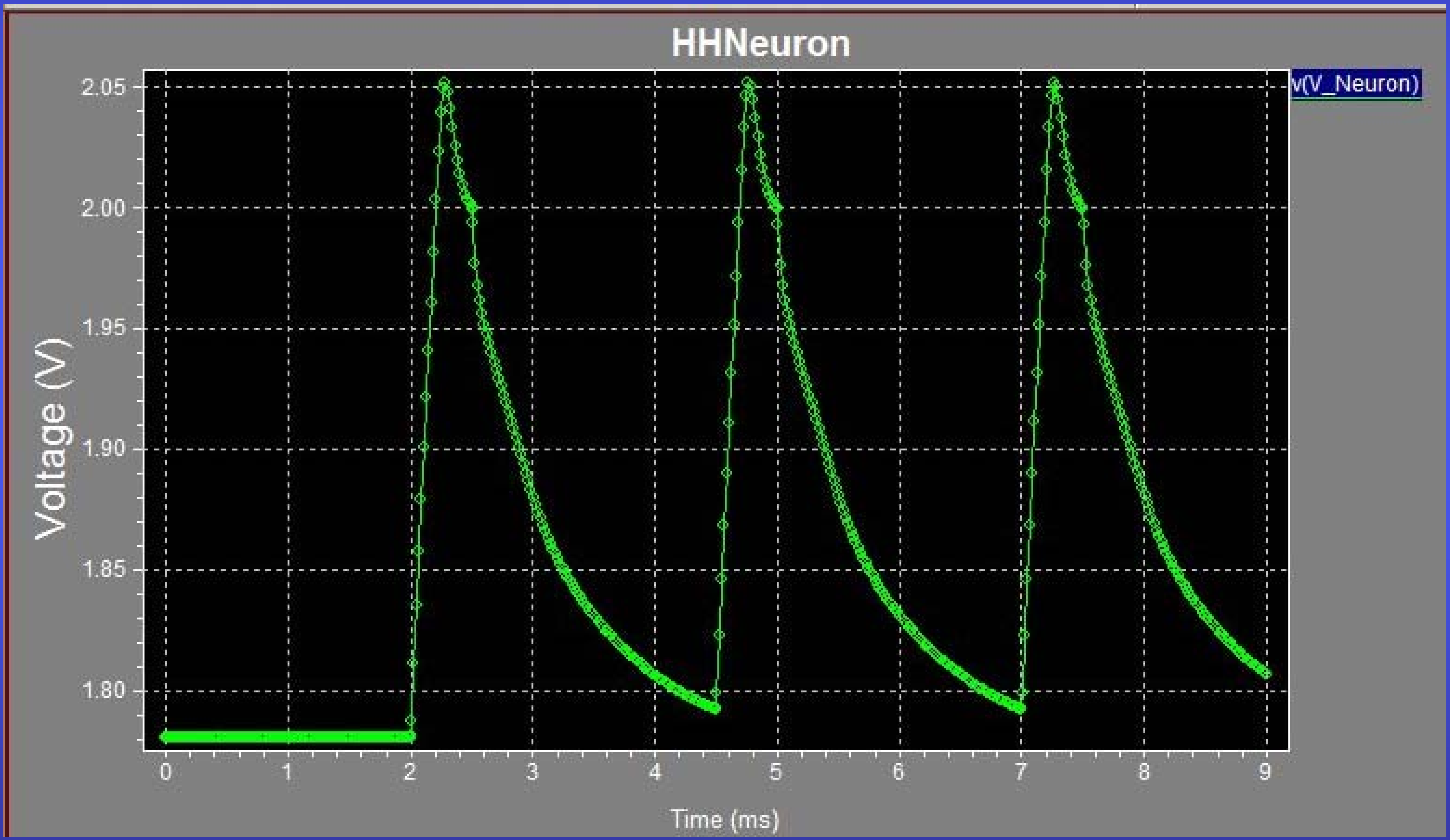


HHNeuron
1.10
1.00
0.90
0.80
0.70
0.60
0.50
0.40
0.30
0.20
0.10
Current (nA)
0.0
0.5
1.0
1.5
2.0
2.5
3.0
Time (ms)
i(v19)
i(v33)
m
h
HHNeuron
0.0
-1.0
-2.0
-3.0
-4.0
-5.0
Current (nA)
0.0
0.5
1.0
1.5
2.0
2.5
3.0
Time (ms)
i(v36)
i(v34)
I_Na
m^3*h
For Help, press F1

Whole Neuron



Whole Neuron



Results & Conclusions

- Designed and Implemented circuits to calculate
  - alphas and betas from voltage
  - m,h, and n from alphas and betas
  - multply m, h, and n's; scale by conductances
  - reference currents to reversal potential and neuron voltage
  - Combine I_{Na}, I_K, and I_{Leak} to simulate neuron dynamics
- Simulated and began to tune parameters to accurately model HH behavior

Future Directions

- Solve remaining dynamical problems
- Optimize bump circuit approximations
  - Generate more accurate a(v)'s and b(v)'s
- Tune other parameters (g_{Na}, g_K, g_{Leak}, capacitors) to optimize HH behavior
- Work on layout of circuit on chip

Special Thanks:
Gert Cauwenberghs
Jon Driscoll

Optimization of Bumps