Spike time-dependent plasticity in VLSI chips.

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Abstract

Recent publications on neural networks on VLSI chips show various neuromorphic circuits featuring spike-time-dependent (STDP) plasticity. These circuits are built in both analog and mixed-domain fashions: sophisticated transistor level circuits, synaptic weights memory look-up tables, digital counters etc. A lot of advancements have been made to mimic the neural networks with the highest number of neurons and interconnecting synapses. The techniques include minimization of the circuit topologies and maximization of energy efficiency. HP Lab's discovery of novel memristive elements resulted in very compact and energy efficient memristive synapse implementations. The paper introduces conceptual STPD circuit implementations in neural VLSI chips, then develops mathematical foundations of novel memristive synapse and provides simulation results and discussion.

1 Classical neuromorphic circuits with spike-time-dependent plasticity.

1.1 Neuron implementation in VLSI chips

The classical way to implement the spiking behavior of neurons similar to those seen in mammalian brains is to use a leaky integrate and fire model demonstrated in Figure 1 as described in [1] and later generalized to a non-linear form with various peaking waveforms [2].

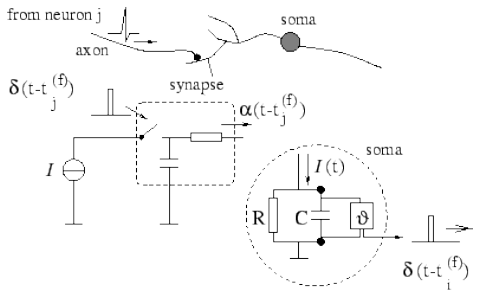

Figure 1. Leaky integrate and fire (I&F) neuron [1]

Current *I(t)* charges the capacitance *C* in the *RC* tank biased at the voltage, corresponding to the *K/Cl* ionic resting potentials. The comparator-switch represented by a block v compares the potential on the capacitor and triggers rapid discharge through a switch as soon as the threshold is reached. Typical waveforms are shown in Figure 2 below.

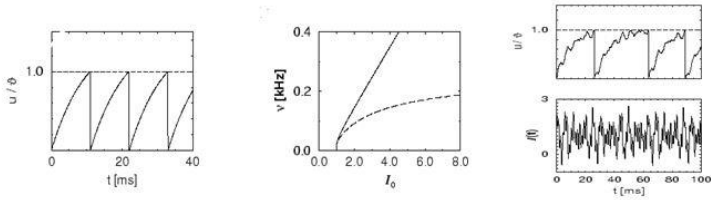

Figure 2. Typical waveforms [2] present in the leaky integrate and fire neurons. a) shows the potential across the capaciatence as the input current is integrated and switch activated after the threshold. b) demonstrates the spiking frequency dependancy on the input current and c) shows the effects of time-varying feed current.

1.2 Spike time-dependent plasticity (STDP)

The primary mechanism of learning in neural networks is due to synaptic structure adaptations. Spike time-dependent plasticity is one of the mechanisms that changes the conductance level of the synaptic strengths depending on the relative timing of the pre and post neurons. Effectively, STDP creates a path of the strong stimuli to propagate through the neural network. STPD can be seen as an extension of the Hebbian learning rule that postulates that the synapse is strengthened if there is a causal relationship between firing of two neurons. Hebb's model does not take into account the synaptic weakening that was postulated by Stent. The combination of the strengthening and the weakening within the short time frame with accordance with specific rules (see [1]) is what is usually referred as STDP.

1.3 Neuromorphic circuits featuring STDP

There are multiple levels of abstractions that can be applied to neuromorphic circuits, depending on the scale of implementation: program architecture level, where the neurons are described in software on a fixed hardware, hardware architecture level, where the neurons are comprised of the fixed circuit elements and reconfiguration happens on the wiring level of the components, and finally, electronic component level, where the plasticity and adaptation are implemented as a physical change occurring inside of the nano-scale devices. As the transition goes to lower levels, it generally is associated with more dense systems with smaller sized neurons and synapes, and featuring lower power operation and dissipation and overall greater efficiency.

Recent trends in miniaturizing consumer electronics (wearable and mobile devices) as well as race for the efficiency in data centers and other corporate infrastructures while increasing the computational and intelligence levels can benefit from ultra-dense neuromorphic circuits. This means that innovation in electronic component level is one of the driving factors in enabling the future generations of smart devices.

2 Memristive implementation of network synapses

The memristive element first introduced in 1971 by Leon Chua as a predicted fourth elementary component relating flux and charge and later generalized to mathematical state variable definition is governed by the following equations:

$$V = R(x, i) \cdot i$$

$$\frac{dx}{dt} = f(x, i)$$

For more details on the definition of memristive devices see [3].

The key takeaway extracted from the model above can be condensed to two memristor "fingerprints":

1. The hysteresis loop on the I-V characteristic plot will always include the point (0,0) (and is referred as pinched hysteresis loop).
2. The area enclosed in the loop decreases as the excitation frequency increases.

2.1 Memristor device discovery

In 2008 HP Labs have successfully fabricated the device that features memristive properties.

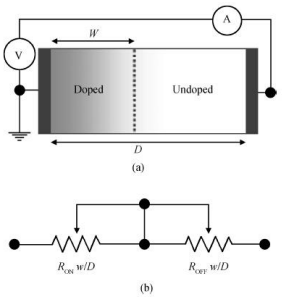

Figure 3. Memristor discovered in HP Labs

The undoped region is made of Tinanium Dioxide (good insulator), and the doped region is the oxidized Titanium Dioxide (becomes a semiconductor). When the voltage is applied across the device, the boundary between the doped and undoped region shifts, and if no voltage is present then the boundary will effectively stay at the same level. To understand how the device above works let's take a look at the governing equations:

$$R_{mem} = R_{ON} \cdot x + R_{OFF} \cdot (1 - x)$$

The resistance seen across the memristor consists of the resistance of the ON semiconductive doped region and OFF undoped isolator.

$$\frac{dx}{dt} = k \cdot i(t) \cdot f(x)$$

$$k = \frac{\mu_v \cdot R_{ON}}{D^2}$$

The dynamics of the boundary x depends on the k-factor describing the mobility of the dopant and the non-linear dopant drift f(x).

$$f(x) = 1 - (2x - 1)^{2p}$$

The non-linear drift is caused by the potential difference across the terminals that create significant E-field in the device due to the nano-scale distances beween the ports. It is also referred as a window finction and should include the boundary drift lower and upper bounds (the boundary of doped and undoped region cannot cross the boundaries of the device itself). The f(x) proposed above satisfies these conditions for any positive value p.

2.2 Memristor model in SPICE

LTSPICE IV is used as a primary SPICE simulator as free and reliable tool. Based on the memristor model dynamics introduced earlier the SPICE model is formulated after work published in 2009 [7]. The window function used is chosen to be after Joglekar09.

To quickly verify the operation of the modelled device the fingerprint has been checked:

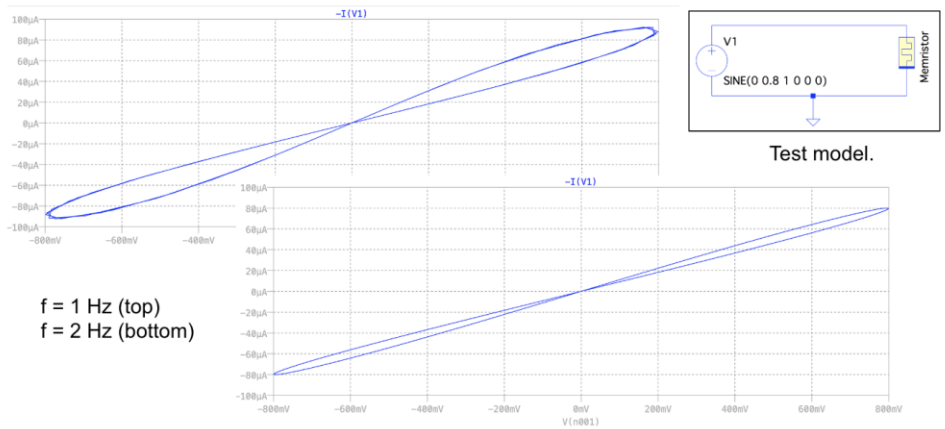

Figure 4. Memristor SPICE model verification.

The typical pinched hysteresis loop with the area dependent on the frequency of operation means the model is correct and the necessary adjustments can include the change of initial conditions.

2.3 Memristive neuromorphic synapse

With the working model developed for SPICE environment, the circuits that involve memristors are now convenient to simulate. There are several implementations of synapses that possess STDP and involve memristors. From the density and energy efficiency standpoints, the optimal configuration consists of just a single memristor. It can be manufactured in the nano-meter scale and does not require and biasing currents minimizing the leakage and dynamic power that are generally associated with more sophisticated circuits.

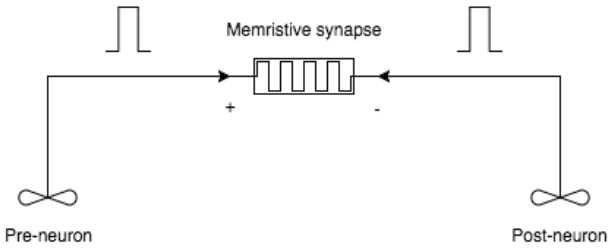

Figure 5. Single memristor plastic synapse

The single memristor synapses are usually arranged in the "crowbar" structures shown in the Figure 6 below.

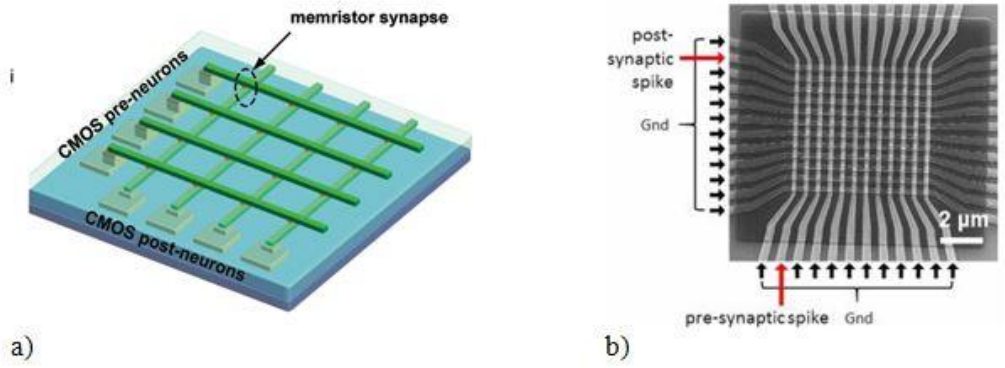

Figure 6. a) "crowbar" memristive-synaptic structure b) fabricated "crowbar"

2.4 Single memristor model verification setup

Several assumptions regarding the spiking patters are made to simplify the simulation of the synaptic plasticity. Figure 7 shows the potentials of the pre-synaptic neuron and the post-synaptic neurons along with the difference between the two that represents the net potential across the memristor.

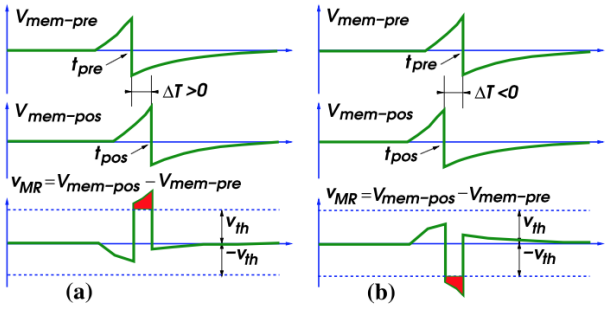

Figure 7. Voltage appearing across the memristor. Figure 2(a) corresponds to the potentiation scenario and Figure 2(b) corresponds to the weakening scenario.

The waveforms chosen as the typically present in I&F type neurons. The voltage drop across the memristor can be simplified to the pulse. The width of the corresponding positive and negative pulses as shown on Figure 8 correspond to the relative arrival times of the spikes. The DC bias is optional and was included to mimic the real system with higher precision.

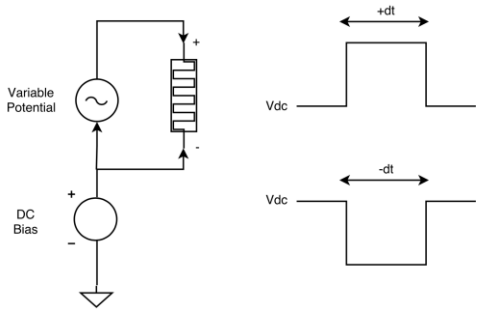

Figure 8. Potential across the memristor for pre arriving first (on top) and last (on the bottom).

In this work, only one type of time-dependent plasticity is considered. The recently published work [5] considers waveform shaping of the pre and post synaptic potentials to observe various behaviors of STDP. Their findings are summarized on figures 9 and 10 below.

It is also important to note that the actual timings that are typically present in the biological systems are not of the most importance as long as the neural synapses are scaled to the corresponding time-frame.

2.5 Single memristor synapse simulation results.

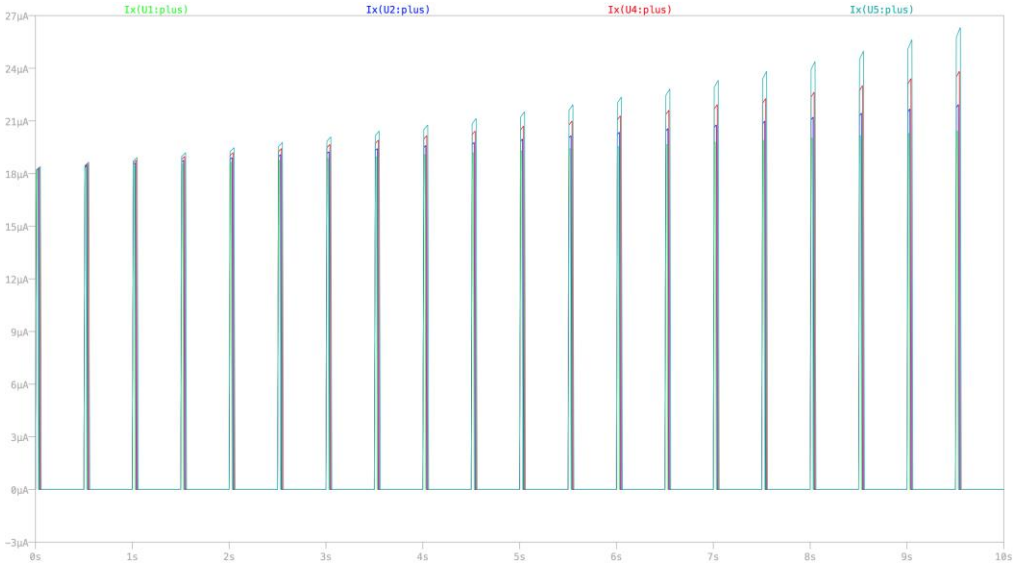

Figure 9. Potentiation of the synaptic strength. Pre neuron spiking first.

Firgure 9 shows the conductance in terms of the current due to the same excitation voltage. As seen on the plot, the green waveform (corresponding to the widest pulse width) shows the fastest rise in time. Smaller pulse widths experience less conductance improvements. Generally speaking, it is consistent with the classical SPDT model.

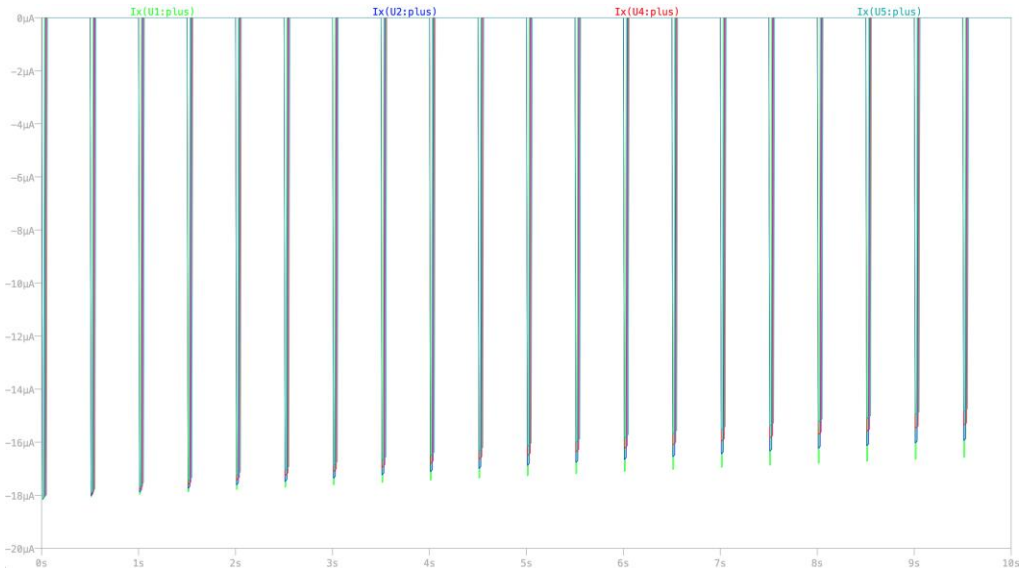

Figure 10. Weakening of the synaptic strength due to post neuron firing first.

Firgure 10 shows the conductance in terms of the current due to the same excitation voltage. As seen on the plot, the green waveform (corresponding to the narrowest pulse width) shows the slowest fall in time. Wider pulse widths experience more conductance weakening. Generally speaking, it is consistent with the classical SPDT model.

The first order verification of the possibility of spike time-dependent plasticity is presented in Figures 7 and 8. It is not completely correct to assume that the pulses are always of the square

shape as the shape will change significantly in the periods where relative timings are not as well timed. It is a crude approximation that had to be done to get the project completed within the given timeframe.

3 Simulation results and future considerations

3.1 Single memristor synapse results

The simulations show that single memristor synapse possesses spike time-dependent characteristics and has potential in realizing neuromorphic circuits.

While preparing this paper another resent research results [5] were found where the researches have used an extended approach to the potential reconstruction across the memristive synapse. The key implementation that allows the implementation of various spike time-dependent mechanisms found in the biological system is in the construction of the spiking shapes in the pre and post-synaptic neurons. The summary of the findings are reprinted in Figure 11. The shape considered in this paper is demonstrated on Figure 11a, which results in the SPDT pattern shown in Figure 11g, that is consistent with the results found in this paper.

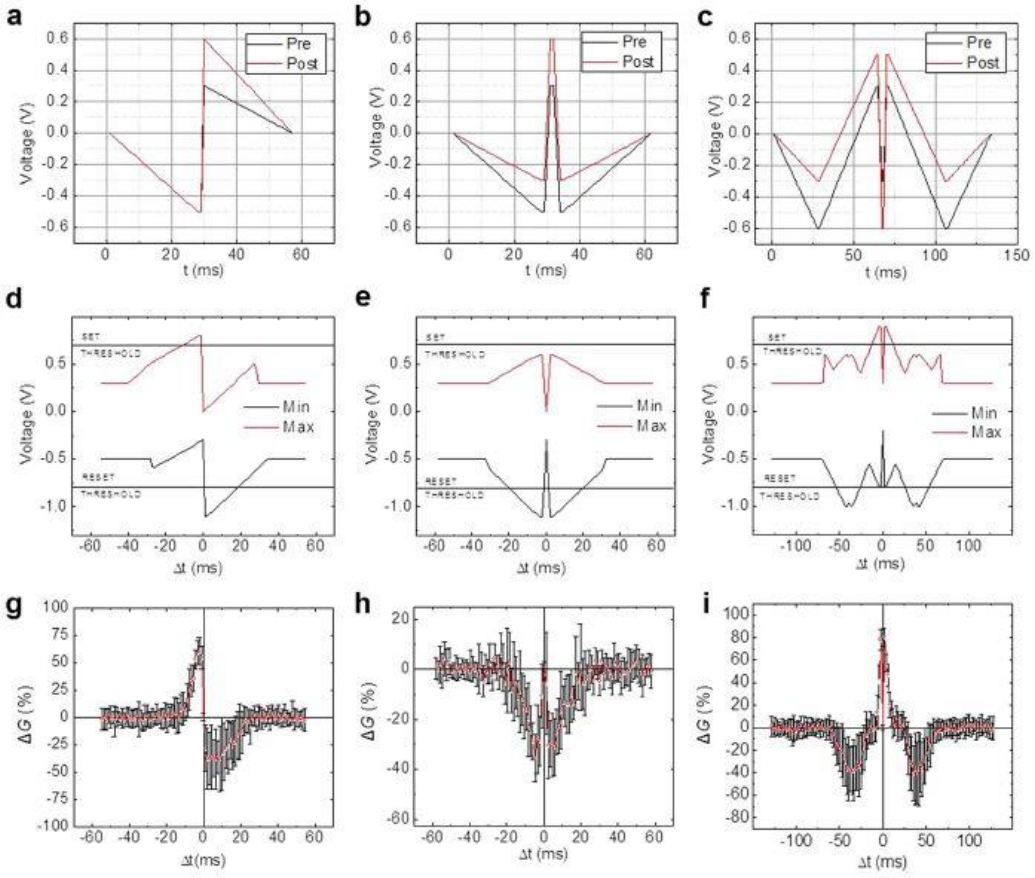

Figure 11. Spike waveform engineering to demonstrateall various types of STDP present in the biological systems.

3.2 Future directions

Having verified the properties that make memristors a convenient tool in building largely integrated synaptic connections, a more detailed analysis must be made regarding how the conductance changes with various types of spiking waveforms.

Fully memristive neuron and synapse pairs is another area that has to be researched to reach for the optimum power and density characteristics.

Acknowledgments

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