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A translinear SiGe BiCMOS current-controlled oscillator with 80 Hz–800 MHz tuning range

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Abstract A 3-phase current controlled sinusoidal oscillator, tunable over a wide range of frequencies is presented. The oscillator comprises a ring of 3 cascaded differential $G_m - C$ low-pass filter stages, implemented in a fully translinear, NPN-only circuit. Closed-form analytical expressions are derived to quantify both frequency and amplitude tuning, as a function of two current biases. Experimental results from a 0.5 μm SiGe BiCMOS chip demonstrate 7 decades of tuning range, from 80 Hz to 800 MHz, as well as low harmonic distortion. Power consumption scales with oscillation frequency, measuring 2 μW/MHz The circuit serves a range of applications including agile communications, analog built-in self-test, stochastic adaptive control, spectroscopy, and bioinstrumentation.

Keywords Current-controlled oscillator · Translinear circuits · Amplitude and frequency control · SiGe BiCMOS · RF circuits

1 Introduction

Oscillators tunable over a wide range of frequencies find use in various applications extending from communications and built-in-test to biology and biomedicine. Depending on the actual application, typical requirements are multi-decade tuning range, high (hundreds of MHz to GHz) maximum achievable frequencies, short and/or long-term stability, linearity, low power, fast frequency tuning, and a simple, compact design amenable to high-density integration. Focusing on on-chip solutions, high-Q resonant devices such as Surface Acoustic Wave (SAW) resonators or crystals, that can only be incorporated as off-chip elements, have to be excluded from consideration. Moreover, setting as priority a high tunable range over low phase noise, rules out the option of *LC* tanks, for which tunability ranges of up to generally just an octave have been demonstrated [1, 2].

Exploring alternate on-chip oscillator configurations, a first-order classification can be made according to the nature of the frequency control: voltage or current. The three most common voltage-controlled oscillator (VCO) topologies that have been mainly exploited, include relaxation VCOs, adjustable delay ring oscillators as well as delay-interpolating ring oscillators [3]. Multiple decade (typically 4–5 decades) frequency control has been demonstrated with both relaxation [4, 5] as well as ring oscillators [6, 7]. Although the reported maximum frequencies for these oscillators extend to hundreds of MHz or even low GHz, these architectures generally suffer from high power consumption and high phase noise. A different VCO approach was proposed in [8, 9], where wide tunable gain current mirrors set the gain of transconductors and consequently the frequency of oscillation in a two-integrator $G_m - C$ topology. A tuning range of 7 decades was achieved, however the maximum frequency was limited to 1 MHz.

Widely tunable current controlled oscillators usually employ translinear circuits and make use of the linear proportionality relation between bias current and transconductance in bipolar junction transistors (BJT), valid

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over multiple decades. Proposed designs include two $G_m - C$ integrators configured as quadrature sinusoidal oscillators [10–12], coupled all-pass filter topologies [13, 14] as well as architectures based on current controlled conveyors [15, 16]. A main advantage of current controlled compared to voltage controlled oscillators is typically lower power consumption, which scales linearly with the oscillation frequency. Reported frequency tuning ranges vary from 3 to 5 decades, however, maximum achievable frequencies generally do not exceed a few tens of MHz. The broadest operating range for a current controlled oscillator was reported in [17], where the dynamic translinear principle was applied in order to implement a second-order oscillator achieving a tunable range that exceeded 6 decades.

The current contribution extends this previous work with the design and implementation of a current-controlled 3-phase oscillator combining high maximum attainable frequencies with low power and ultra-wide frequency tuning range, in a fully integrated circuit of low complexity. The circuit is based on translinear networks and a SiGe BiCMOS process has been selected for its fabrication in order to achieve a high maximum frequency of oscillation. To avoid the slower response of PNP bipolar junction devices, the design targets the exclusive use of NPN bipolar junction devices in a fully differential and symmetrical architecture, for high frequency operation and low distortion. Amplitude control based on inherent circuit nonlinearities is achieved through an external biasing current.

Examples of applications that benefit from the oscillator design are given in Sect. 2. The general system architecture is presented in Sect. 3, while Sect. 4 introduces the actual circuit implementation. Analytical expressions for the frequency and amplitude of oscillation are derived in Sect. 5 and experimental results are demonstrated in Sect. 6. Section 7 closes with concluding remarks.

2 Applications

Applications of the oscillator circuit abound in communications, analog built-in self-test, multi-dithering adaptive electronics, and biomedical instrumentation. Some examples are given below.

2.1 Agile frequency hopping in communications

The current trend towards transceivers able to operate with multiple telecommunication standards at different bands requires the ability of multiple frequency generation on a single chip. Power as well as area constraints prohibit solutions with one oscillator per band and interest has shifted towards widely tunable oscillators (e.g. [18–20]). An extra challenge is added when frequency hopping within the same band is required by the communication protocol (e.g. for spread spectrum techniques), asking for agility within the tuning range of the oscillator. Current-controlled multi-decade tunable translinear oscillators can be considered candidates for such applications, however, additional care needs to be taken for suppressing phase noise.

Phase-locked loops (PLLs) mitigate the problems with direct current control of the oscillator. Embedding the current-controlled oscillator in a PLL offers both advantages of digital tuning of frequency, and reduction of the intrinsic oscillator phase noise. With careful design of the PLL loop dynamics, the resulting phase noise is limited mainly by the jitter of the digital clock controlling the PLL.

2.2 Analog built-in self-test

Oscillators with both amplitude and frequency control, tunable over multiple decades can find fertile ground in testing and system fault diagnosis. Test equipment cost as well as signal distortion due to parasitic loading and coupling from the probes has led to integration of testing circuitry on the same die as the actual system [21–23]. Built-in self-tests (BIST) significantly expedite characterization of systems-on-chip (SoC) and their building blocks as well as spot defects and process variations. Compact, low power and widely tunable designs of generators are more attractive due to the reduced area and power overhead as well as the ability to characterize over broader frequency ranges.

One of the many applications of analog BIST is characterization of the frequency response of an integrated analog filter DUT (device under test). For this purpose, the oscillator provides wide-range sinusoidal excitation of the filter DUT input. Both magnitude and phase of the frequency response of the filter DUT output are estimated by synchronous (or coherent) detection. Comprising a mixer and lowpass filter in conjunction with a 3-phase oscillator as illustrated in Fig. 1, the synchronous detector performs down-conversion of the filter DUT output. Since the same oscillator input provides the filter DUT input as well as the reference in the mixing of the filter DUT output, phase noise in the oscillator has limited effect on the frequency response measurement. Furthermore, all three (equally spaced) phases of the oscillator are available as reference in the mixer, yielding redundant estimates of the magnitude A and phase ϕ of the frequency response:

$$\begin{aligned} SD_0 &= A \cdot \cos(\phi)\sigma^2 \\ SD_{2\pi/3} &= A \cdot \cos(\phi + 2\pi/3)\sigma^2 \\ SD_{4\pi/3} &= A \cdot \cos(\phi + 4\pi/3)\sigma^2 \end{aligned} \tag{1}$$

where SD_0 is the synchronous detection output for a phase selection in the mixing identical to the phase selected for

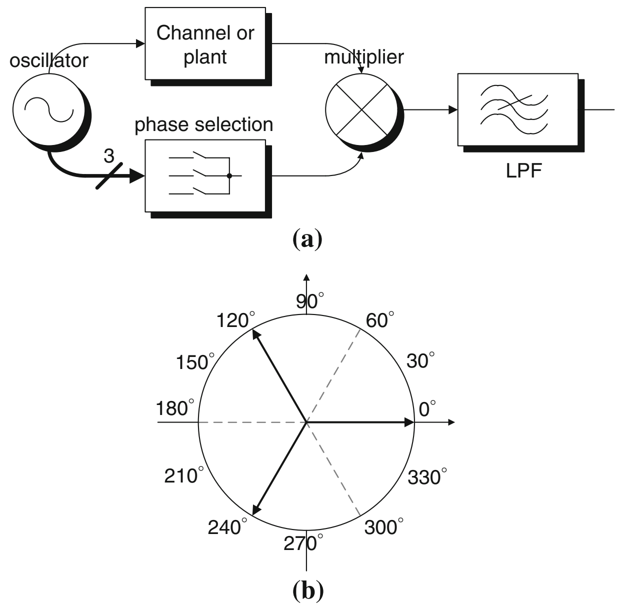

Fig. 1 Synchronous detection using a three-phase oscillator. (**a**) System diagram. (**b**) Phase diagram for different phase selections in mixing

the filter DUT excitation, and where $SD_{2\pi/3}$ and $SD_{4\pi/3}$ are the synchronous detection outputs at relative phase selections $2\pi/3$ and $4\pi/3$, respectively. σ^2 represents the product of the excitation signal and mixing reference signal magnitudes (not necessarily equal). In principle, only two of the measurements (1) are needed to estimate the two parameters A and ϕ; in practice least-squares estimation including the additional third measurement improves robustness to measurement noise.

2.3 Multi-dithering adaptive control

Widely tunable oscillators find also use as part of synchronous detection schemes in adaptive controllers. Known in the adaptive optics research community as multi-dithering [24], parallel sinusoidal excitation across multiple control channels allows for precise 'model-free' estimation of the gradient of a performance metric, such as beam quality or image quality affected by atmospheric phase abberations and corrected using a spatial phase modulator [25]. In [26], a fully tunable controller architecture has been proposed implementing multi-channel gradient descent optimization through parallel coherent detection for an optical phased array. Operation relies on the superposition of small-amplitude sinusoidal signals on the actual control. Each element of the array is excited by a different frequency and the frequencies are chosen according to the bandwidth of the variations in the system. Note that in this particular application, the immunity of synchronous detection to phase noise loosens the constraints of spectral purity for the excitation sources. Furthermore, the narrowband nature of the excitation signals reduces effects of propagation delays in the plant and in the gradient estimation to a single phase parameter per channel, adaptively estimated jointly with the gradient estimation for delay-insensitive control [27].

Gradient estimation in the implementation of the multi-dithering control architecture amounts to multi-channel dithering and parallel synchronous detection, as a parallel extension to the architecture in Fig. 1 further implemented in SiGe BiCMOS integrated circuits [28]. A robust constant-slope version of continuous-time gradient descent is implemented by a comparator and a charge pump provided in each channel acting on one of the control variables.

2.4 Spectroscopy in bioinstrumentation and biomedicine

Oscillators able to sweep in a multi-decade range find applications also in other fields, such as biomedicine or nuclear magnetic resonance (NMR) spectroscopy. In [29, 30] a sinusoidal source generating signals from 1 kHz to 10 MHz was used in order to stimulate dielectrophoresis and electrorotation phenomena in yeast cells and study their ac electrodynamics. An NMR spectrometer based on homodyne detection was proposed in [31], where an oscillator source sweeping from 10 MHz to 1 GHz was employed in order to display the distribution of effective fields at different nuclei in ferromagnetic materials.

The above are just a few examples of the many applications, combining the oscillator with integrated mixers or other detectors compatible with implementation in the same SiGe BiCMOS circuit technology.

3 Architecture

A block diagram of the proposed 3-phase oscillator is shown in Fig. 2. It consists of three identical modules approximately acting as single pole low-pass filters. In steady-state operation each module has unity voltage gain and introduces a phase shift of 60° in the loop at the frequency of oscillation. The additional 180° phase shift needed for oscillations is provided by signal inversion at the output of each module. Considering the signals across

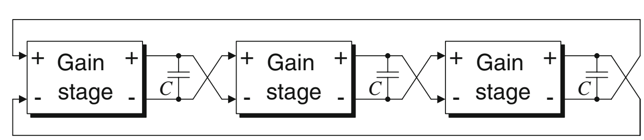

Fig. 2 Block diagram architecture of the proposed 3-phase oscillator. Cross-coupled single-pole low-pass filters provide a total phase of 360° at the frequency of oscillation

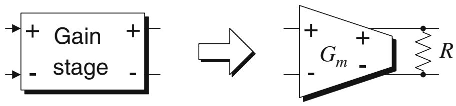

Fig. 3 Implementation of a linear gain stage using a cascade of a linear transconductor G_m and a linear resistor R

the capacitors as the (three) outputs of the oscillator, the generated three phases are equally spread in the phase domain and 120° apart.

As an initial approach and in order to gain better intuition in the principle of operation, the gain stages are considered linear, and more specifically as cascades of a linear transconductance G_m and a linear resistor R (Fig. 3). Actual circuit implementation and nonlinearities in these components will be addressed in the next section. Each $G_m - R - C$ low-pass filter module exhibits a gain of

$$|H(j\omega)| = \frac{G_m R}{\sqrt{1 + (\omega RC)^2}}$$

and contributes to the loop a phase of

$$\angle H(j\omega) = \tan^{-1}(-\omega RC)$$

Applying the Barkhausen oscillation criterion (unity open loop gain and $2\kappa\pi$ total phase), the following conditions for oscillation are derived

$$G_m \cdot R = 2 \tag{2}$$

$$\omega = \frac{\sqrt{3}G_m}{2C}. \tag{3}$$

According to (3), the frequency of oscillation ω is linearly controlled by transconductance G_m. Appealing from a circuits perspective is the use of translinear networks in implementing this architecture. Taking advantage of the linear dependence between transconductance and biasing current in such networks over a wide range, the oscillation frequency is tunable over multiple decades through a single parameter, as shown in the following section. Equation 2 points to the need of having the load R follow any changes in the transconductance G_m. Therefore, R has also to be tunable and scale inversely proportionally to G_m.

Deriving the poles of the closed loop system, we observe that one pole lies on the real axis at the left hand side (LHS) of the s-plane, while the other two poles have a negative, zero, or positive real part, depending on the value of $G_m \cdot R$

$$p_1 = -\frac{1 + G_m R}{RC}$$

$$p_2 = -\frac{(2 - G_m R)}{2RC} + \frac{\sqrt{3}G_m R}{2RC}j$$

$$p_3 = -\frac{(2 - G_m R)}{2RC} - \frac{\sqrt{3}G_m R}{2RC}j.$$

For $G_m \cdot R > 2$ the system becomes unstable and diverges, whereas for $G_m \cdot R < 2$ the system converges to a stable point. Oscillations are observed only for $G_m \cdot R = 2$, which needs to be ensured through an amplitude stabilization mechanism as detailed below.

4 Circuit implementation

The transconductance-resistance gain stage is designed and implemented according to the two main attributes desired from the oscillator: wide tunability range and high (hundreds of MHz to low GHz) maximum attainable frequencies. To satisfy the first specification, translinear networks are implemented using bipolar junction transistors available in a BiCMOS process. The latter specification is addressed by avoiding the use of any PNP bipolar junction transistors, that are generally characterized by slow speeds and high parasitic capacitances, and instead by focusing on an NPN-only bipolar design.

In order to keep the circuit complexity low and the design simple, no closed-loop amplitude control is added. Instead, the design is based on a nonlinear implementation of the $G_m - R$ stage, that provides an amplitude limiting mechanism for the oscillations. More specifically, the input dependent gain of the $G_m - R$ stage is higher than 2 at power-up (assuming zero initial conditions), so as to position poles p_2 and p_3 to the right hand side (RHS) of the s-plane and cause the magnitude of the output signals to increase. The gain drops as the input increases and oscillations settle to an amplitude for which the time-averaging equation $\frac{1}{T}\int_0^T G_m \cdot R\, dt = 2$ is approximately satisfied.

A simple implementation for the above scenario is shown in Fig. 4. Diodes $D_1 - D_6$ are base-collector

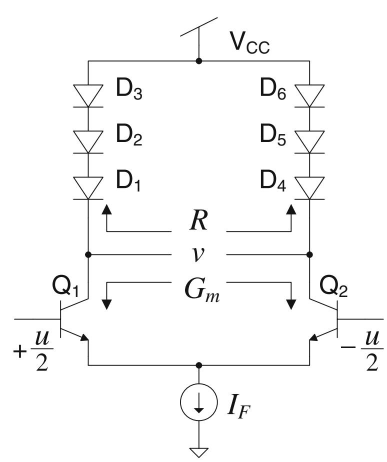

Fig. 4 Possible circuit implementation of the $G_m - R$ module. The architecture is fully translinear and avoids PNP devices, however requires a large voltage headroom

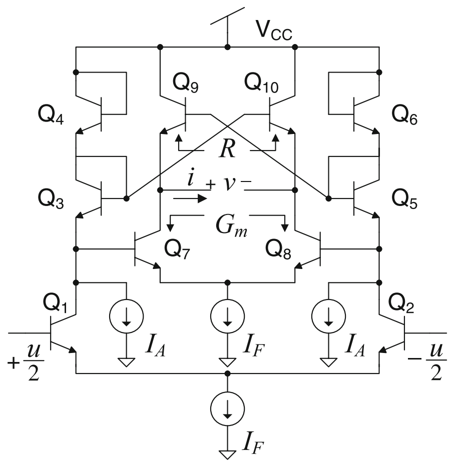

Fig. 5 Proposed translinear implementation of the $G_m - R$ module of Fig. 3

coupled transistors and form the load R, while transconductance G_m is obtained through transistors Q_1 and Q_2 that have the same size as their diode connected counterparts $D_1 - D_6$. The network has a gain of 3, which complies with the requirement of $G_m \cdot R > 2$ for small inputs. The gain remains fairly constant as the amplitude of oscillation grows, until any of the transistors start to enter the cut-off region. At that point the gain decreases and stabilizes the amplitude of oscillation. Transconductance G_m is linearly controlled through I_F and, due to (3), so is the frequency of oscillation.

A drawback of the previous design is the need for excessive voltage headroom, usually not available in typical BiCMOS processes. In order to comply with the 3.3 V requirement for the power supply in most BiCMOS technologies, the design of Fig. 5 is proposed for the implementation of the $G_m - R$ blocks in the oscillator architecture. Transconductance G_m here is considered as formed by transistors $Q_1 - Q_8$ and the load R from transistors Q_9 and Q_{10}. A small-signal analysis of the topology reveals again a gain of 3 for small inputs (and $I_A = 0$). A detailed analysis of how amplitude and frequency evolve is presented in the following section. Current sources I_A have been included in the design in order to provide the option of feed-forward amplitude adjustment.

It should be noted that the obtainable oscillation amplitudes for the proposed circuit are limited to a few V_T's (V_T is the thermal voltage, equal to 26 mV at room temperature) due to the small "linear" region of the corresponding gain. The maximum amplitude can be increased and the linearity improved, if the input transistors Q_1 and Q_2 are replaced by a "doublet" (multi-tanh) network [32].

5 Circuit analysis

5.1 Circuit operation

Denoting as u the differential input voltage of the network of Fig. 5 and as v its differential output, analysis of the circuit reveals the following input–output relation of the unloaded translinear amplifier

$$v = 3V_T \ln\left(\frac{e^{\frac{u}{V_T}} + \beta\left(1 + e^{\frac{u}{V_T}}\right)}{1 + \beta(1 + e^{\frac{u}{V_T}})}\right) \tag{4}$$

where $\beta = I_A/I_F$. Setting $I_A = 0$ A, Eq. 4 collapses to $v = 3u$, providing, as in the case of Fig. 4, a widely linear gain relation of $G_m \cdot R = 3$, valid until any of the transistors enters the cut-off region. For $\beta > 0$, the unloaded input–output voltage relation is no longer linear, and the amplitude is limited by the inherent nonlinearities of the circuit. Current I_A provides the flexibility of controlling the shape of the input–output curve (Eq. 4) and therefore serves as a tuning parameter for the amplitude. Plots of the unloaded input–output voltage relation (u vs. v) as well as of its first derivative, are drawn in Fig. 6.

The translinear network exhibits maximum gain for 0 input and the gain is derived by evaluating the derivative of v with respect to u (Eq. 4) for $u = 0$. The maximum gain can be also viewed as the small signal gain of the translinear circuit around the origin $(u,v) = (0,0)$ and compared to condition (2) that has been derived for the linear network of Fig. 3. For oscillations to start, the maximum value of the gain needs to be higher than 2, which gives an upper limit for β

$$0 \le \beta < 0.25 \Leftrightarrow 0 \le I_A < 0.25 I_F. \tag{5}$$

5.2 Frequency

In order to derive the actual frequency of oscillation, the translinear amplifier of Fig. 5 is embedded in the oscillator loop of Fig. 2 and its output current as a function of the input and output voltages u and v, respectively, is evaluated. The resulting expression is presented below

$$i = f(u,v) = \frac{I_F\left(k^3(u) - e^{\frac{v}{V_T}}\ell^3(u)\right)}{(k^2(u) + \ell^2(u))\left(k(u) + e^{\frac{v}{V_T}}\ell(u)\right)} \tag{6}$$

where

$$k(u) = e^{\frac{u}{V_T}} + \beta\left(1 + e^{\frac{u}{V_T}}\right) \text{and } \ \ell(u) = 1 + \beta\left(1 + e^{\frac{u}{V_T}}\right).$$

As a first-order approximation, (6) is expanded to a Taylor series, evaluated around $u = 0$, with terms up to 3rd order.

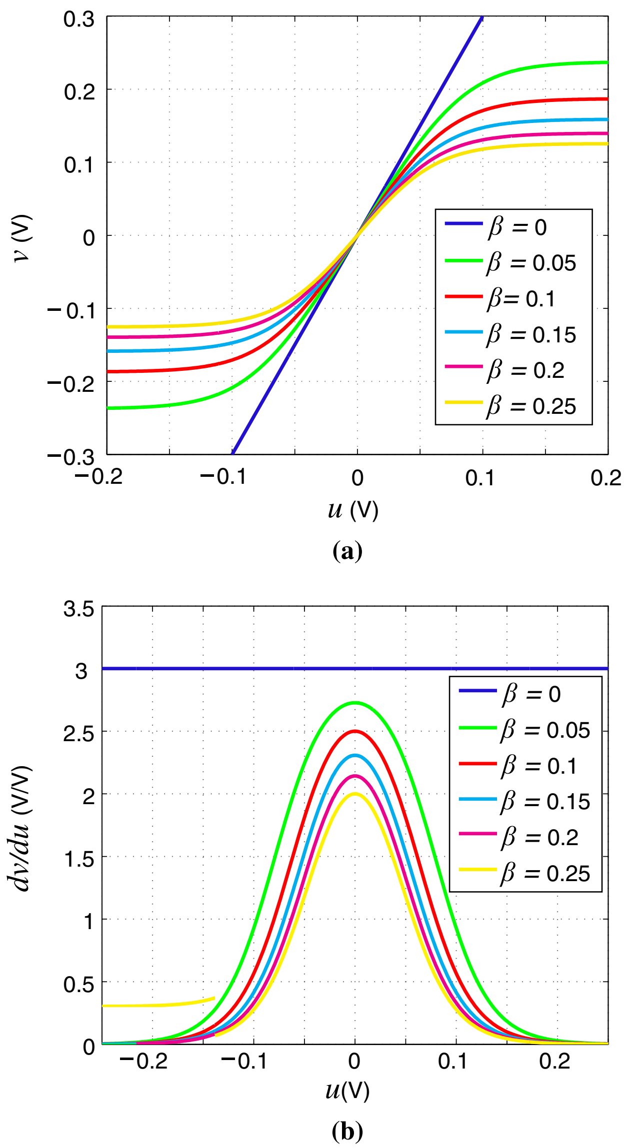

Fig. 6 (**a**) Input–output curves for the translinear circuit of Fig. 5 plotted for several values of β. (**b**) Gain of the translinear circuit as a function of the input voltage u for several values of β

Noting the symmetry of the circuit and its differential nature, even order terms cancel out and (6) is approximated by

$$f(u,v) \simeq a_1u + a_2v + b_1u^3 + b_2u^2v + b_3uv^2 + b_4v^3 \tag{7}$$

where the factors a and b are the scaled first and third order, respectively, partial derivatives of $f(u,v)$ with respect to u and v.

For each translinear amplifier block, the output current corresponds to the current flowing through capacitor C

$$C\dot{v} = f(u,v). \tag{8}$$

Assuming that only sinusoidal signals at the fundamental frequency are sustained in the oscillator loop and taking into account that during oscillations each $G_m - R - C$ block introduces a 60° phase shift in the loop, the input and output voltages u and v follow

$$\begin{aligned} u &= A \cdot \sin(\omega t) \\ v &= A \cdot \sin(\omega t - \tfrac{\pi}{3}) \end{aligned} \tag{9}$$

where A is the amplitude of oscillation.

Substituting (9) in (7) and (8), and retaining terms at only the fundamental frequency, the following expression is derived for the frequency of oscillation

$$\omega = \frac{\sqrt{3}}{2} \cdot \frac{I_F}{V_T C} \cdot \frac{3 + 4\beta + 2\beta^2}{7 + 6\beta - 16\beta^3}. \tag{10}$$

From (10) note that the frequency of oscillation is indeed linearly controlled by I_F for constant β as was expected due to the translinear design. It is also worth mentioning that the frequency of oscillation is loosely coupled to β, and that an increase in β corresponds to an upwards shift in frequency, and vice versa.

5.3 Amplitude

The above process results also in the subsequent estimate for the amplitude of the oscillations

$$A = 4\sqrt{\frac{4\beta - 1}{7 + 6\beta - 16\beta^3}} \cdot (1 + 2\beta) \cdot V_T \tag{11}$$

which, however, does not result in accurate results. Higher accuracy in the approximation can be obtained by including higher order terms in the Taylor approximation, however, doing so, requires solving an intractable system of equations.

To circumvent this issue, a different approach has been pursued to decouple the amplitude estimation from the frequency estimation. Starting from (4), the voltage gain of the translinear amplifier of Fig. 5 is derived by taking the derivative of the output voltage v with respect to the input u

$$\frac{dv}{du} = 3\frac{1 + 2\beta}{\left(1 + \beta\left(1 + e^{-\frac{u}{V_T}}\right)\right)\left(1 + \beta\left(1 + e^{\frac{u}{V_T}}\right)\right)}. \tag{12}$$

According to the linear version of the topology and (2), this gain needs to equal 2 for oscillations to be sustained. Since the gain is input dependent in the nonlinear version, the linear criterion (2) is extended and assumed to hold also for the time averaged value of the gain of the nonlinear translinear amplifier. Linearizing (12) in the form of a Taylor series with terms up to 5th order and assuming oscillations at frequency ω and of amplitude A, the following requirement

$$\frac{1}{2\pi}\int_0^{2\pi} \left.\frac{dv}{du}\right|_{u=A\sin(\theta)} d\theta = 2$$

leads to the expression of Eq. 13 for the amplitude of oscillation.

$$A = 8(1+2\beta)\frac{\sqrt{3\beta(-1+7\beta+16\beta^2+8\beta^3)\left(6\beta^2+6\beta-\sqrt{372\beta^4+144\beta^3-30\beta^2+6\beta+192\beta^5}\right)}}{-12\beta+84\beta^2+192\beta^3+96\beta^4} \quad (13)$$

6 Experimental results

The circuit has been fabricated in an IBM SiGe BiCMOS process provided through MOSIS with minimum feature size of 0.5 μm and an f_T for the NPN devices of 50 GHz. The capacitor values are 0.5 pF and the supply voltage is set at 3.3 V. Power consumption scales linearly with oscillation frequency and exhibits approximately 2 μW/MHz measured dependence. A microphotograph of the oscillator is shown in Fig. 7. Note that due to the high thickness of the top metal layer, the underlying circuitry cannot be easily distinguished.

The dependence of the oscillation frequency to biasing current I_F was first investigated, by sweeping I_F from a few tenths of a nA to almost a mA, while keeping I_A (and therefore β) equal to 0, and measuring the output frequency. The results are shown in Fig. 8, demonstrating a linear frequency tuning range of 5 decades. The total range of achievable frequencies extends over 7 decades, from below 80 Hz to above 800 MHz.

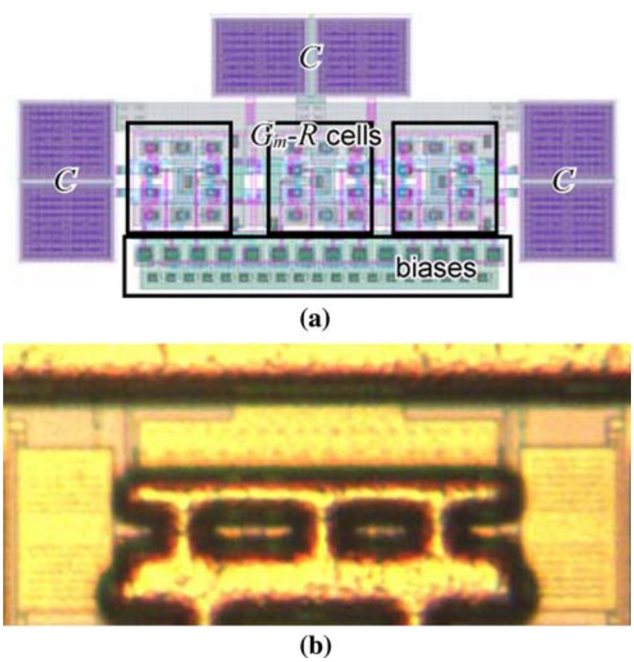

Fig. 7 (**a**) Layout and (**b**) microphotograph of the oscillator. Dimensions are approximately 150 μm × 300 μm in 0.5 μm BiCMOS SiGe technology

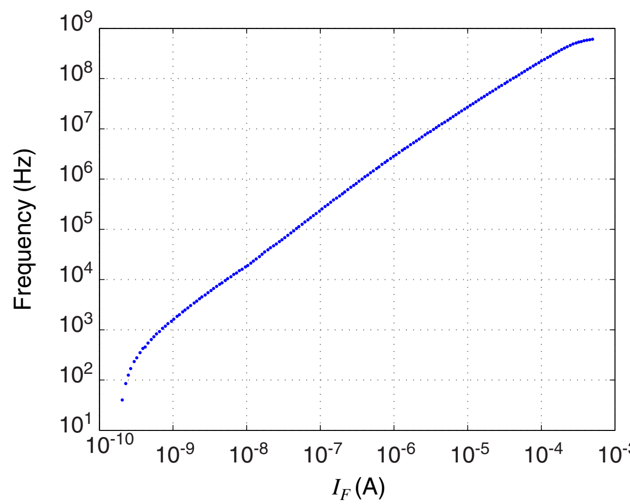

Fig. 8 Dependence of the oscillation frequency to current I_F. The range of measured frequencies spans 7 decades

A comparison between the theoretically expected amplitude (13) of oscillation as a function of β and its measured value is shown in Fig. 9. For the measurements, I_F was kept constant and β was varied through I_A. According to (5), the maximum value of β for which oscillations would theoretically be observed is 0.25, however this value would vary in measurements for different tested oscillators. This discrepancy can be justified due to mismatches in the current mirrors. For a fair comparison between theory and measurements, the current mirror gains were measured and used to scale the experimental data.

It is also worth noting that for very low and very high currents I_F the amplitude of oscillation drops significantly. This is due to the reduced value of the forward current gain (β_F) of the transistors at very low and very high biasing currents, causing the translinear principle to fail and the oscillator to no longer operate as expected.

Finally, the spectrum of the output, probed at one of the phases of the oscillator, is plotted in Fig. 10, for an oscillation frequency set to 100 MHz and for $\beta = 0$. Note that the second harmonic has been almost completely suppressed due to the differential nature of the output, whereas the third harmonic is almost 40 dB below the level of the fundamental.

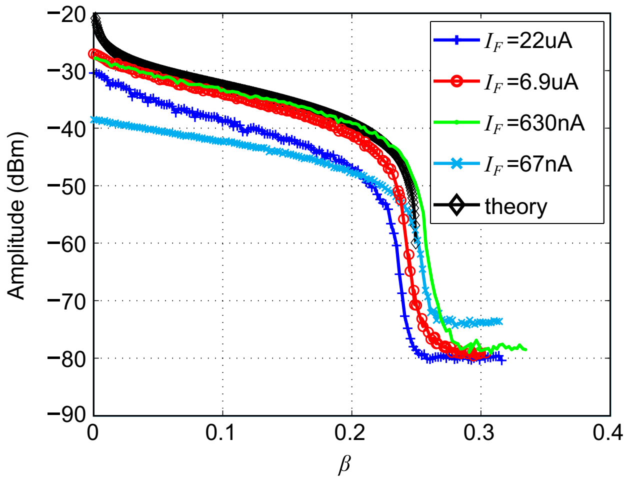

Fig. 9 Dependence of the amplitude of oscillation to β for several fixed values of I_F

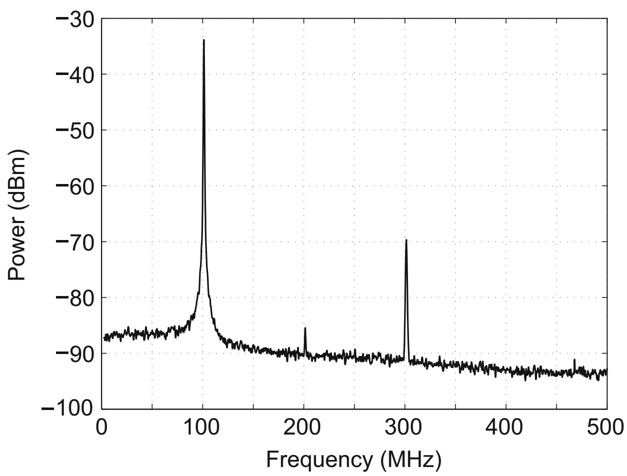

Fig. 10 Spectrum of the output signal from one of the phases of the oscillator for a generated frequency of 100 MHz

7 Conclusion

The architecture and SiGe BiCMOS implementation of a 3-phase, 7-decade frequency tunable sinusoidal oscillator have been presented. The oscillator has been designed as a closed-loop of 3 cascaded translinear $G_m - C$ filters and features both frequency and amplitude control. An analysis of the conditions that have to be met for oscillation and the system behavior during oscillation has been performed, and closed-form expressions have been derived for the amplitude and frequency of oscillation. Experimental results demonstrate frequency tunability from 80 Hz to 800 MHz, low distortion, and 2 μW/MHz linear scaling of power with oscillation frequency. Examples have been given where the oscillator circuit is embedded with other integrated circuits for applications in communications, self-test, adaptive control, and bioinstrumentation.

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