Micropower Integrated Bioamplifier and Auto-ranging ADC for Wireless and Implantable Medical Instrumentation

Yu M. Chi* and Gert Cauwenberghs‡
*Department of Electrical and Computer Engineering
‡Department of Bioengineering
University of California, San Diego La Jolla, CA 92093

***Abstract*—A micropower, high-resolution biopotential data acquisition circuit for wireless and implantable medical instrumentation is presented. The circuit is an incremental $\Delta\Sigma$ (BioADC) that accepts inputs directly from recording electrodes and serves as both amplifier and digitizer with just a single OTA at the core. Auto-ranging and precise digital gain control allow the BioADC to accommodate input ranges of $1mV$ to $30mV$ with DC offset rejection. The hybrid amplifier/ADC achieves up to 12 bits of resolution, a sampling rate of 2.048kHz and an input referred noise of $2.65\mu Vrms$ at a power consumption of $20\mu W$. The bioamplifier achieves a noise efficiency factor of 3.1. Live physiological ECG data are shown, acquired by connecting passive Ag/AgCl electrodes directly to the BioADC input.**

I. Introduction

Wireless and implantable biomedical devices are becoming increasingly important for healthcare and research. Wearable, unobtrusive ECG/EEG systems allow patients to screen their vital signs for abnormalities during their daily lives. High density multi-channel implantable neural electrodes benefit researchers in understanding the nervous system and will be integral to future neuroprosthetics to help the disabled. Advancements in ultra-low power, integrated circuits has is a key driving force in this field.

The analog front-end consisting of the amplifier and ADC is a one major component in a biopotential acquisition system. For miniature wireless battery powered devices, minimizing the power and complexity of the analog front-end is still a challenge.

To date, several authors have built innovative integrated solutions for multi-channel biopotential recordings using the approach of a low noise preamplifier [1] followed by an ultra-low power SAR [2] or $\Delta\Sigma$ ADC [3]. It is possible to achieve excellent noise efficiency specifications [4] [5] [6] as well as very high channel densities [7].

In addition, single chip, commercial multi-channel ECG/EEG products have also appeared on the market with very high resolution, but a relatively large power consumption of around $1mA$/channel. [8]

However, nearly all currently known bioamplifier circuits are designed to drive a separate ADC block, with the exception of [9] which produces pulse delay modulated output. Thus, there are two primary sources of power and complexity in the typical analog front-end. The amplifier section consumes up to several microamperes of current, and is dictated by the noise requirement. The ADC section itself will require separate circuits and will also consume up to tens of microamperes per ADC channel [3]. For future integrated systems, an even more efficient solution is desirable.

In this work, we introduce a new bioamplifier circuit that configures the OTA normally used as just as the amplifier into also functioning simultaneously as an incremental $\Delta\Sigma$ ADC. By integrating the amplifier within the ADC, there is no need to drive any portion of the analog front-end beyond Nyqusit rate and and an explicit anti-alias filter is not needed. The BioADC interfaces directly with unbuffered, μV levels signals from the body and provides a digitized output.

The BioADC reduces the complexity and power of the analog-front end for biopotential systems by integrating the amplification and digitization of signals into one circuit. The main source of static power dissipation is from biasing the core OTA, which sets the noise levels, the same as conventional systems. Power and area for a separate, dedicated ADC circuits are eliminated. We are able to achieve a total power consumption of less than $20\mu W$ per channel without compromising on noise and resolution.

II. Circuit Overview

The core of the BioADC consists (Fig. 1) of an OTA, a comparator, data latches and input coupling and feedback capacitors. Signals from a differential pair of recording electrodes are directly coupled through the on-chip capacitor, C_{in}, to the OTA's input. The comparator and feedback capacitors complete the incremental $\Delta\Sigma$ feedback loop. The digital output from the BioADC is taken from the comparator's latch.

A. Input Coupling and Auto-ranging

A reset switch is enabled only at power-up to initialize the voltage at the OTA's input to a known value, V_{ref}. During normal operation, the input nodes of the OTA are left at a very high impedance. If left unattended, leakage currents at the OTA's input will cause both an uncontrolled common and differential-mode drift, eventually causing the BioADC to fail.

To control the OTA input node voltages, two sets of increment/decrement update circuits [10] are utilized as a

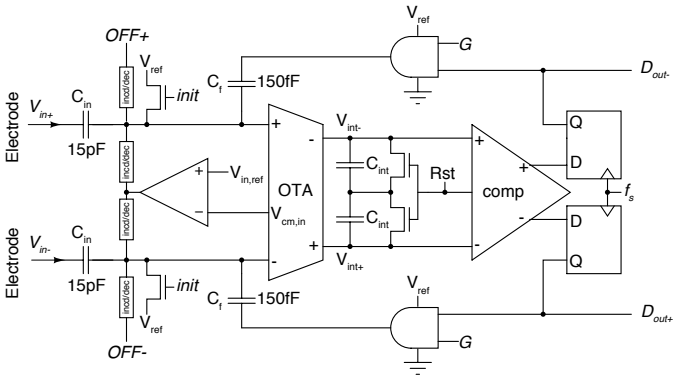

Fig. 1. Complete schematic of the BioADC for a single channel. Inputs are AC coupled to the input's of the OTA which have dynamic auto-ranging and offset correction through an increment/decrement circuit [10]. The OTA serves as the integrator of the incremental $\Delta\Sigma$ ADC. The amount of feedback from the comparator's decision applied back to the OTA input's is digitally controlled to precisely set the gain.

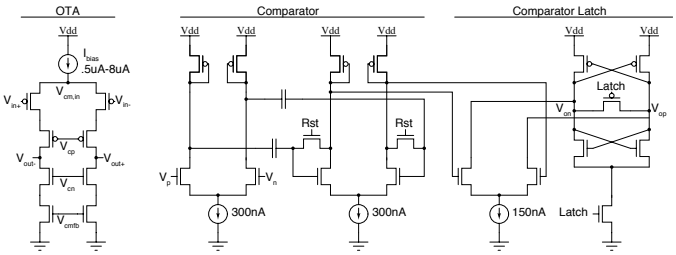

Fig. 2. Transistor level schematics of the OTA and latched comparator. The main source of static power consumption is the DC biasing current of the OTA which sets the fundamental noise limits.

way to dynamically inject small amounts of current. The increment/update circuits are built from a NMOS and PMOS transistor placed in parallel with their gates respectively tied close to ground and the supply to inject small amounts of current into the high impedance OTA input node.

For common mode control, the voltage at the source of the OTA input pair, $V_{cm,in}$ (Fig. 1 and Fig. 2), is monitored and compared to the desired level, $V_{in,ref}$. The comparator for the common-mode control circuit is a simple 1-stage OTA biased with only $50nA$ of current and does not contribute a significant amount of power.

Differential offsets are dynamically cancelled by monitoring the output bitstream. The direction of the charge pump (OFF+, OFF-) is controlled such a negative feedback loop is formed at low frequencies, causing the BioADC to auto-range signals to center near midscale over long time periods. In the current implementation, this effectively implements a low-pass filter of around $1Hz$. In addition, different modulation patterns for the charge pump can be used to achieve various high-pass filtering characteristics.

B. OTA and Comparator Circuits

Figure 2 depicts the transistor level schematics for the core OTA and latched comparator for the BioADC.

The OTA is a standard, fully-differential cascoded amplifier. The input PMOS pair was sized with an extremely large W/L

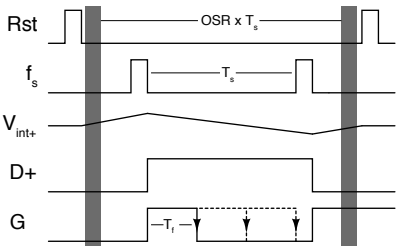

Fig. 3. Timing diagram showing the integrator reset, the integration and decision of one sample and the digital gain control. The duty cycle of G controls the amount of feedback applied in the $\Delta\Sigma$ loop. The signals for one half of the fully differential circuit is shown.

(480/1.5) ratio and operated in subthreshold. All the other devices are sized to be long, and operated in strong inversion such that the noise should be dominated by the input pair alone [1]. CMFB is accomplished by taking common-mode of the output signal available at the node in-between the two integration capacitors, C_{int} with the DC level restored during the normal reset phase of the BioADC.

The bias current of the OTA sets the noise floor of the BioADC is nominally between $.5uA$ and $8uA$. This biasing current is normally the largest source of static power dissipation.

A latched comparator is used as the quantizer for the $\Delta\Sigma$ modulator and consists of two preamplifier stages followed by a positive feedback latch circuit [11]. The first and second pre-amplifier stages are capacitively coupled and reset at the same time as the OTA integrator. This stores the offset of both the comparator and OTA at the same time. A total of $750nA$ is used to bias the latch's preamplifiers.

C. Incremental $\Delta\Sigma$ ADC

A first order, continuous-time, incremental $\Delta\Sigma$ ADC is formed through the OTA, which serves as a resettable $G_m - C$ integrator, a comparator and a negative feedback loop through C_f.

A timing diagram for one sample is shown in Figure 3. A sample begins with a pulse (Rst) which resets C_{int} and simultaneously nulls the comparator and OTA offset. The signal is integrated for a period of T_s which ends with a pulse to latch the comparator's decision, f_s.

Depending on the integrated voltage, either D+ or D- is asserted high. Because both the inputs and comparator decision are capacitively coupled, the summing node which combines the signal and the $\Delta\Sigma$ negative feedback can be implemented right at the same OTA's input.

The voltage at the output of the OTA integrator over one period, T_s, can be written as,

$$V_{int} = \frac{g_m}{2C_{int}} \int_0^{T_s} V_{in}(t) \frac{C_{in}}{C_t} dt \pm \frac{g_m}{2C_{int}} \int_0^{T_f} V_{ref} \frac{C_f}{C_t} dt \quad (1)$$

where the polarity of the second term is controlled by the comparator's last decision, g_m is the OTA's transconductance and C_t is the sum of the capacitances at the OTA's input (including parasitics).

The full scale code for the incremental ADC is set by the amount of feedback applied in the loop and is controlled by the supply voltage and the duty cycle of G (T_f/T_s) resulting in full-scale input of,

$$V_{range} = 2\frac{C_f}{C_{in}}\frac{T_s}{T_f}V_{ref}. \quad (2)$$

A total of OSR periods is integrated and quantized before reseting the integrator. Summing the periods that D_{out+} is high represents a OSR-bit resolution code for the input signal over a single sample, completing the operation of the incremental ADC. The circuit cannot function reliably as a conventional $\Delta\Sigma$ ADC over long periods of time due to the need to for periodically refreshing the DC level of the comparator's pre-amplifier and the OTA CMFB circuit.

The overall transfer function from input voltage to bits can then be expressed as,

$$D_{out} = 2^{OSR}2V_{ref}\frac{C_f}{C_{in}}\frac{T_f}{T_s}\frac{(V_{in+} - V_{in-})}{V_{range}}. \quad (3)$$

The gain is ratiometric and set by the sizes of C_{in} ($15pF$) and C_f ($150fF$) and independent of PVT, bias current and parasitic input capacitances. The two variables that control the full-scale range of the BioADC, and hence gain, V_{ref} (nomially set at V_{dd}) and the duty cycle of G (T_f/T_s). Thus, the gain can be well defined and easily tuned through digital control. With the BioADC, it is possible to have full-scale input ranges of less than $1mV$ differential, allowing for small μV signals to be directly connected to the BioADC.

The BioADC combines the advantages of several previous implementations of bioamplifiers and ADCs, while integrating both functions with a single core analog OTA for optimal power efficiency. A typical low-noise bioamplifier [1] [3] will also consist of an OTA along with signal coupling capacitors C_{in} and C_f arranged in negative feedback to set the closed loop gain. The addition of the explicit OTA load capacitance, C_{int} and comparator in the feedback loop, essentially operates the circuit as a class-D bioamplifier. In combination with the $\Delta\Sigma$ feedback, the switched output of the BioADC is directly provides a digital output.

III. Characterization

The fabricated chip (Fig. 7) containing two separate channels was tested for distortion and noise performance using a simple custom PCB with a USB data acquisition circuit. The chip was also connected directly to electrodes placed on a subject to collect live physiological data.

A. Distortion and Resolution

Since the BioADC is fundamentally an AC coupled system, the INL and DNL of the ADC cannot be determined from measurements.

To characterize the ADC for AC signals, a single tone test is used to measure the level of distortion. The FFT of a $100Hz$, $1mV$ input signal is shown in Figure 4. For this test, the BioADC was set to operate at an oversampling ration of 2^{10} which corresponded to a post decimation sample rate of 512Hz. The gain setting was set such that the full-scale code was just slightly higher than the 1mV input tone.

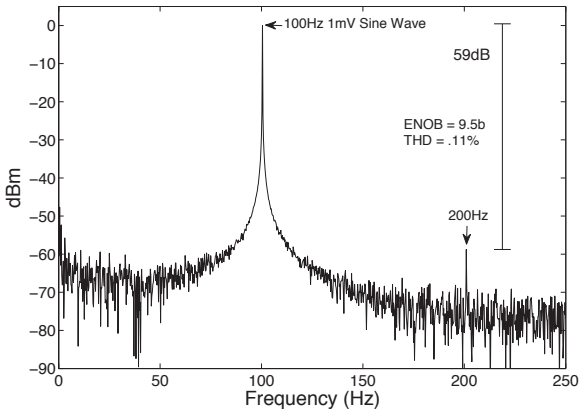

Fig. 4. Single tone test at 100Hz. The BioADC achieves an ENOB of 9.5b when operating an oversampling ratio of 2^{10} and an output data rate of 512Hz.

Overall distortion levels are low, and the BioADC achieves an ENOB of $9.5b$ for a $1mV$ full scale input matching well with the OSR of 2^{10} in line with the SNR requirements for an OSR of 2^{10}

B. Noise Performance

The ADC's noise floor was measured by shorting both differential inputs to ground and recording the output data stream. Figure 5 shows the input-referred voltage noise density for OTA bias currents of $1\mu A$ and $8\mu A$.

The noise at low frequencies is mainly dominated by $1/f$ noise of the input transistors as well as noise from leakage currents from the charge pump. At higher frequencies, the levels approach the thermal noise limits of the input differential pair.

A noise efficiency factor of the ADC is 3.1 at a bias current of $1\mu A$ and a total input referred voltage noise of $2.6\mu Vrms$ is measured. At a bias current of $1\mu A$, the BioADC approaches the fundamental thermal noise floor of the subthreshold input pair showing that the addition of the ADC circuits does not significantly degrade the noise performance. The overall performance of the BioADC is comparable to the best integrated bioamplifiers reported to date.

C. Physiological Recordings

Live ECG data was acquired by connecting the differential inputs of the ADC directly to a subject's chest via purely passive Ag/AgCl electrodes. The recorded data can be seen in Fig. 6 along with a recording of an artificial ECG from a signal generator.

IV. Conclusion

We present a low power amplifier/ADC specifically suited for wireless and implantable biomedical devices. The biopotential acquisition circuit accepts unbuffered signals at it's and performs both amplification and digitization using just one core OTA. Overall performance in terms of power, noise and

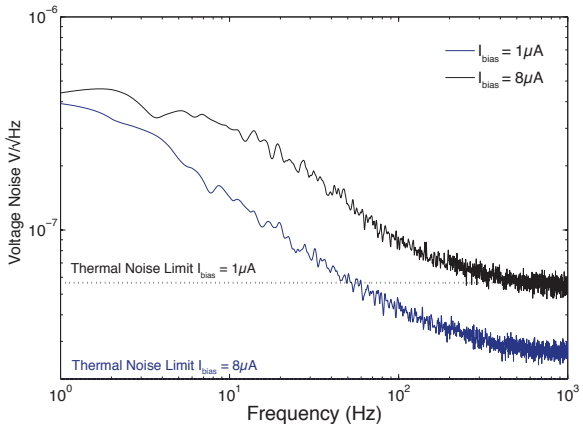

Fig. 5. Input referred voltage noise of the BioADC at an OTA bias current of $1\mu A$ and 8μ. The BioADC achieves an NEF of 3.1 and an input referred noise of $2.6\mu VRMS$ at $I_{bias} = 1\mu A$. The theoretical thermal noise limit, $2qI_{bias}/g_m^2$, of a subthreshold MOS transistor is also shown.

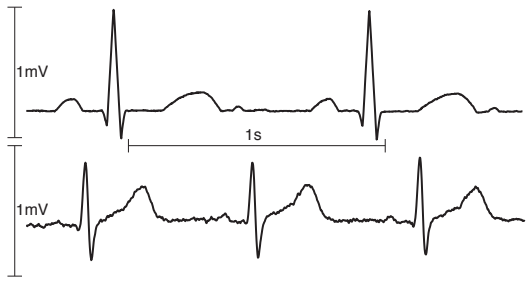

Fig. 6. Artificial (top) and live ECG (bottom) signals acquired by the BioADC. Passive AgCl clinical adhesive electrodes on the subject's were connected directly to the BioADC's inputs. The subject was also passively connected to circuit ground through a third AgCl electrode.

resolution is comparable to standard bioamplifier circuits with an analog output. The BioADC provides a simple, efficient circuit to build highly integrated, multi-channel biopotential acquisition systems.

V. Acknowledgements

Chip fabrication was provided through the MOSIS MEP.

TABLE I
CHIP SUMMARY

Process	0.5μm CMOS
Full-scale Input Range	$\pm 1mV$ to $\pm 30mV$
Sampling Rate	128Hz to 2.048kHz
Frequency Response	1Hz to $f_{sample}/2$
Resolution	8b to 12b
Distortion	9.5 ENOB and .11% THD
Input Referred Noise	$2.65\mu V$ RMS
NEF	3.1
OTA Bias	$.5\mu A$ to $8\mu A$
BioADC 1-channel Power Consumption	$20uW$/channel at 3.3V

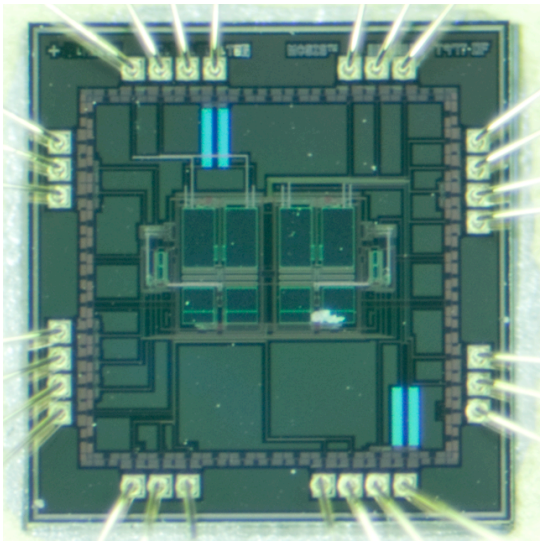

Fig. 7. Micrograph of the fabricated $1.5mm \times 1.5mm$ chip containing two channels.

References

[1] R.R. Harrison and C. Charles. A low-power low-noise cmos amplifier for neural recording applications. *Solid-State Circuits, IEEE Journal of*, 38(6):958 – 965, june 2003.

[2] Long Yan, Namjun Cho, J. Yoo, Binhee Kim, and Hoi-Jun Yoo. A two-electrode $2.88nJ/conversion$ biopotential acquisition system for portable healthcare device. In *Solid-State Circuits Conference, 2008. A-SSCC '08. IEEE Asian*, pages 329 –332, nov. 2008.

[3] M. Mollazadeh, K. Murari, G. Cauwenberghs, and N. Thakor. Micropower cmos integrated low-noise amplification, filtering, and digitization of multimodal neuropotentials. *Biomedical Circuits and Systems, IEEE Transactions on*, 3(1):1 –10, feb. 2009.

[4] J. Holleman and B. Otis. A sub-microwatt low-noise amplifier for neural recording. In *Engineering in Medicine and Biology Society, 2007. EMBS 2007. 29th Annual International Conference of the IEEE*, pages 3930 –3933, aug. 2007.

[5] R.F. Yazicioglu, P. Merken, R. Puers, and C. Van Hoof. A $60\mu W 60nV/Hz$ readout front-end for portable biopotential acquisition systems. In *Solid-State Circuits Conference, 2006. ISSCC 2006. Digest of Technical Papers. IEEE International*, pages 109 –118, feb. 2006.

[6] W. Wattanapanitch, M. Fee, and R. Sarpeshkar. An energy-efficient micropower neural recording amplifier. *Biomedical Circuits and Systems, IEEE Transactions on*, 1(2):136 –147, june 2007.

[7] R. R. Harrison, P. T. Watkins, R. J. Kier, R. O. Lovejoy, D. J. Black, B. Greger, and F. Solzbacher. A low-power integrated circuit for a wireless 100-electrode neural recording system. *Solid-State Circuits, IEEE Journal of*, 42(1):123 –133, jan. 2007.

[8] Texas Instruments. *ADS1298 8-Channel, 24-bit Analog-to-Digital Converter with Integrated ECG Front End Datasheet*. 2010.

[9] Du Chen, J.G. Harris, and J.C. Principe. A bio-amplifier with pulse output. In *Engineering in Medicine and Biology Society, 2004. IEMBS '04. 26th Annual International Conference of the IEEE*, volume 2, pages 4071 –4074, sept. 2004.

[10] G. Cauwenberghs and A. Yariv. Fault-tolerant dynamic multilevel storage in analog vlsi. *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, 41(12):827 –829, dec 1994.

[11] R. Jacob Baker. *CMOS Circuit Design, Layout, and Simulation*. Wiley-IEEE Press, 1997.

[12] Ming Yin and M. Ghovanloo. A low-noise preamplifier with adjustable gain and bandwidth for biopotential recording applications. In *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on*, pages 321 –324, may 2007.