THREE-DECADE PROGRAMMABLE FULLY DIFFERENTIAL LINEAR OTA

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ABSTRACT

Acoustic and sonar analog signal processing applications require design of operational transconductance amplifiers (OTAs) that can be configured over wide frequency range in multiple bands and yet achieve low power consumption and low harmonic distortion. A fully differential, linear OTA is presented with digitally programmable transconductance ranging over three decades of dynamic range. Measurements from a prototype fabricated in a 0.5μm CMOS process demonstrate a 0.4 nA/V to 0.8 μA/V transconductance range, 40 dB common-mode rejection ratio (CMRR), and -48 dB third-order harmonic distortion, at 12 μW power dissipation.

1. INTRODUCTION

One of the advantages of field programmable analog arrays is its flexibility in reconfiguring circuit topologies and adapting them to specifications of different applications. In filter bank analog design, specifications may dictate adjustment of bandwidth parameters ranging over a wide range of frequencies covering audio to ultra-sonic range. The adjustment of filter parameters can be achieved either through digitally addressed capacitor arrays or through programmable OTAs whose transconductance can be digitally varied over a large range [1]. For very low frequency applications, digitally programmable capacitor sizing and resolution is limited by available silicon area, hence a more viable approach is to design wide range field programmable OTAs. Previous work in this field has focused on wide range analog tunability [2] using MOS transistors operating in subthreshold, or high-frequency applications [3] with tunability limited to 2 decades of transconductance. Limiting factors in increasing the range of tunability to several decades have been conflicting requirements of high linearity and dynamic range. This paper proposes an OTA architecture whose transconductance can be varied over 3 decades without appreciable degradation of its linearity or dynamic range. The design presented in this paper builds upon the tunable linear OTA architecture in [4, 1] and is augmented by using two-level digital current scaling techniques to obtain a wide-range linear transconductance.

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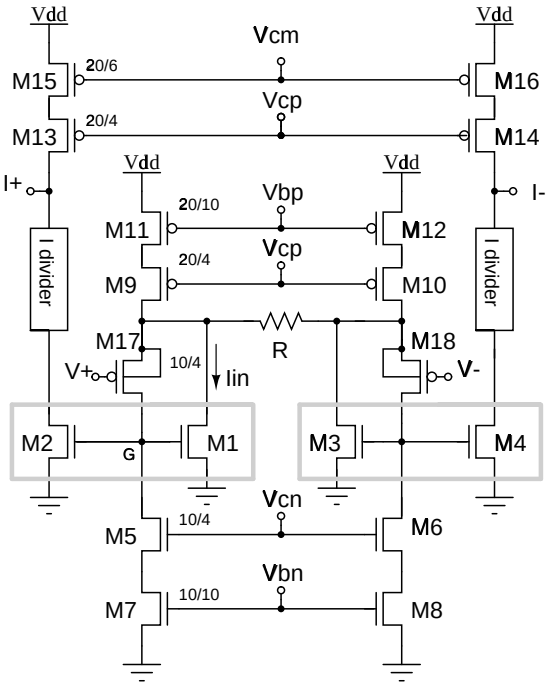

Fig. 1. Fully differential digitally programmable OTA. Transistor dimensions are given in units $\lambda = 0.3\mu m$.

The paper is organized as follows. Section 2 describes different elements used to design the digitally adjustable, fully differential OTA including current scaling techniques and common-mode feedback. Section 3 describes experimental results obtained from a prototype fabricated in 0.5μ CMOS technology, and section 4 provides concluding remarks.

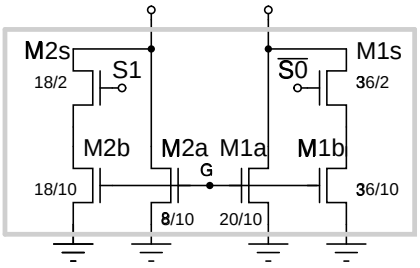

Fig. 2. Variable current ratioing for transistor pairs M1-M2 and M3-M4 in Figure 1.

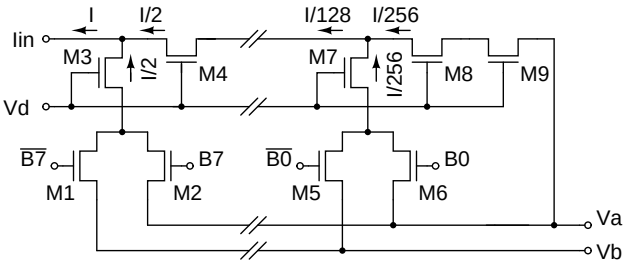

Fig. 3. 8-bit current divider [6]. All transistor are identically sized (8/8 λ units).

2. DIGITALLY PROGRAMMABLE OTA DESIGN

Figure 1 shows the architecture of the OTA. The design is fully symmetric for high noise immunity and high power supply rejection ratio. The key elements in the design are the input transistors $M17, M18$, the current sensing transistors $M1, M3$ and the mirror transistors $M2, M4$. The current mirror ratios $M1, M2$ and $M3, M4$ are digitally selectable through bits S_1 and S_0 ($\overline{S_0}$) as clarified in Figure 2.

Denote gm_p the transconductance and gd_p the output conductance of the input stage transistors $M17, M18$. Also let gm_n the transconductance of the current sensing transistors $M1, M3$. Then the relative current change δI_{in} with respect to a change in the differential input voltage δV_{in} is expressed as

$$\delta I_{in}/\delta V_{in} \approx 1/R \tag{1}$$

where R denotes the source degeneration linear resistance shown in Figure 1. Condition (1) is valid as long as

$$R \gg 2gd_p/gm_p gm_n \ . \tag{2}$$

Rather than adjusting the linear resistance R using active elements, it is more convenient to obtain a variable transconducance through scaling of the output current of the OTA first stage, in a second stage. Coarse level scaling is performed by the digitally programmable mirrors $M1, M2$ and $M3, M4$ and fine level scaling is performed at the output stage by the current divider in Figure 1, detailed in Figure 3.

2.1. Current Divider

The current divider scales the input current I_{in} by a binary coded digital factor with bits B_i, generating an output current:

$$I_{out} = I_{in} \sum_{i=1}^{n} B_i 2^{-i} \tag{3}$$

The current divider described in [6] and shown in Figure 3 offers the advantage of compactness in implementation, with four transistors for each bit of digital resolution.

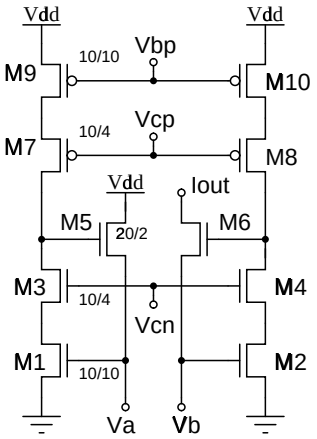

Fig. 4. Regulated cascode current conveyor for the current divider.

Critically important in achieving uniform scaling in the circuit of Figure 3 are low impedances nodes V_a and V_b, ideally at same potential. This is achieved by using the regulated cascode current conveyor [7] architecture shown in Figure 4. The node I_{out} is connected to the output current source of the OTA as shown in Figure 1 to establish high output impedance as essential to a transconductance amplifier. The output common mode at this high impedances node is determined by a common-mode feedback circuit described below.

2.2. Common Mode Feedback

The common-mode stabilization for the OTA is achieved using the simple circuit shown in Figure 5. The circuit regulates the bias level V_{cm} to maintain the maximum of V^+ and V^- to a predeterimined level, near the upper end of the range. Nonlinearity due to the maximum operation affect the outputs V^+ and V^-, but not their difference to first order. In contrast to more involved circuits to maintain true common mode, *e.g.,* [8], the common-mode circuit of Figure 5 uses fewer transistors and yet is effective. OTAs with common output nodes V^+ and V^- share a single common-

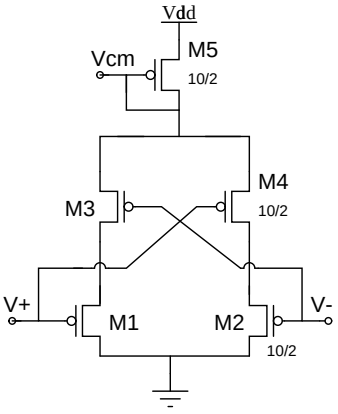

Fig. 5. Common-mode feedback circuit.

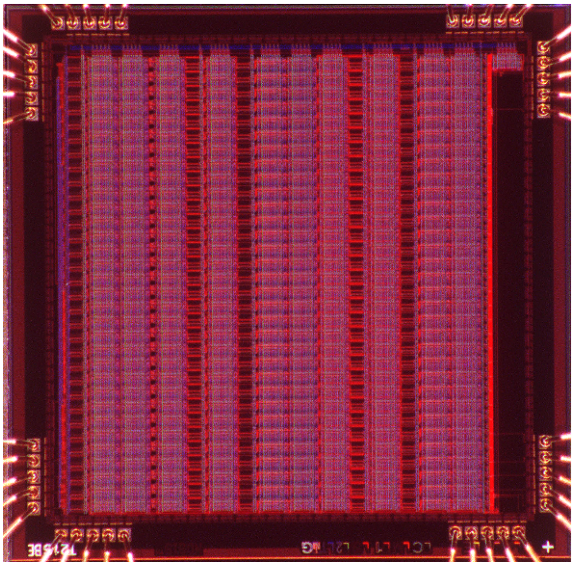

Fig. 6. Photomicrograph of programmable and reconfigurable OTA-C array.

mode stabilization circuit.

3. EXPERIMENTS

A prototype array of OTAs implementing a reconfigurable 32-channel filter-bank was fabricated in a 0.5μ CMOS process. The 3 $\times$ 3mm chip shown in Figure 6 consists of mainly 320 OTAs for different configurations of filter topologies.

Figure 7 presents linearity and dynamic range measurements from the OTA. The results indicate differential input dynamic range of 1.2V and common-mode input range of 1.5V. The CMRR (common-mode rejection ratio) measures 40 dB. Figure 8 demonstrates the wide digitally programmable range of the OTA. The four different curves

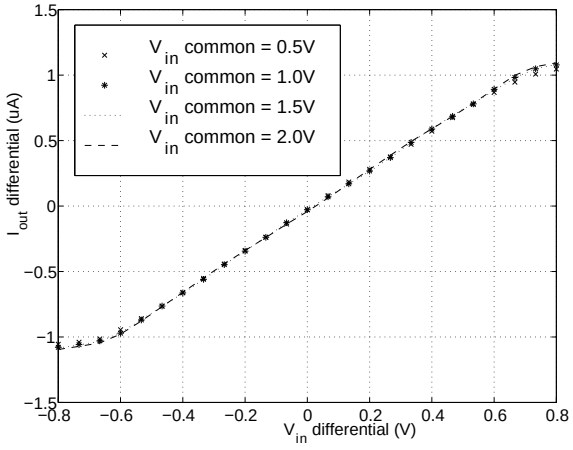

Fig. 7. Input differential and common-mode voltage range.

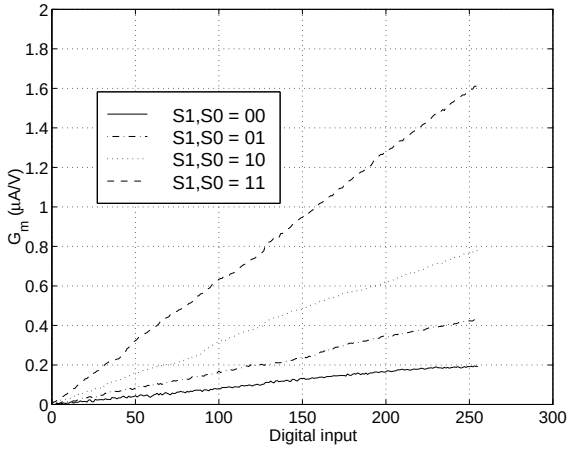

Fig. 8. Tuning curves: G_m as a function of digital control bits B7...B0 and S1,S0.

shown correspond to different $S1$ and $S0$ bit settings which achieve coarse-level scaling by approximate factors 1, 2, 4 and 8. Figure 8 also illustrates the effect of fine-level scaling indicated by the digital values in x coordinates to achieve a scaling by a factor of 255. In conjunction both stages of scaling result in an overall transconductance range of 0.39 nA/V to 0.8 μA/V, covering more than three decades. Table 1 summarizes the overall specification and measured performance figures of a single OTA.

OTAs and capacitors can be combined on-chip to generate various filter topologies. As an example, a first-order low-pass filter was realized. The low-pass filter comprises two OTAs and a capacitor as shown in Figure 9. The filter was programmed to unity gain at low frequency (by programming the two OTAs to have identical transconductance value) and with variable cut-off frequency. The measured frequency response for various programmed values of the

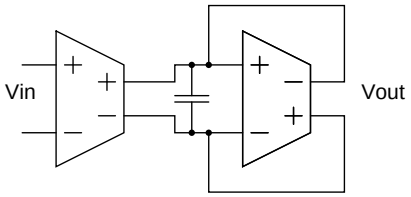

Fig. 9. Two OTAs and one capacitor configured as first-order low-pass filter.

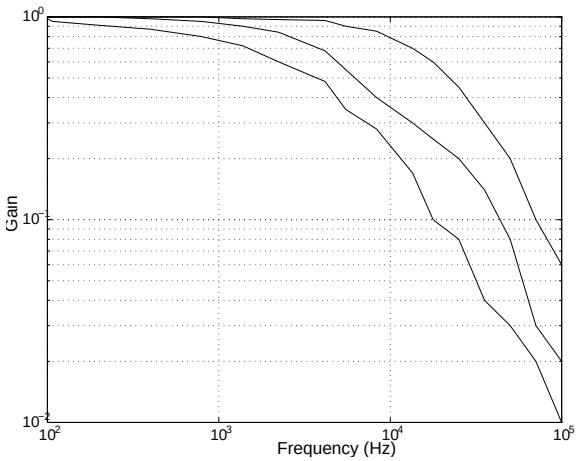

Fig. 10. Measured frequency response of first-order low-pass filter.

cut-off frequency is illustrated in Figure 10.

4. CONCLUSION

A fully differential operational transconductance amplifier with three decades of digitally programmable range has been presented. The OTA demonstrated low third order harmonic distortion, large CMRR and a large input dynamic range. The flexible design allows the OTA to operate with small bias currents which results in a minimum power consumption of 12μW. This design can be adapted for use in different applications with center frequencies ranging from subsonic to ultrasonic frequencies (10 Hz-120 kHz).

Table 1. OTA Characteristics

Parameter	Measured Value
Maximum Gm	0.8 μA/V
Minimum Gm	0.39 nA/V
Programming ratio	1/2048
Input offset voltage	20 mV
Input dynamic range	$\pm$1.2 V
Third-order harmonic distortion	-48 dB
Common-mode input voltage range	0.5-3 V
Common-mode output voltage range	1.0-4.0 V
Common-mode rejection ratio	40 dB
Silicon area	0.014 mm^2
Power supply	5 V
Power consumption	12 μW

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