A SPIKING SILICON CENTRAL PATTERN GENERATOR WITH FLOATING GATE SYNAPSES

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ABSTRACT

A programmable array of silicon neurons for the creation of Central Pattern Generator (CPG) networks is described. The design consists of 20 integrate-and-fire neurons, each with multiple synaptic inputs and tunable spike frequency adaptation circuitry. Synapse area is reduced by 80% relative to our previously fabricated chip by using floating gate transconductance amplifiers in place of current DACs. In addition to describing the design of the silicon neurons and synapses, we present results illustrating performance characteristics of the circuits and show how elaborate and biologically-plausible CPG networks can be implemented by controlling synaptic weights. The patterns generated by these circuits are shown to be sufficient to control a biped robot with a variety of different locomotory gaits.

1. INTRODUCTION

Locomotion, as well as many other periodic activities performed by animals, relies on the oscillating activity of a group of neural circuits in the spinal cord called the Central Pattern Generator (CPG) [1]. In the lamprey, for example, which is one of the best known CPG model systems [2], the CPG produces a pattern of motor activity that alternates between the right and left sides of the body as it travels along the length of the spinal cord, allowing the animal to propel itself through the water in various directions and at different speeds. In other vertebrates, agonist, antagonist, ipsilateral and contralateral limb muscles must be activated sequentially with appropriate timing relationships in order to achieve different locomotory gaits.

The timing relationships in a CPG-driven system correspond to phase shifts in the activity of different outputs. Specific phasic relationships are essential for all locomotion, natural or robotic. In much the same way that animals have CPGs constructed out of neurons, legged robots can have silicon equivalents of neurons to produce the necessary oscillatory outputs. Artificial systems that produce antiphase oscillatory, rhythmic waveforms, have been fabricated in the past [3–5]. In particular, an array of silicon neurons [5] (from which the circuits described here evolved) was able to generate outputs with the phase relationships required to produce walking gaits in a biped robot. However, although these outputs were biologically-motivated, they were not spike-based waveforms. Here, a similar array of neurons is presented, with modifications that allow production of spike-based CPG waveforms without the external circuitry of [6]. Additionally, the design has been

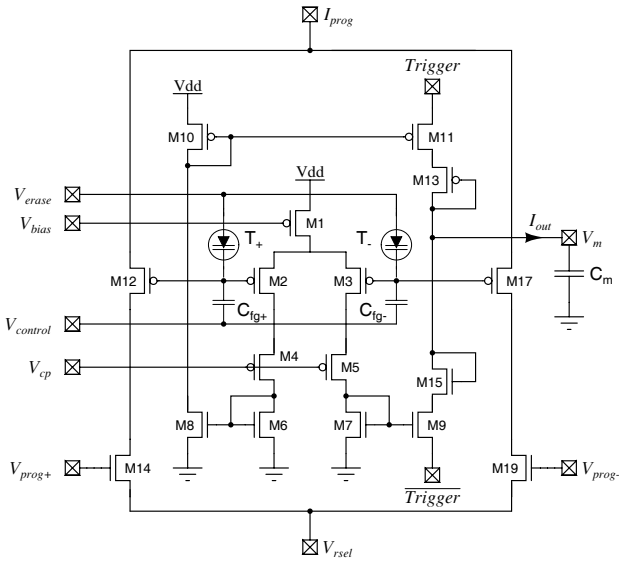

Fig. 1. Synapse schematic. The synapse is selected for programming through the V_{rsel} row select pin and the V_{prog+}, V_{prog-} column selectors that allow injection of negative charge on the floating gates.

modified to replace bulky current DACs with compact floating-gate transconductance amplifiers, resulting in an 80% reduction in silicon area. This savings allows for more neurons and synapses to be implemented on the same die, permitting implementation of more complex networks whose frequency and phase exhibit increased robustness to external perturbations such as those occurring during navigation through a hostile environment.

2. SYNAPSE AND NEURON ARCHITECTURE

Each neuron in the design is constructed from three compartments: a dendritic compartment containing the synapses, a somatic compartment that produces spikes, and an axonal compartment that communicates outgoing spikes to all other neurons on-chip and to external targets. The overall structure of the design is similar to the architecture presented in [7], except for the use of floating gate-based analog memory [8] in place of digital memory. This

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allows for continuous variation of synaptic strength and results in a significant reduction in silicon area and a higher density of neurons.

2.1. Synapses

All synapses in this design have the same architecture and are based on an operational transconductance amplifier, with floating gates controlling the voltage on the amplifier's differential inputs (Fig. 1). Therefore, each synapse has to be programmed before it can be activated.

To program a synapse, it must first be selected by setting the row select line (V_{rsel}) low and the column-wise V_{prog+} or V_{prog-} line high. A current is then programmed onto the floating gate, e.g. $\mathsf{C_{fg+}}$, by attaching a current source to I_{prog}, causing hot electron injection (HEI) [9] on transistor M12. This decreases the voltage on the gate of M2 and allows more current to flow along the transconductance amplifier's positive branch. The difference of the voltages on the two gates M2 and M3 determines the properties of the synapse: the polarity of the synaptic current (excitatory or inhibitory) is determined by the sign of the difference $\mathsf{M2} - \mathsf{M3}$ while the synaptic strength is set by the magnitude of the difference. Because HEI can only reduce the voltage on the floating gates, they may eventually need to be reset to a high potential. This is achieved by Fowler-Nordheim tunnelling [10] through $\mathsf{T_+}$ and $\mathsf{T_-}$, activated by the global V_{erase} pin. However, tunnelling requires high voltages, so it is avoided as often as possible: the differential pair design allows for multiple increases and decreases in synaptic strength exclusively through hot electron injection.

A synapse is activated by pulsing the $trigger$ and $\overline{trigger}$ lines, which gate the two currents generated by the differential pair (and mirrored by M6–M11) onto the cell's membrane capacitor $\mathsf{C_{mem}}$. The diode-connected transistors M13 and M15 in Figure 1 implement a voltage-dependant conductance that decreases the synaptic current as the potential stored on the membrane capacitor approaches the voltage on $trigger$ or $\overline{trigger}$ [7]. This allows a wider range of coupling strengths between neurons [5]. The output current, I_{out}, is therefore a function of four elements: (1) V_{bias}; (2) V_{fg+} and V_{fg-}, the voltage on the two floating gates; (3) $trigger$ and $\overline{trigger}$, which can be different from V_{dd} and gnd so that external analog inputs can affect the charging and discharging of the membrane potential; and (4) V_m, the voltage on the membrane capacitor. Defining I_{out+} and I_{out-} as the currents through M11 and M9, respectively, $I_{out} = I_{out+} - I_{out-}$ and the four elements described above affect the output current according to the following equations:

$$I_+^* = I_0 e^{\frac{V_{bias}^*}{\kappa U_T}} \tanh \frac{\kappa(V_{dd} - V_{fg}^+)}{2}$$

$$I_-^* = I_0 e^{\frac{V_{bias}^*}{\kappa U_T}} \tanh \frac{\kappa(V_{dd} - V_{fg}^-)}{2}$$

$$I_{out+} = I_+^* e^{-\frac{V_{dd} - trigger}{U_T}} (1 - e^{-\frac{trigger - V_m - 2V_{tp}}{U_T}})$$

$$I_{out-} = I_-^* e^{-\frac{\overline{trigger}}{U_T}} (1 - e^{-\frac{V_m - 2V_{tn} - \overline{trigger}}{U_T}})$$

where I_+^* and I_-^* are the currents through M6 and M7, respectively; $V_{bias}^* = V_{dd} - V_{bias}$; V_{fg+} and V_{fg-} are the floating gate voltages on the positive and negative terminals; and V_{tp} and V_{tn} are the threshold voltages of the PMOS and NMOS transistors.

There are three different types of synapses in the design, categorized according to what they are used for. One synapse per cell provides a constant (tunable) tonic drive for the neuron; a second group of synapses on every cell accepts external inputs on its $trigger$ and $\overline{trigger}$ lines; and a third group of synapses on every cell allows for all-to-all connectivity between neurons on the chip by routing each cell's output back to all the neurons in the array.

2.2. Neuron

Each neuron in the array contains 20 synapses, all of which contribute charge to the neuron's large membrane capacitor ($\mathsf{C_{mem}}$ in Fig. 1). When the voltage on the capacitor reaches a certain value (determined by a hysteretic comparator representing the biological axon hillock), the output of the comparator goes high. This causes the following four events:

- A *discharge* circuit drains charge from $\mathsf{C_{mem}}$ until the membrane potential falls below the hysteretic comparator's lower threshold, causing the output to go low again.
- A *refractory* circuit also discharges $\mathsf{C_{mem}}$ and sets the membrane potential to a fixed (tunable) voltage for a fixed (tunable) amount of time.
- A *pulse-width* circuit generates a fixed-duration (tunable) pulse whose rising edge coincides with the rising edge of the hysteretic comparator.
- A *spike-frequency adaptation* (SFA) circuit generates a prolonged discharge current proportional to the spike rate, essentially imposing a maximum spike frequency. This element has been shown to be critical in CPG networks [6].

Neurons with spike frequency adaptation capabilities have been realized in the past [11, 12], but whereas the work by Shin et al. [11] captures much of the biology of spike frequency adaptation, the approach taken here is more similar to Indiveri's [12]: simple, but effective. The input to the SFA circuit (Fig. 2a) is composed of two current generators, I_+ and I_-, both gated by the inverse of the neuron output ($\overline{OUT}$); the output from the circuit is attached to the neuron's V_m node. The current I_+ charges up the capacitor $\mathsf{C_{sfa}}$ when OUT is high and I_- discharges it when OUT is low. When the voltage on $\mathsf{C_{sfa}}$ approaches V_{tn}, transistor M3 draws significant current from V_m, making it increasingly difficult for the neuron's membrane potential to reach threshold. This makes the spikes more sparse until an equilibrium state is reached, in which the spike frequency is stable and $\mathrm{V_{sfa}}$ oscillates around a nonzero fixed point (Fig. 2c).

In normal operation, the voltage on $\mathsf{C_{sfa}}$ will not reach V_{tn}, so M3 will operate in subthreshold and the output frequency will depend exponentially on V_{sfa} (Fig. 2b). This relationship can be mathematically described via direct application of Kirchoff's Current Law (KCL) at the V_m node of neuron i:

$$C_{m_i} \frac{dV_{m_i}}{dt} = \sum_j W_{ij}^+ I_j - \sum_k W_{ik}^- I_k - S_i I_d - S_i I_{rf} - I_0 e^{\frac{V_{sfa}}{V_t}}$$

$$S_i(t+dt) = \begin{cases} 1 & \text{if } (S_i(t) = 1 \wedge V_i^m > V_T^-) \vee (V_i^m > V_T^+) \\ 0 & \text{if } (S_i(t) = 0 \wedge V_i^m > V_T^+) \vee (V_i^m > V_T^-) \end{cases}$$

where $\mathsf{C_{m_i}}$ is the membrane capacitance of the i-th neuron; V_T^+ and V_T^- are the high and low thresholds of the hysteretic comparator, respectively; V_{m_i} is the voltage across the membrane capacitor; and $S_i(t)$ is the state of the hysteretic comparator at time t. The first summation is over all the excitatory synapses of the i-th neuron and the second summation is over all the inhibitory synapses.

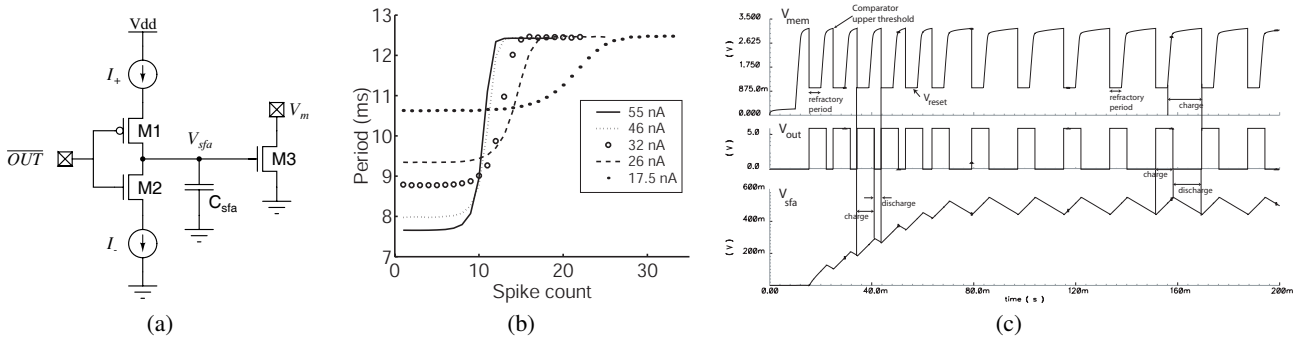


Fig. 2. (a) Spike frequency adaptation circuit; (b) Increase in period of oscillations as the voltage on the SFA capacitor increases; (c) Top: membrane voltage, Center: neuron output, Bottom: SFA capacitor voltage.

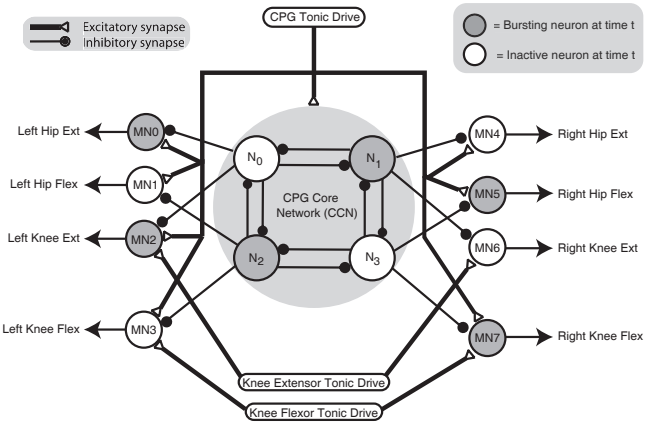


Fig. 3. CPG network. Filled black circles indicate inhibitory synapses, unterminated line segments indicate excitatory synapses.

The discharge and refractory currents, I_d and I_{rf}, are responsible for the rate of discharge and the duration of the refractory period, respectively. The final element represents the current that is drained from the capacitor due to the SFA circuitry, and specifically to the gate voltage on transistor M3, (Fig. 2a). This current is the main source of discharge of the subthreshold contributions; all other dependencies are assumed to be negligible and, with some additional considerations, can be incorporated into I_0.

3. CPG NETWORKS

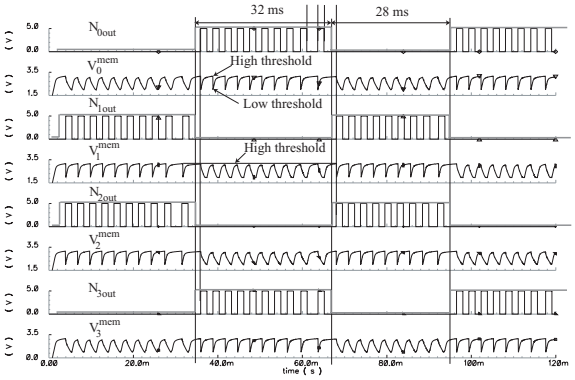
The simplest CPG that can be constructed from these neurons is a half-center oscillator [13]. In this case, two neurons are driven by the same tonic input and are coupled together like N_0 and N_2 in Figure 3. Before going into the details of the elaborate network used for this work, it is worthwhile to explain how the half-center oscillator works. We start by assuming that, although the tonic input is weighted equally by both neurons, due to mismatches in the circuitry one of the two neurons, e.g. N_0, will reach threshold before the other. When it reaches threshold, it inhibits N_2 for the duration of its output pulse. As this occurs, the V_m of N_0 charges up again and will again reach threshold faster than N_2 since N_2 has to recover from inhibition. This process would continue indefinitely in the absence of SFA. However, with SFA, the spike frequency of N_0 decreases as V_{sfa_0} grows. At some point, N_2 will not be significantly inhibited by N_0, and since charge is being drained off of C_{mem_0} by the SFA circuitry, N_2 will reach threshold sooner. It then continues to spike and inhibit N_0 until, as before, the SFA's action becomes dominant, and the process starts anew.

It is important to note that in the half-center oscillator described above, the two neurons will produce 180° out-of-phase bursting patterns. Similarly, in the network depicted in Figure 3 [6], it is clear that if neurons N_0 and N_3 are spiking, then N_1 and N_2 are not, due to the inhibitory connections shown. In this case, this core of four neurons constitutes the system's Central Pattern Generator. This network has the added ability to alter the behavior of appropriate motor neurons to achieve the necessary waveforms required for biped locomotion.

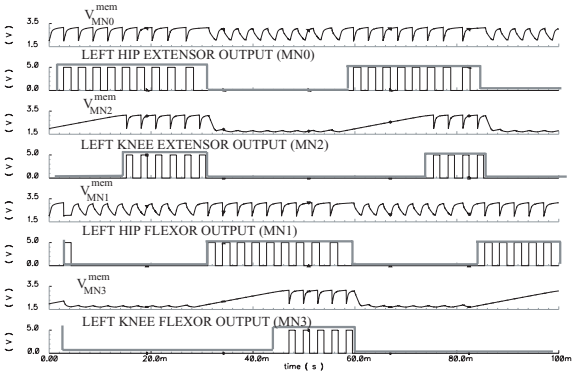
In a normal walking gait, the left and right hips are 180° out-of-phase with each other, whereas the knees are approximately 90° out-of-phase with their respective hip and, consequently, 180° out-of-phase with each other. To achieve the 90° phase delays in our CPG network, it is necessary to weigh the tonic input differently for the knees than for the hips. Specifically, the weight of the tonic inputs to the knee flexor and extensor are weakened such that those motorneurons begin firing after half of the respective hip-burst has elapsed. This results in four different bursting patterns: Figure 4a shows the outputs of the four CPG neurons that form the core network, while Figure 4b shows the motorneurons' waveforms for just the "left leg". Since our design has 20 neurons, all 12 of these signals can be implemented on one chip. Furthermore, by changing the synaptic weights, particularly those governing the impact of the tonic input on the neurons, it is possible to achieve different waveforms that are locked in frequency and are out-of-phase by any desired angle. For example, if desired, the knee bursts can also have 50% duty cycles by adding an additional neuron for two synchronized knee muscles that would set the end of the bursts.

4. CONCLUSION

We have presented a novel design for a silicon central pattern generator and demonstrated how the circuits could be used to construct a feed-forward CPG network with 12 neurons. In the future, we intend to use the chip to control a robotic biped. However, an essential feature of biological CPGs is the use of feedback to modulate the activity [14]. The Redbot robot of Iguana Robotics, Inc. (Fig. 5) has previously been controlled by the 12-neuron network shown here, but only with a computer in the loop [6]. This



(a)



(b)

Fig. 4. (a) CPG neurons' outputs (N_0, N_1, N_2, N_3) and their membrane potentials. (b) Motor neurons' outputs (MN_0, MN_2, MN_1, MN_3) and membrane potentials. The thick grey waveforms in each of the figures represent the envelope of the desired waveforms.

new design will allow for a self-contained solution in which feedback plays a vital role. The feedback will come from a variety of sensors mounted on the robot, relaying proprioceptive, tactile, and visual information. Integrating sensory information into the CPG network is the subject of our future work.

5. ACKNOWLEDGMENTS

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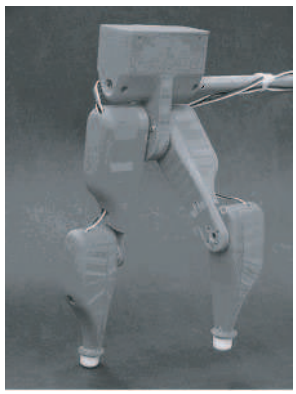

Fig. 5. The "RedBot" robot to be controlled with the networks. The robot stands approximately 28 cm tall.