

Image Sharpness and Beam Focus VLSI Sensors for Adaptive Optics

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Abstract—High-resolution wavefront control for adaptive optics requires accurate sensing of a measure of optical quality. We present two analog very-large-scale-integration (VLSI) image-plane sensors that supply real-time metrics of image and beam quality, for applications in imaging and line-of-sight laser communication. The image metric VLSI sensor quantifies sharpness of the received image in terms of average rectified spatial gradients. The beam metric VLSI sensor returns first and second order spatial moments of the received laser beam to quantify centroid and width. Closed-loop wavefront control of a laser beam through turbulence is demonstrated using a spatial phase modulator and analog VLSI controller that performs stochastic parallel gradient descent of the beam width metric.

Index Terms—Adaptive optics, analog very large scale integration (VLSI), focal-plane image processing, image sensors, optical communication.

I. INTRODUCTION

HIGH-BANDWIDTH line-of-sight laser communication is a rapidly growing field of research with great commercial application. Near-ground laser communication over extended distances is affected by wavefront distortion caused by atmospheric turbulence. Wavefront control through adaptive optics, as used extensively in astronomical imaging, allows one to correct for some of this distortion. Critical to implementing adaptive optics is a technique to accurately and instantaneously estimate the phase of the wavefront and correct for it in real time. Direct sensing of the wavefront involves the use of expensive optical components that complicate system integration.

Among the simplest and most versatile of adaptive wavefront correction techniques is stochastic parallel gradient descent (SPGD) of a chosen measure (“metric”) of optical quality in a closed-loop control system comprising any type of spatial phase modulator [1]. Technologies for high-resolution wavefront shaping are available in various forms including microelectromechanical (MEMS) mirrors and liquid crystal spatial light modulators (LC SLMs). The metric could be any

real-time quantity that indicates system “quality” as affected by the wavefront distortion. Depending on the type of adaptive optical system, the performance metric might be intensity of radiation at the focus [2], [3], image sharpness [4], [5], or scattered field statistical moments [6].

In this paper, we present two analog very-large-scale-integration (VLSI) focal-plane sensors that compute “image quality” for imaging applications and “beam quality” for laser transmitter/receiver applications. Section II reviews SPGD control for adaptive optics in the context of quality metric sensors. Section III discusses previous work on image and beam quality metric sensing. Section IV presents VLSI implementation and experimental validation of an “image quality” metric sensor that computes the high spatial frequency energy content of an image. A laser “beam quality” metric sensor chip that computes the variance of the beam’s cross section, and experimental results that demonstrate use of the “beam quality” metric chip in a closed-loop adaptive optics system, are described in Section V. Section VI closes with concluding remarks.

II. MODEL-FREE CONTROL FOR ADAPTIVE OPTICS

Stochastic approximation techniques [7] are used to evaluate gradients of an objective function where only discrete and noisy observations of the objective are available. The techniques are model-free [8] in that the evaluation of the gradient does not assume knowledge of the function. The model-free approach is attractive for control applications [9] where derivation of functional derivatives of the plant could be complex or unavailable. The advantage of model-free control is that the architecture of the system becomes largely independent of the intricacies of the task and the control and sensing elements used. Model-free control also lends itself to efficient real-time analog hardware implementation [10], [11].

Fig. 1 schematizes the model-free approach to wavefront control using a general “quality” metric [12]. In this schematized laser communication receiver system, the launched beam’s wavefront phase is distorted by atmospheric turbulence encountered along its propagation path. At the receiver, the wavefront passes through an adaptive phase-correcting device (MEMS mirror or LC SLM) and is focused onto a VLSI focal-plane sensor. This sensor computes a scalar metric $J(\mathbf{u})$ which quantifies the “quality” of the received beam (or image). $J(\mathbf{u})$ is a function of all N controllable elements \mathbf{u} in the wavefront phase corrector and provides a scalar feedback signal that is augmented to gradient information through stochastic parallel perturbation of the elements \mathbf{u} .

The model-free perturbative SPGD algorithm is summarized as follows. At every time-step k , the controller differentially per-

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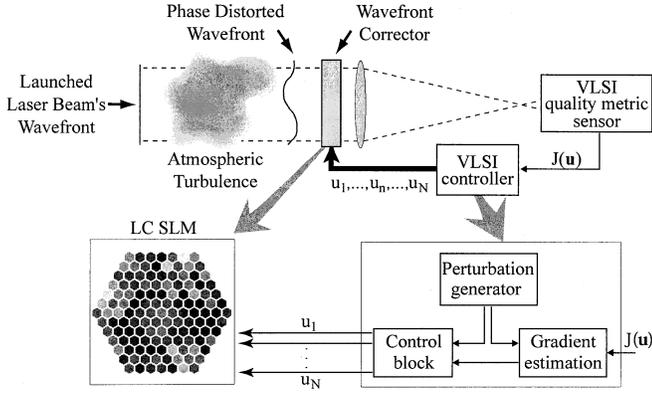


Fig. 1. Adaptive laser optical system architecture. A quality metric sensor provides scalar feedback to the controller which produces parallel updates to the elements of the wavefront corrector.

turbs each element of the wavefront corrector u_j by δu_j and the resulting change in the measured performance metric is evaluated:

$$\delta J^{(k)} = J\left(u_1^{(k)} + \delta u_1^{(k)}, \dots, u_N^{(k)} + \delta u_N^{(k)}\right) - J\left(u_1^{(k)} - \delta u_1^{(k)}, \dots, u_N^{(k)} - \delta u_N^{(k)}\right). \quad (1)$$

Each of the control channels is updated in parallel at every time-step according to the following rule:

$$u_j^{(k+1)} = u_j^{(k)} - \gamma \delta J^{(k)} \delta u_j^{(k)} \quad (2)$$

where γ is a learning-rate parameter.

In model-free optimization, system performance is limited mainly by the precision at which the metric $J(\mathbf{u})$ is acquired. Therefore, a critical component in the stochastic control system for adaptive optics is the metric sensor which quantifies an index of optical quality in real time. The precision of implementing the control algorithms is less critical [13] and allows for compact analog realization for real-time control extending over a large number of parallel channels that directly connect to the parallel input of wavefront correctors [14]–[17].

III. PERFORMANCE METRICS

A. Functional Form

A performance metric $J(\mathbf{u})$ must be carefully defined for the particular application and must be computable in a time much less than the characteristic time of the turbulence (≈ 2 ms). Several “sharpness” metrics have been suggested [4] and, in particular, metrics for “image sharpness” and “focus” have been proposed [18] which take the form

$$J_{\text{image}} = \int_{\mathbf{r}} \|\nabla I(\mathbf{r}, t)\|^\nu d^2\mathbf{r} \quad (3)$$

where ν is a parameter of the selected norm and $\mathbf{r} = \{x, y\}$ represents location in the image-plane.

For laser beam focusing, metrics involve computing the sum over the image plane of functions of the two-dimensional (2-D) beam intensity distribution $I(\mathbf{r}, t)$ as

$$J_{\text{beam}} = \mathcal{F}_r \{I(\mathbf{r}, t)\}. \quad (4)$$

where \mathcal{F} represents some selected function. In the past, computing metrics of the form (4) have proven to be computationally too expensive for real-time applications. In response, Vorontsov *et al.* [5] have suggested speckle field metrics that can be computed rather efficiently from the power spectrum of a single photodetector or from the size and number of speckles falling onto an imaging sensor.

B. VLSI Implementation

Several research groups have developed mixed-mode VLSI chips that reveal edges and locate and track the center of a received image in real time, e.g., bio-inspired retina-like imagers [19], [20], programmable and steerable kernel image template processors [21], [22], edge-tracking image processors [23], [24], and countless others. Most of these chips return the edge information in scanned image output format, which can be conveniently combined into various forms of quality metrics using external sequential processing. To obtain high bandwidth (kilohertz range) in the evaluation of the quality metric requires a custom implementation with continuous-time analog circuitry to aggregate edge information across all pixels in the array. The image sharpness metric (3) with $\nu = 1$ has been implemented in VLSI for computing image focus in real time by Delbrück [25], [26].

To quantify the quality of a received image, the approach taken here is to measure image sharpness in terms of the energy content at high spatial frequencies. Defocus of an image results in attenuation of the high spatial frequencies. A simple measure of high-spatial-frequency energy is chosen for efficient VLSI implementation. The implemented image quality metric (IQM) is the intensity normalized sum of the absolute value of pixel photocurrents convolved with a spatial high-pass filter

$$\text{IQM} = \frac{1}{E} \sum_i \sum_j |I_{i,j} * K|$$

with

$$K = \begin{bmatrix} 0 & -1 & 0 \\ -1 & 4 & -1 \\ 0 & -1 & 0 \end{bmatrix} \quad (5)$$

where $I_{i,j}$ is the intensity at the $(i, j)^{\text{th}}$ pixel and $E = \sum_i \sum_j I_{i,j}$ is the intensity of the received image. These quantities are easily combined using current-mode VLSI circuitry, described in the next section.

Conversely, for determining the quality of a transmitted or received laser beam, the beam variance metric (BVM) is defined as the *variance* of the beam intensity distribution normalized by the square of the intensity

$$\text{BVM} = \frac{N \cdot M}{E^2} \sum_i \sum_j I_{i,j}^2 \quad (6)$$

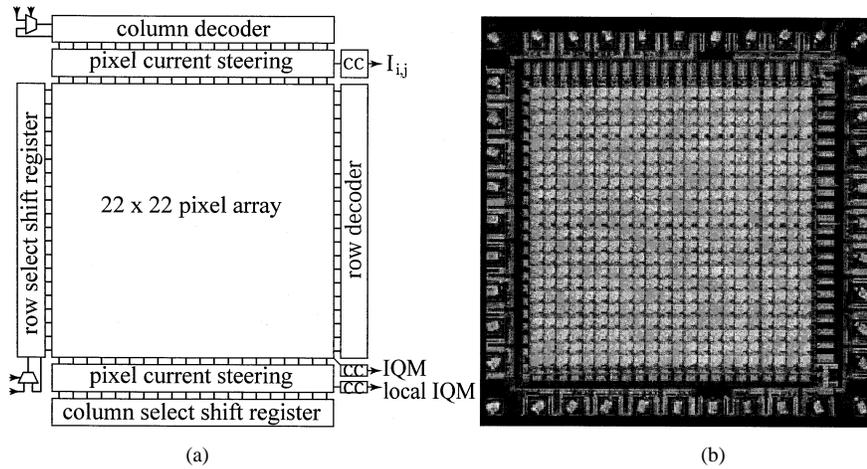


Fig. 2. (a) IQM chip architecture. Row and column decoders allow random access to imager pixels. Row and column shift registers allow readout of user defined pixel groups for local image quality computation. Current steering circuits route the selected pixel currents to current conveyors (cc) which amplify the currents before sending them off-chip. (b) Photomicrograph of the 2.2 x 2.25 mm² IQM sensor chip manufactured through MOSIS in 1.2- μ m CMOS technology.

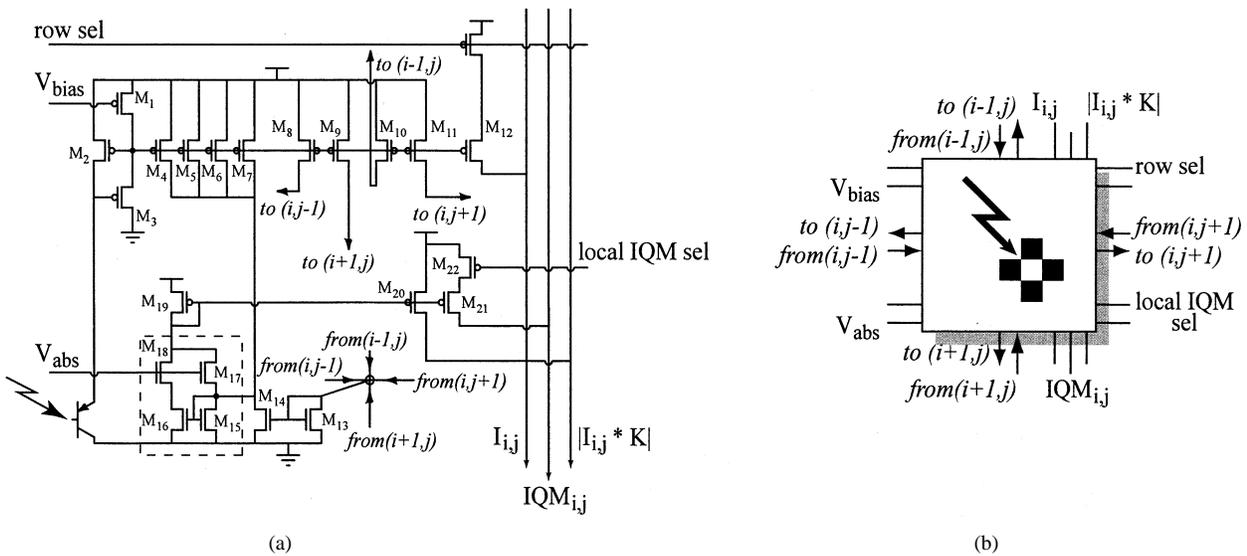


Fig. 3. (a) IQM pixel circuit diagram. (b) Circuit symbol.

where N and M are the number of rows and columns, respectively, in the array of pixels. This metric is suitable for point sources and increases monotonically as the width of the focused beam decreases. In addition, the beam centroid is computed in two dimensions $\{X_C, Y_C\}$.

IV. IMAGE QUALITY METRIC CHIP

A. VLSI Implementation

The IQM chip produces several outputs: a captured image, integral image quality taken over the whole captured image as defined by (5), and regional image quality over a user-defined subregion of the captured image. The chip architecture is shown in Fig. 2(a). It consists of a 22 x 22 array of pixels with perimeter pixels acting as dummy pixels to mitigate array edge effects [27]. Random access readout of pixel currents is provided by row and column decoders at the periphery. Programmable row and column shift registers allow for readout of local image quality from a user-selected group of pixels.

Multiplexers allow for either external loading of the shift registers or internal feedback. Local image quality is a performance metric used in synthetic imaging applications [28]. Current steering circuits route the selected pixel's or group of pixels' currents to current conveyors which amplify the currents before sending them off-chip for current-to-voltage conversion. Fig. 2(b) shows a photomicrograph of the IQM sensor chip.

The pixel circuit diagram and its corresponding circuit symbol are shown in Fig. 3(a) and (b), respectively. A vertical PNP bipolar transistor converts the collected photons into emitter photocurrent $I_{i,j}$. Since nine copies of this current are needed, a current conveyor mirror (transistors M_1 , M_2 , and M_3) sets the gate voltage for current-copying transistors M_8, \dots, M_{12} . The significant capacitive load from these nine transistor gates can be quickly charged/discharged by the current source M_1 whose gate voltage is a global value set off-chip. The convolution kernel K described in (5) is formed as follows: M_4, \dots, M_7 source the central component of the kernel $+4I_{i,j}$ while M_{13} sinks current from the surrounding four pixels $-I_{i+1,j}$, $-I_{i-1,j}$, $-I_{i,j+1}$, and $-I_{i,j-1}$. M_{13}

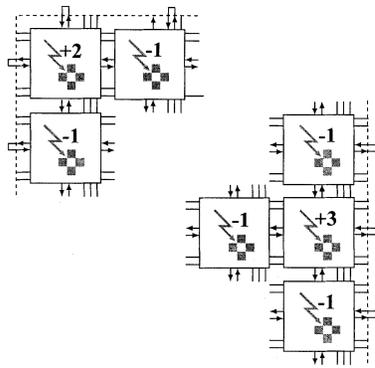


Fig. 4. A single IQM pixel design allows for hard-wiring corner and edge kernels by simply "looping back" the appropriate interconnect currents.

mirrors this current through M_{14} . The difference between M_{14} 's drain current and the currents sourced by M_4, \dots, M_7 is the current $I_{i,j} * K$.

What remains is to compute the absolute value of this current. Transistors M_{15}, \dots, M_{18} shown in the dashed box form a current-mode absolute value circuit. If $I_{i,j} * K$ is positive, it is mirrored down the left side by M_{16} and sourced by diode-connected M_{19} . If negative, the current is directly sourced down the right side by M_{19} . M_{18} is a cascode for the mirror formed by M_{15} and M_{16} . Its gate voltage is a global bias signal set off-chip. M_{17} makes the absolute value circuit symmetric. The current through M_{19} , $|I_{i,j} * K|$ is mirrored by M_{20} . M_{20} 's drain is connected in common for all pixels in the array giving a total current of $\sum_i^N \sum_j^M |I_{i,j} * K|$.

If the local IQM sel line (common for that row) is low, M_{22} is on, and M_{21} sources its current to the current steering circuits at the bottom periphery of the chip. The currents sourced by M_8, \dots, M_{12} are distributed to the neighboring four pixels $I_{i+1,j}$, $I_{i-1,j}$, $I_{i,j+1}$, and $I_{i,j-1}$ for computing their own convolutions. The fabricated pixel measures $120 \mu\text{m}$ on a side in a $1.2\text{-}\mu\text{m}$ technology.

To utilize the entire 22×22 array of pixels for computing IQM, the spatial high-pass filter K is appropriately adjusted at the corners of the array and along each edge of the array, as shown in Fig. 4. The pixel's input and output currents that constitute the hard-wired kernel are simply looped back when they have no neighboring pixels.

For readout of $I_{i,j}$, a 5-b row decoder at the periphery selects the i^{th} row and all pixels in that row send their currents $I_{i,j}$ for $j = 1, \dots, 20$ to the current steering network at the top of the chip. A 5-b column decoder selects the j^{th} column and the selected pixel's current $I_{i,j}$ is steered to the periphery. The remaining unselected pixels' current in the selected i^{th} row are steered along a dummy line to the periphery. Both the selected and dummy lines are held at a fixed readout potential provided to the chip as a global bias voltage.

Readout of the local image quality metric is performed in a similar fashion. The programmable row and column shift registers take the place of the decoders. The row shift register selects a subset of rows in the array by pulling down the local IQM sel line. Currents from selected rows accumulate down the columns. Those columns that are selected by the column shift register steer their currents to a common node which yields the

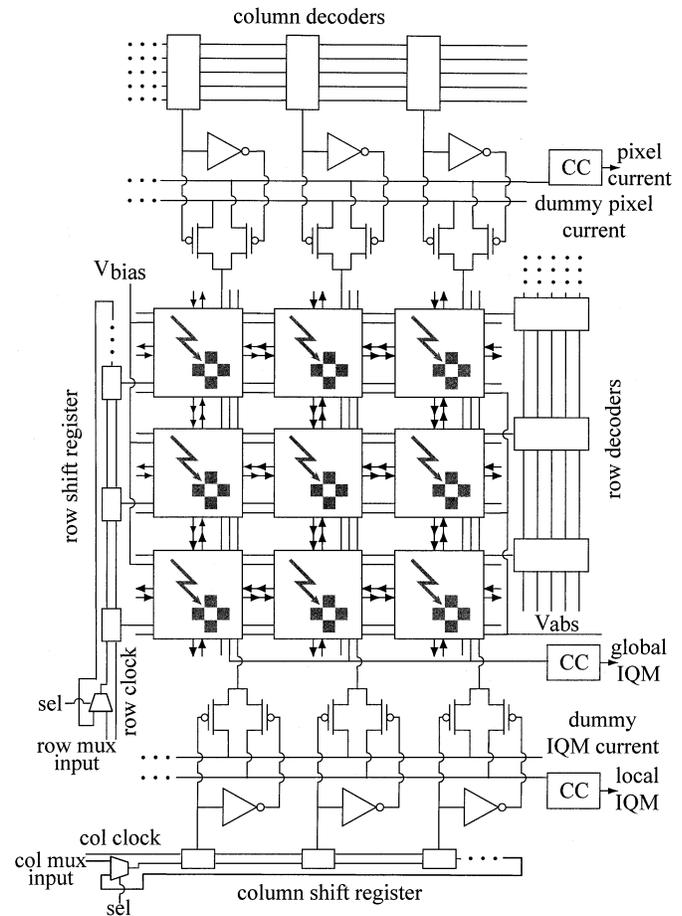


Fig. 5. Detailed view of a 3×3 IQM pixel array showing row-and-column decoders and current steering network for pixel current $I_{i,j}$ readout, and row-and-column shift registers for image map IQM_{local} readout.

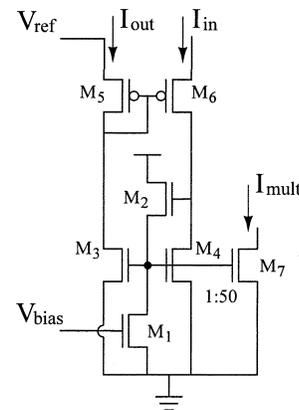


Fig. 6. CMOS current conveyor current mirror.

local image quality for the selected subset of pixels. Those that are not selected steer their currents to a dummy line.

Since the row and column shift registers can be individually clocked, the programmed grouping of pixels which contribute to the local image quality can be scanned across the chip. The current collection nodes are also held at a fixed potential.

Fig. 5 shows detailed system connectivity for the decoders, shift registers, current steering, and readout current amplification for a 3×3 array of pixels.

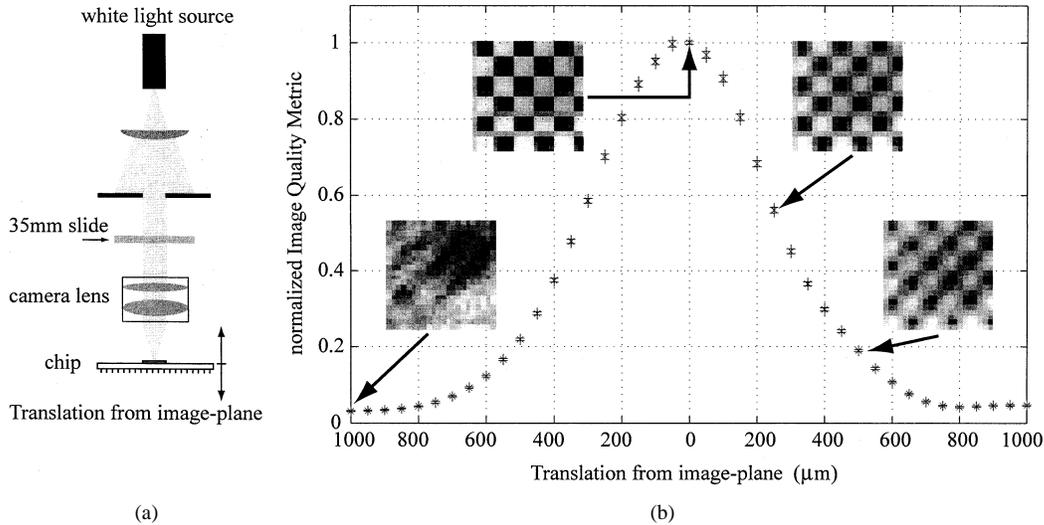


Fig. 7. Bench-top testing of the image quality metric chip. (a) Experimental setup. (b) Experimental Results.

The currents $I_{i,j}$, IQM and local IQM are each sent to an on-chip CMOS current conveyor [29], [30] which clamps the voltage at which the current is read and further amplifies the current before it is sent off-chip.

Fig. 6 shows the circuit schematic for the CMOS current conveyor current mirror. Input current I_{in} enters the low impedance source of M_6 . All four transistors M_3, \dots, M_6 pass the same current so I_{out} is a copy of I_{in} . The source of M_3 is held at an externally set potential V_{ref} and an equal voltage appears at the source of M_6 . M_1 and M_2 form a source follower so that M_4 's gate voltage follows its drain voltage and passes current I_{in} . M_1 's gate potential V_{bias} is set off-chip. The follower facilitates rapid charging and discharging of the large gate capacitance presented by transistors M_3, M_4 , and M_7 . The gained-up ($\approx 50\times$) output current I_{mult} is available at the high impedance drain of M_7 .

B. Experimental Results

Experimental results characterizing the IQM sensor chip are given in Fig. 7(a). A white light source was used to illuminate a grayscale 35-mm slide whose image was focused down onto the chip surface. The chip was mounted on a translation stage so that it could be moved into and out of the image plane. The 35-mm slide's image consisted of a grayscale checkerboard pattern. The chip was moved 1 mm on either side of the image plane in steps of $50 \mu\text{m}$. At each position we recorded the IQM returned by the chip and scanned the image captured by the chip. Fig. 7(b) plots the recorded normalized IQM as a function of displacement from the image plane with error bars indicating ± 3 standard deviations in the measurement. The insets show four representative images scanned off the chip for various displacements from the image plane.

Fig. 8 shows the IQM measured on-chip plotted against the IQM calculated from the image captured by the chip, with both axes normalized with respect to their maxima. We also scanned the local image quality map (i.e., $IQM_{local,i,j} = |I_{i,j} * K|$). Four scanned images and their corresponding local image quality maps are plotted for the locations marked 1...4 on the graph. The linear relationship between the measured and

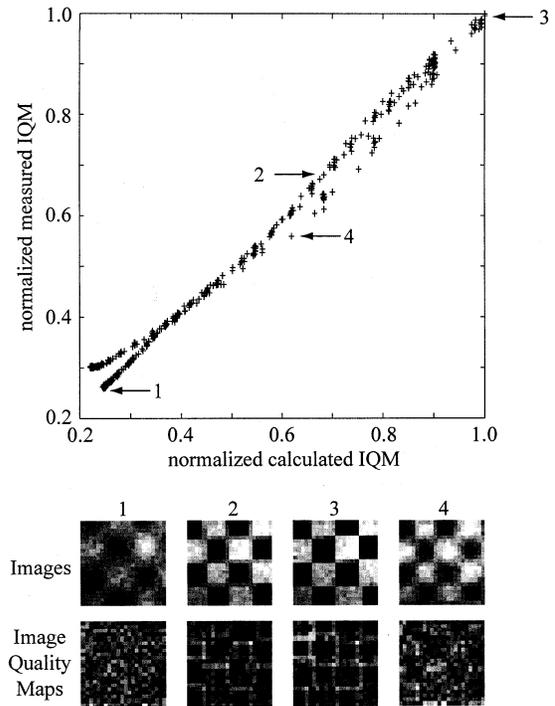


Fig. 8. Normalized IQM measured on-chip versus normalized IQM calculated off-chip from the captured image. Captured images and image quality maps correspond to the four positions marked on the graph.

calculated IQM values indicates that the on-chip circuitry for calculating the global IQM is accurate. Having access to the local IQM is important because it allows one to compute and visualize the image quality map at different levels of granularity.

V. BVM CHIP

A. VLSI Implementation

The BVM chip images the focused laser beam, computes the beam variance metric as described in (6), and calculates the beam centroid. Fig. 9(a) shows the floorplan of the BVM chip. It consists of a 20×20 array of pixels surrounded by a ring of

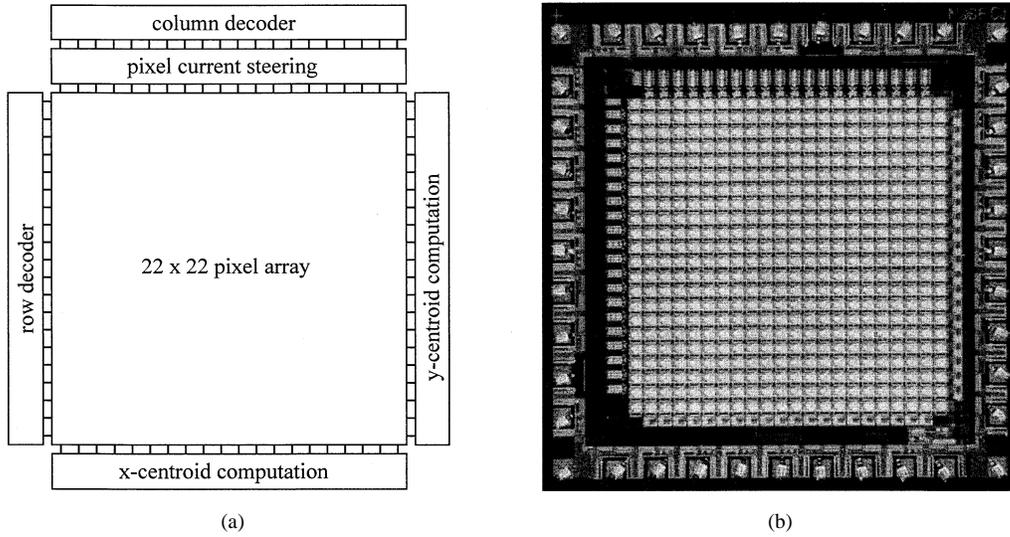


Fig. 9. (a) BVM chip architecture. Row and column decoders provide random access readout of the 20×20 image. Current steering circuits route the selected pixel current off chip. x and y centroid circuits utilize pixel row and column sums at the periphery. (b) Photomicrograph of the 2.2×2.25 mm² BVM sensor chip manufactured through MOSIS in $1.2\text{-}\mu\text{m}$ CMOS technology.

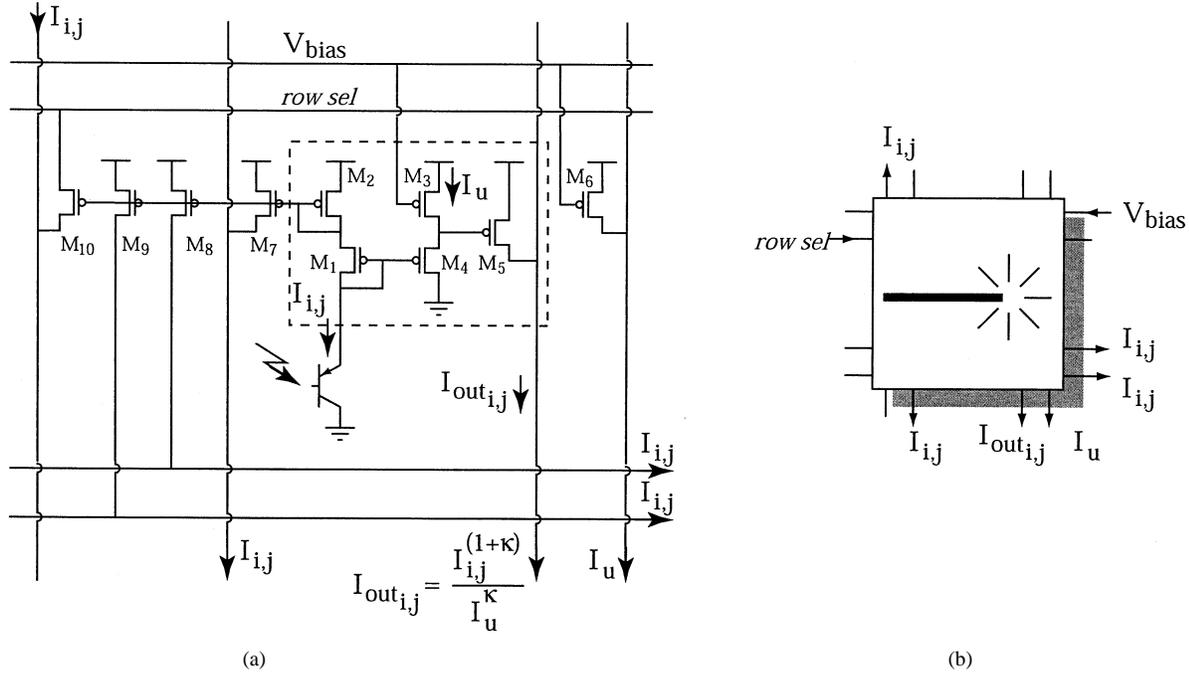


Fig. 10. (a) BVM pixel circuit diagram. (b) Circuit symbol.

dummy pixels. Row and column decoders provide random access pixel current $I_{i,j}$ readout. Once a row has been selected, current steering circuits at the top of each column route the selected column's current to an output current line with all other nonselected column's currents routed to a dummy line. Both lines are held at the same fixed reference potential off-chip. Pixel row and column sums are continuously available for computing the beam's x - and y -centroid location $\{X_C, Y_C\}$ using signal aggregation across coupled transconductance amplifiers [31]. These signals are used directly to control tip-tilt mirrors. A photomicrograph of the BVM sensor chip is shown in Fig. 9(b).

Fig. 10 shows the pixel circuit diagram along with its circuit symbol. Each pixel measures $70 \times 70 \mu\text{m}^2$ in a $1.2\text{-}\mu\text{m}$ technology. A vertical bipolar phototransistor produces an emitter

current $I_{i,j}$ proportional to the received photon energy. $I_{i,j}$ is copied by transistors M_7 , M_8 , and M_9 . The first two copies are summed down columns and across rows, respectively, to form row and column sums at the periphery. M_9 sources $I_{i,j}$ to the current steering circuit at the top of the j^{th} column only when its source is pulled high by the i^{th} row select line. The row select line can be pulled slightly higher than the analog supply voltage to amplify the pixel current. The remaining transistors are used for computing the summands in (6).

When operating in the subthreshold regime, M_1, \dots, M_5 form a translinear loop [32], [20] such that

$$I_{out,i,j} = \frac{I_{i,j} I_{i,j}^\kappa}{I_u^\kappa} \quad (7)$$

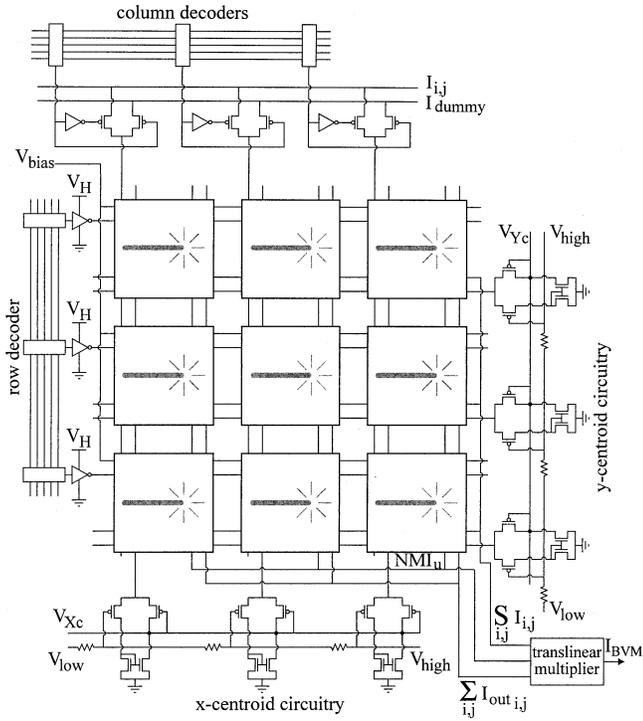


Fig. 11. Example 3×3 array of BVM pixels showing their peripheral support circuits: row and column decoders, current steering network, x and y centroid computation and translinear multiplier.

where I_u is a subthreshold bias current and $\kappa \approx 0.6$ is the subthreshold slope factor for a pMOS transistor.¹ M_3 and M_6 's gate voltages are globally connected and set off-chip. M_6 sources a copy of the bias current I_u which is globally summed to produce $NM I_u$ necessary for proper normalization of the current-domain equivalent(6)

$$BVM = \frac{N \cdot M \cdot I_u \sum_i \sum_j \frac{I_{i,j}^{(1+\kappa)}}{I_u^\kappa}}{\left(\sum_i \sum_j I_{i,j} \right)^2}. \quad (8)$$

An example 3×3 array of pixels and their associated peripheral support circuitry are shown in Fig. 11. Row-and-column decoders select the $\{i, j\}^{\text{th}}$ pixel for readout. The selected pixel's current $I_{i,j}$ is steered to the periphery where it is read off-chip at a fixed potential. All unselected pixels' currents contribute to I_{dummy} which is also held at the same fixed readout potential. The sum of each row's and each column's pixel currents are used at the periphery to bias operational transconductance amplifiers that participate in the distributed computation of x and y centroids [31].

All currents that contribute to the calculation of the BVM (6), namely I_u , $NM I_u$, $\sum_{i,j} I_{i,j}$, and $\sum_{i,j} I_{out\ i,j}$, are used in the vertical NPN bipolar transistor translinear circuit [32] shown at the bottom right of Fig. 11.

¹If transistors M_1 and M_4 were each in a separate n -well with their sources tied to their own well potential, κ would drop out of (7) to give $I_{out\ i,j} \propto I_{i,j}^2$.

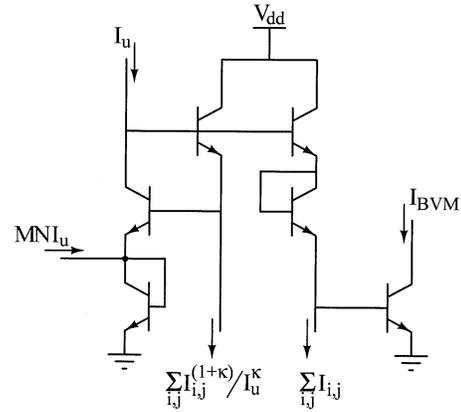


Fig. 12. Vertical NPN bipolar transistor translinear circuit used at the periphery to compute the current-domain form of the beam variance metric I_{BVM} .

Fig. 12 gives the circuit schematic for this bipolar translinear circuit that is used to compute the final current-domain approximation of the BVM (6) as

$$I_{BVM} = \frac{(NM + 1) I_u^2 \sum_i \sum_j I_{out\ i,j}}{\left(\sum_i \sum_j I_{i,j} \right)^2}. \quad (9)$$

B. Experimental Results

We tested the BVM chip using a similar setup to that used for testing the IQM sensor chip, shown in Fig. 13(a). The BVM chip was mounted on a translation stage that could be moved toward or away from the light source using a vernier. A fiber-optic white light source was focused down onto the chip surface which was positioned at the image plane. Moving the chip in front of and behind the image plane allows us to defocus the beam, thereby diffusing the image intensity profile across neighboring pixels. Experimental results of the BVM as a function of the distance away from the image plane are shown in Fig. 13(b).

To compare the BVM measured on-chip with the BVM calculated off-chip from the acquired images, we used an experimental setup similar to that depicted in Fig. 13, except that we used a laser to supply beams of different widths that we focused down onto the chip. The off-chip calculated BVM was computed from the image captured by the chip. Fig. 14 plots the results.

For wide beams, the light intensity profile extends across many pixels so that the resulting photocurrents are low (< 40 nA). As a consequence, the transistors in each pixel's translinear current squaring circuit all operate in their subthreshold regime. When the beam is compact, the photo-generated pixel current is large (> 100 nA) and the translinear circuit operates with above threshold currents. The plot shows a linear regression line drawn through the subthreshold data and another drawn through the above threshold data. Four images captured by the BVM chip are also shown in Fig. 14.

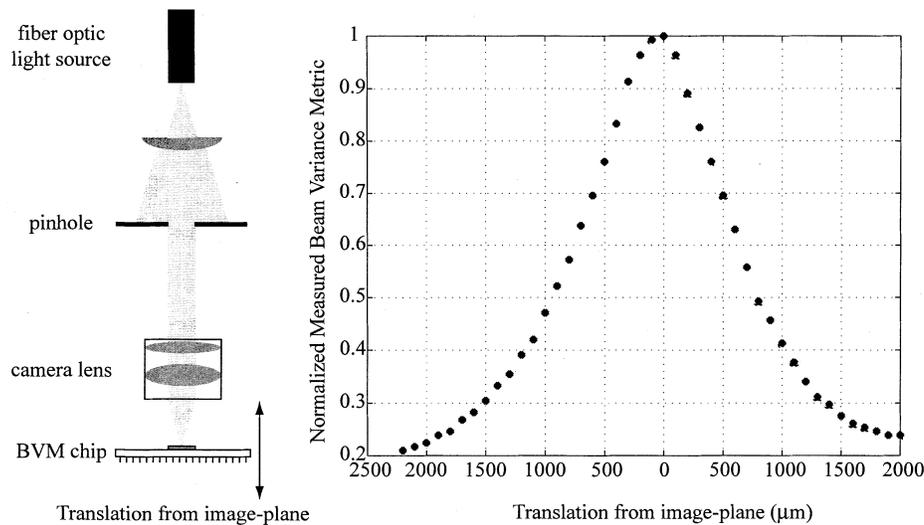


Fig. 13. Bench-top testing of the beam variance metric chip. (a) Experimental setup. (b) Experimental results.

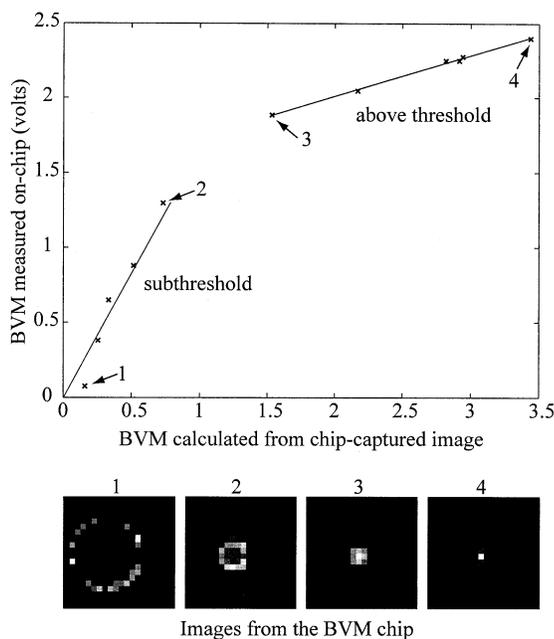


Fig. 14. Experiments on the BVM chip using “real laser beams” demonstrate a monotonic relationship between BVM measured on-chip and BVM calculated off-chip from acquired images. The subthreshold curve is for data where photogenerated pixel currents are subthreshold (wide beams) while the above threshold curve is representative of above threshold pixel currents (compact beams). The displayed chip-captured images of four different beam widths correspond with their BVM values shown in the graph.

The number above each image corresponds with positions 1–4 shown on the graph.

The monotonic nature of the measured versus calculated BVM is important, and the decrease in the slope of this relationship from the subthreshold to the above-threshold regimes of operation is expected.² In fact, the shape of this relationship is desirable for the dynamics of adaptation where the chip supplies the BVM signal $J(\mathbf{u})$ to the controller. The rate of adaptation is fast far from convergence for a wide beam because

²In the subthreshold regime, the photogenerated current is raised to a power > 1 by the translinear circuit, while the above-threshold region has reduced gain.

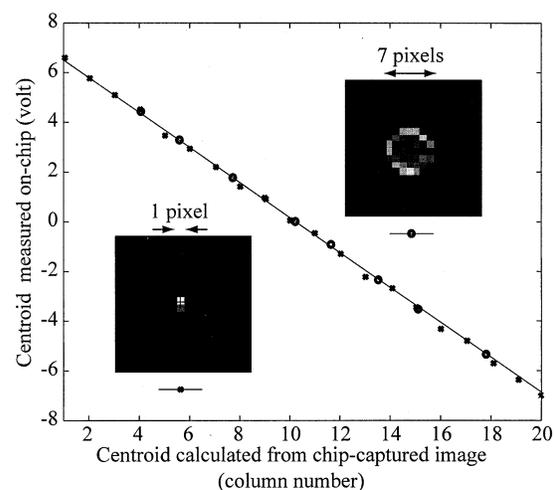


Fig. 15. On-chip computed x -centroid versus calculated x -centroid for two different laser beam widths. Linear regression line through all data demonstrates good accuracy and linearity. Chip-captured images of the beams showing the two beam widths used to collect the data.

of the high slope. Conversely, the adaptation rate decreases as the beam becomes more compact near convergence.

Experimental results of the centroid computation circuits on the chip are given in Fig. 15, confirming high linearity of the estimated centroids both for wide and narrow beams.

The corrective capacity of the BVM sensor chip was evaluated in the closed-loop adaptive optical setup shown in Fig. 16. The beam from an Argon laser ($\lambda = 514$ nm) was expanded to a diameter of 12 mm, reflected off of a 2-degrees-of-freedom x, y -tilt mirror, and then reflected off of a deformable membrane MEMS mirror. The AdOpt system [14] controlled all 37 elements of the MEMS mirror using the SPGD control law described in Section II. As a basis for comparison, a simple feedback signal used in adaptive optics experiments is the Strehl ratio of the focused beam, implemented with a photodetector measuring the intensity of the beam passing through a pinhole. When the beam’s wavefront has been corrected, the compact beam passes most of its energy through the pinhole and the photodetector registers a large output voltage. Both pinhole and

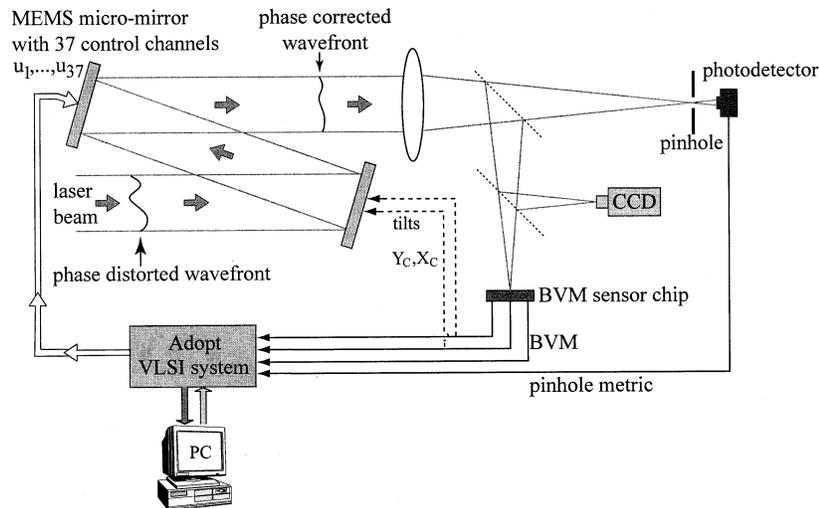


Fig. 16. Experimental setup for verifying correct performance of the BVM sensor chip in a closed-loop adaptive optics task.

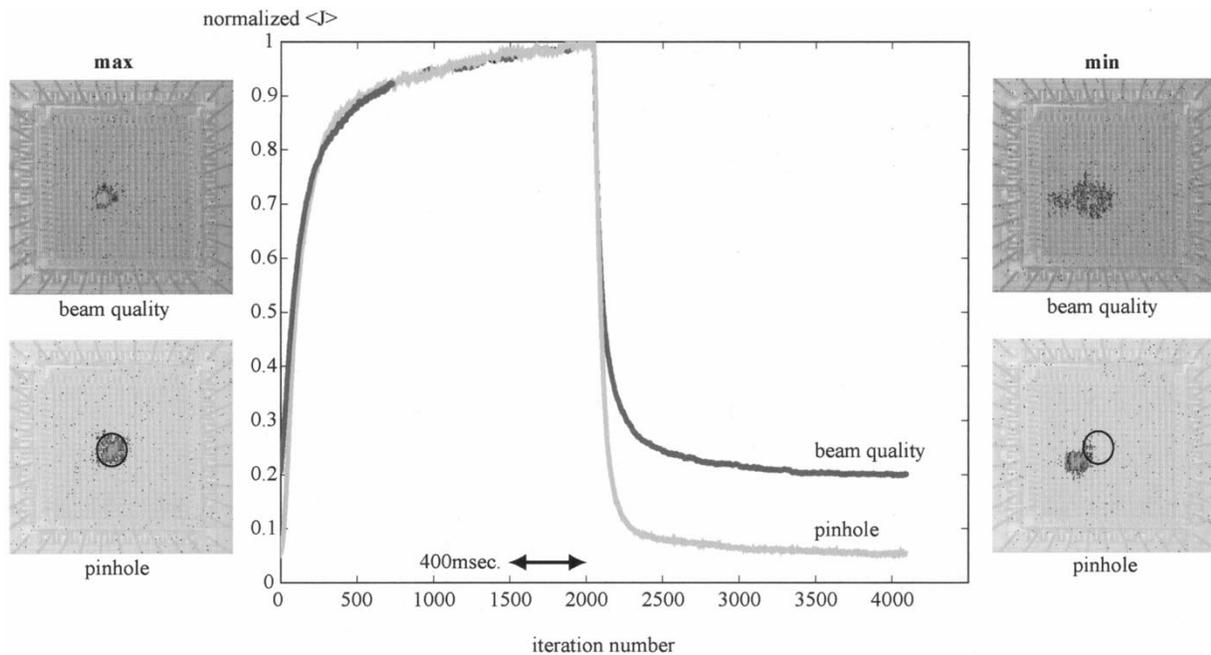


Fig. 17. Experimental results comparing the performance and shape of the focused beam for pinhole and beam variance metrics.

BVM metrics were interfaced with a personal computer (PC). The PC supplies timing signals and bias voltages to the AdOpt VLSI system and also records and displays system performance in real-time.

We instructed the system to repeatedly maximize then minimize the performance metric and collected data from 100 such cycles using first the *pinhole metric* and then the BVM. Fig. 17 shows the results. The normalized mean performance for both pinhole and beam variance metrics are plotted against iteration number for metric maximization followed by metric minimization. The pinhole metric produces a higher dynamic range than the beam quality metric. The CCD images to the left and right of this plot explain why. To the left, we plot the imaged beam on the surface of the BVM chip for metric maximization and to the right for metric minimization. The position and relative size of the pinhole are marked for comparison on the chip image

for the *pinhole* case. During metric maximization, the *beam variance* metric produces a compact circular beam (high output voltage), while during metric minimization it produces a diffuse beam (low output voltage). The *pinhole* metric produces a less compact, elliptically shaped beam during maximization and for minimization simply steers the beam out of the pinhole (output voltage close to zero). For both metrics, maximization takes about 1 s while minimization takes about 0.5 s. The overall speed of the closed-loop system is determined by the speed of the wavefront corrector's actuators and not by the speed of the BVM sensor.

VI. CONCLUSION

The model-free approach to wavefront control relaxes requirements on the design of the sensor array quantifying

TABLE I
CHARACTERISTICS OF IQM AND BVM SENSORS

	IQM chip	BVM chip
Chip size	2.2mm × 2.25mm	2.2mm × 2.25mm
Technology	1.2μm CMOS	1.2μm CMOS
Array size	22 × 22	20 × 20
Pixel size	120μm × 120μm	70μm × 70μm
Fill factor	10%	33%
Dynamic range	36dB	30dB
Bandwidth	7KHz	5KHz
Video scan rate	30Hz	30Hz
Power consumed	0.7mW	0.55mW

wavefront distortion. Direct measurement of the phase of the wavefront incurs physical resources that are hard to integrate. The model-free approach shifts the burden from direct estimation of wavefront control variables to that of accurately acquiring a direct measure of quality. This paper has presented two designs of image-plane VLSI sensors that compute metrics of image sharpness and beam compactness.

For imaging tasks, the IQM chip computes a measure of the high-spatial-frequency energy content of an image is computed on the focal plane in real time, for imaging applications. For line-of-sight laser communication applications, the BVM chip computes energy distribution and centroid of a laser beam. The BVM chip was used as the feedback sensor in a hybrid adaptive VLSI/optical control system and yielded better performance than a commonly used pinhole metric sensor.

Table I lists the size and performance characteristics for the two sensors. At 1-kHz bandwidth, the IQM sensor performs 3.5 GOPS/W and the BVM sensor performs 1.5 GOPS/W.

The sensors can be used with other wavefront control modalities that directly or indirectly perform gradient descent on the quality metrics, e.g., multidithering. It is also possible to augment the sensors with other sensor arrays that reveal partial gradient information to construct control systems of higher corrective power or faster convergence.

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