Micropower CMOS Integrated Low-Noise Amplification, Filtering, and Digitization of Multimodal Neuropotentials

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***Abstract*—Electrical activity in the brain spans a wide range of spatial and temporal scales, requiring simultaneous recording of multiple modalities of neurophysiological signals in order to capture various aspects of brain state dynamics. Here, we present a 16-channel neural interface integrated circuit fabricated in a 0.5 μm 3M2P CMOS process for selective digital acquisition of biopotentials across the spectrum of neural signal modalities in the brain, ranging from single spike action potentials to local field potentials (LFP), electrocorticograms (ECoG), and electroencephalograms (EEG). Each channel is composed of a tunable bandwidth, fixed gain front-end amplifier and a programmable gain/resolution continuous-time incremental $\Delta\Sigma$ analog-to-digital converter (ADC). A two-stage topology for the front-end voltage amplifier with capacitive feedback offers independent tuning of the amplifier bandpass frequency corners, and attains a noise efficiency factor (NEF) of 2.9 at 8.2 kHz bandwidth for spike recording, and a NEF of 3.2 at 140 Hz bandwidth for EEG recording. The amplifier has a measured midband gain of 39.6 dB, frequency response from 0.2 Hz to 8.2 kHz, and an input-referred noise of 1.94 $\mu V_{\rm rms}$ while drawing 12.2 μA of current from a 3.3 V supply. The lower and higher cutoff frequencies of the bandpass filter are adjustable from 0.2 to 94 Hz and 140 Hz to 8.2 kHz, respectively. At 10-bit resolution, the ADC has an SNDR of 56 dB while consuming 76 μW power. Time-modulation feedback in the ADC offers programmable digital gain (1-4096) for auto-ranging, further improving the dynamic range and linearity of the ADC. Experimental recordings with the system show spike signals in rat somatosensory cortex as well as alpha EEG activity in a human subject.**

***Index Terms*—Analog VLSI, biopotential amplifier, digital telemetry, electrocorticogram, electroencephalogram, local field potentials, micropower instrumentation, neural interface.**

I. Introduction

ADVANCES in neuroscience research and clinical applications increasingly call for low-noise low-power integrated simultaneous recording of electrical potentials over large numbers of electrodes in the brain and the body. Implanted deep in the brain, these electrodes convey both high-frequency content of individual neuron action potentials (spikes), and lower-frequency content of local field potential (LFP) neural activity. Arrays of electrodes on the cortical surface or placed noninvasively on the scalp convey brain signals with further reduced frequency content known as electrocorticograms (ECoG) and electroencephalograms (EEG), respectively.

Spike recordings usually convey the extracellular electrical activity of a single neuron unit. Depending on distance between the active neuron and the recording electrode, the amplitude of the extracellular spike signal is on the order of 500 μV and its frequency content ranges from 100 Hz to 7 kHz [1]. These recordings can be obtained using a single electrode or a microelectrode array [2]–[4]. LFPs are the result of collective synaptic activities of large assemblies of neurons around the recording electrode [5]. These signals may have amplitudes as high as 1 mV with frequency content up to 200 Hz [6]. LFPs may be recorded using the same electrodes as spikes. Electrical activity recorded from the surface of the brain (ECoG) or the scalp (EEG) using surface electrodes conveys brain wave signals that result from the volume conduction of coherent, collective neuronal activity over larger scales, throughout the brain. The power spectrum of EEG and ECoG signals is typically confined to 100 Hz and 200 Hz, respectively. The signal amplitude varies from 10 to 5000 μV for ECoG signals, and from 5 to 300 μV for EEG signals [7].

These various modalities of neural signals span a wide range of frequencies and amplitudes. Hence, an interface circuit for acquisition of biopotentials that can accommodate the above ranges and selectively isolate a signal of interest on demand, offers great advantages over an otherwise equally capable circuit confined to one specific signal modality. To be further useful, the system should also have low input-referred noise and should be able to remove the large dc offset on the signal due to the electrode-tissue interface without compromising the information-bearing low-frequency components of the signal. Over the years, several VLSI systems have been developed [8]–[23] to meet low noise and low power constraints imposed by the range of signal frequencies and amplitudes of interest to neuroscience and biomedicine. Typically the range of frequencies covered by any one of these systems is limited to one or two signal modalities, to accommodate high efficiency for the targeted application.

Harrison *et al.* [12] described a spike recording circuit with a bandwidth of 0.025 Hz to 7.2 kHz, input-referred noise of

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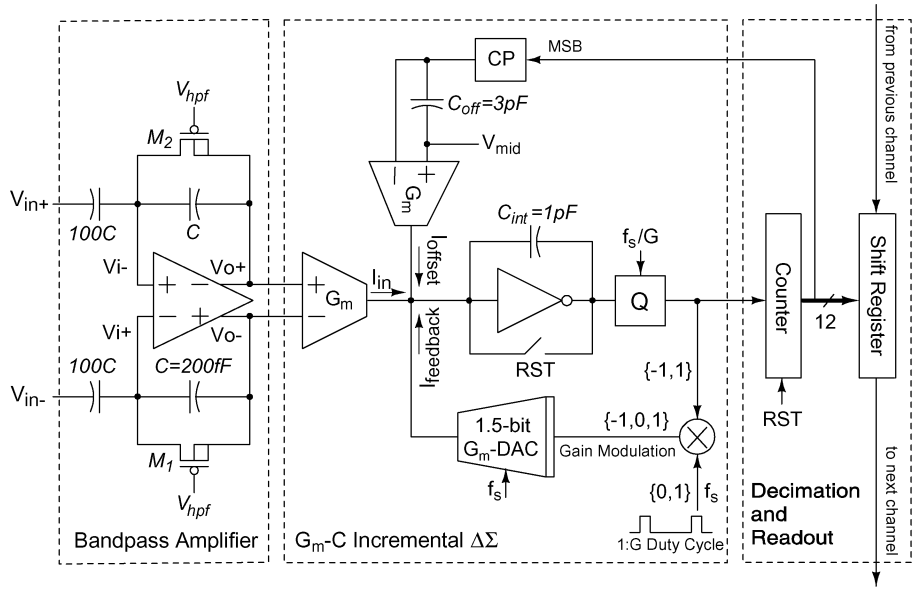

Fig. 1. Functional block diagram for one channel of the 16-channel biopotential ADC.

2.2 $\mu V_{\rm rms}$ and power dissipation of 80 μW. A modified version of the circuit with a bandwidth of 30 Hz and power dissipation of 0.9 μW was also used as an EEG amplifier. Perelman *et al.* [17] reported a system which separates spikes from LFP after amplification. The amplifier has an input-referred noise of 3 $\mu V_{\rm rms}$ for a current consumption of 75 μA in the amplification stage. A biopotential acquisition system with a 57 nV/$\sqrt{\rm Hz}$ input-referred voltage noise density and 60 μW power consumption capable of recording all biopotentials was reported by Yazicioglu *et al.* [20]. The amplifier uses a chopping technique to reduce the 1/f noise corner with a slight increase in power dissipation, and requires external components to implement highpass filtering. Lower power consumption with chopping for 1/f compensation is accomplished by adaptive feedback in the chopped signal [21]. A neural recording amplifier with two bandwidth settings for LFP and spike recording is reported in [22]. The design uses a folded cascode OTA in the input stage and has an input-referred noise of 3 $\mu V_{\rm rms}$ while consuming 7.56 μW of power from a 2.8 V supply.

Here, we present a 16-channel CMOS neural interface circuit with adjustable bandwidth, gain and resolution for the acquisition of biopotentials from the brain. The flexible design of the system and individual programmability of the channels enables capturing multimodal information across a wide frequency range of neural signals from spikes to EEG, while offering consistently low-noise and low-power performance over the range of frequency settings. For *in vivo* implantable instrumentation, the chip also includes digital readout in a bit-serial format compatible with wireless digital telemetry [24] as an alternative to analog wireless telemetry [25].

Section II describes the system architecture of the VLSI chip. Results of benchtop characterization and *in-vivo* recordings follow in Section III, and Section IV concludes the paper.

II. System Architecture

The neural biopotential interface circuit contains 16 parallel differential voltage input, serial digital output channels for acquisition of neurophysiological signals. Fig. 1 shows the block diagram of one channel. Each channel consists of a bandpass amplifier, a $G_m - {\rm C}$ incremental $\Delta\Sigma$ ADC and decimation and readout circuitry. Two stages of gain are implemented in the system; a constant gain in the front-end amplifier, and a variable digital gain in the ADC stage. The amplifier's midband gain, $A_m = 100$ (40 dB), is set by the capacitor ratio $100C/C$, where C is 200 fF. Tunable filtering is incorporated in the amplifier stage itself. The low-end (highpass) cutoff frequency is set by the pseudo-resistive elements in the feedback loop (M_1 and M_2) and C as $1/2\pi {\rm R}C$ where R is the resistance of M_1 and M_2 which is controlled by their gate voltage, $V_{\rm hpf}$ [26]. The high-end (lowpass) cutoff frequency is set by the unity gain frequency of the amplifier, f_u, and A_m as f_u/A_m. The high-end cutoff can be controlled by changing the g_m of the amplifier which results in a change in f_u.

The differential output voltage of the amplifier is then digitized by a 12-bit nominal, $G_m - {\rm C}$ continuous-time, incremental $\Delta\Sigma$ ADC. The differential signal is first converted to a current by an operational transconductance amplifier (OTA). The difference between this current and the $\Delta\Sigma$ feedback current is then integrated on a capacitance $C_{\rm int}$ during the quantization cycle. The core of this ADC is a modified version of the ADC presented previously in [27]. This ADC structure was chosen for two reasons: because the continuous-time integration by the Gm-C input stage obliterates the need for sampling and thus for anti-alias filtering, and because the flexibility in choosing the number of bits allows optimal setting of resolution versus conversion bandwidth as dictated by the signals of interest; e.g., 7-bit at 16,000 samples/s for spikes and 12-bit at 500 samples/s for EEG recordings. The digital gain modulation implements duty cycle modulation in the $\Delta\Sigma$ current feedback, offering a precise and programmable digital gain between 1 and 4096. This gain modulation also decreases the quantization noise of the ADC since the input current is integrated over a longer time interval, albeit at the expense of a proportionally slower sampling rate. Thus, the system allows a configurable tradeoff between

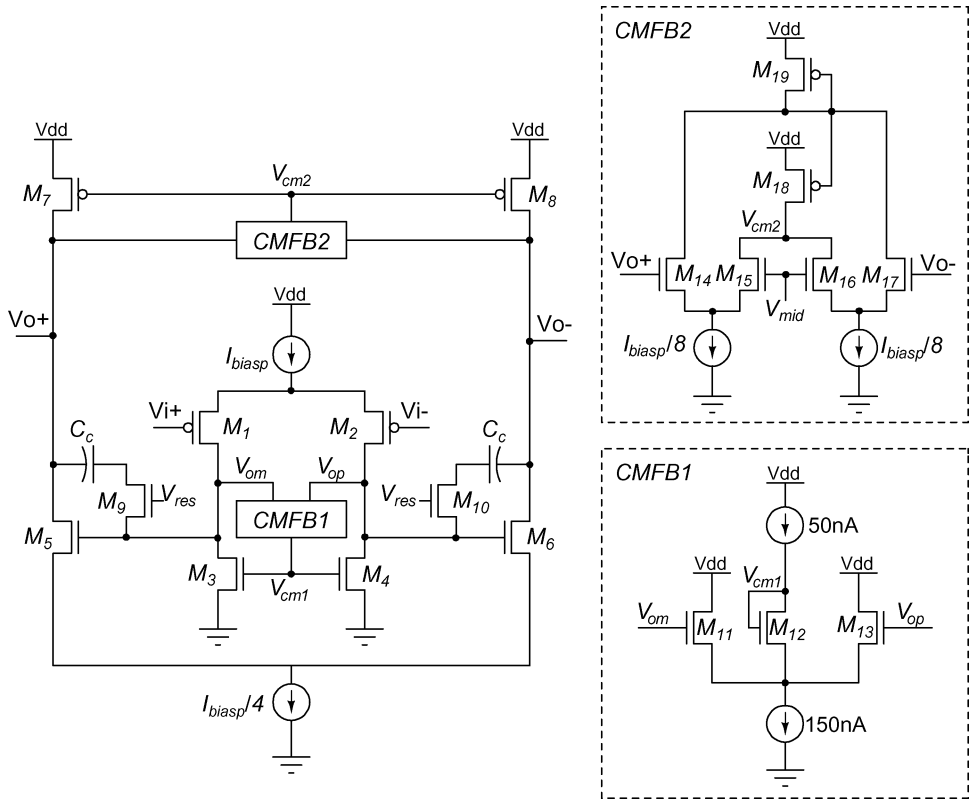

Fig. 2. Fully differential two-stage amplifier in the bandpass amplifier frontend of Fig. 1.

sampling rate and SNR. This along with the tunable filters allow the system to handle a wide gamut of neural signals from weak and slow (EEG, ECoG) to stronger and faster (spikes). In order to compensate for the inherent offset in the OTA stage, a charge pump circuit was added to nullify the output current of the OTA for zero input voltage. The control signal of the charge pump comes from the MSB of the digitized output such that when the bit is predominantly high (low), a respective dc current is added to (subtracted from) the output current of the OTA. This results in a midscale output of the ADC for a dc signal.

The digitized output then goes to the decimation and readout circuitry. The parallel-in serial-out circuitry of each channel is connected in a daisy chain fashion to the next channel in order to have a single-bit serial output. For benchtop characterization (Section III) this serial output was connected to a National Instruments DAQ data acquisition card to read the data into a computer.

A. Amplifier

The circuit diagram of the amplifier is shown in Fig. 2. The design is a two-stage fully differential voltage amplifier with independent common-mode feedback circuitry in each stage. The input transistors M_1 and M_2 were chosen as p-channel devices for lower 1/f noise. For balancing of the bias currents, transistors $M_1 - M_4$ and $M_5 - M_8$ are biased at currents $I_{\rm biasp}/2$ and $I_{\rm biasp}/8$, respectively. Exact matching of the differential pairs was not a consideration in transistor sizing, since the amplifier offset along with the dc signal component is removed by the highpass filter surrounding the amplifier [12]. The maximum bandwidth is achieved by setting $I_{\rm biasp}$ to 8 μA. To maximize the gain, input transistors of both stages M_1, M_2 and M_5, M_6 are sized with large W/L to operate in the subthreshold region with this maximum bias current. The amplifier's unity-gain frequency f_u is given by $g_{m1}/2\pi C_c$ where C_c is 15 pF for a maximum f_u of 800 kHz.

A decrease in $I_{\rm biasp}$ results in a decrease in the unity gain frequency and hence the bandwidth of the amplifier while maintaining the input transistors in the subthreshold region. The additional transistors M_9 and M_{10} cancel the zero in the right hand plane of the frequency response. The amplifier was designed for a phase margin of 62°.

Common mode feedback circuitry (CMFB) was implemented in each stage in order to control the output levels independently. Circuit schematics for CMFB1 and CMFB2 are shown in Fig. 2. CMFB1 is designed to operate in the subthreshold region in order to minimize power consumption. The forward gain of the CMFB1 is also small enough not to cause instability in the amplifier. Since $M_{11} - M_{13}$ are in subthreshold

$$V_{cm1} = \max(V_{om}, V_{op}). \tag{1}$$

CMFB2 implements standard common-mode feedback circuitry [28]. The input transistors $M_{14} - M_{17}$ are sized with long geometry to maximize the operational linear range of the feedback circuitry.

Analysis of the input-referred thermal noise of this circuit results in:

$$\overline{v_n^2} = \frac{16kT}{3}\frac{1}{g_{m1}}\left(1 + \frac{g_{m3}}{g_{m1}} + \frac{g_{m5}+g_{m7}}{g_{m1}g_{m5}^2(r_{o1}||r_{o3})^2}\right)\Delta f \tag{2}$$

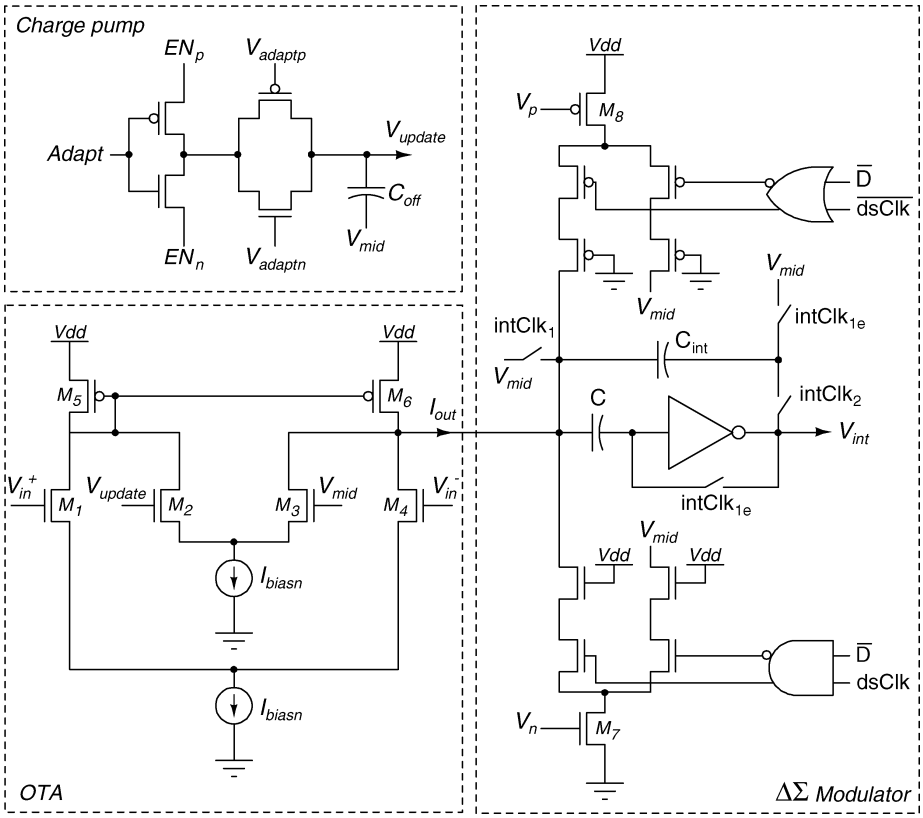

Fig. 3. Circuit schematic of the continuous-time Gm-C incremental $\Delta\Sigma$ ADC, including adaptive offset cancelation.

where k is the Boltzman constant, T is the absolute temperature, and Δf is the bandwidth. The first two terms in the right-hand side of (2), proportional to $1+g_{m3}/g_{m1}$, represent noise contributions from the first stage transistors, while the third term originates from the second stage. Since the third term is negligible, the bias current of the second stage was chosen to be smaller (1/8) than that of the first stage in order to conserve power while maintaining low noise operation. Also, $1/g_{m1}$ and g_{m3}/g_{m1} were kept small to minimize the input-referred noise, by sizing the input transistors to operate in the subthreshold region, maximizing their g_m/I_D ratio. Transistor pairs M_1-M_2 and M_5-M_6 are sized very wide (216 μ/1.8 μ and 18 μ/1.8 μ, respectively) while M_3-M_4 and M_7-M_8 are sized very long (3.6 μ/27 μ and 3.6 μ/7.2 μ, respectively). A decrease in $I_{\rm biasp}$ results in higher thermal noise levels at a smaller bandwidth. Correspondingly, the total noise power, integrated over frequency, remains approximately constant. A decrease in $V_{\rm hpf}$ reduces the resistance and thus the thermal noise from the pseudo-resistor element, and also decreases the 1/f noise since it is filtered out to greater extent at higher low-end (highpass) cut-off frequency.

B. Continuous-time Gm-C Incremental $\Delta\Sigma$

A dedicated ADC is provided for each channel, in order to bypass the need for multiplexing the amplifier outputs to a high speed ADC, thereby reducing the complexity and power consumption of the system. Fig. 3 shows the circuit schematic of the ADC. In order to digitize the differential output voltage of the amplifier, the amplified signals are first converted to a single ended current using a nMOS differential pair OTA which also removes any remaining common mode signal. At the beginning of each conversion cycle, the output node the OTA is set to $V_{\rm mid}$ $({\rm int}Clk_1)$, the other plate of $C_{\rm int}$ is set to $V_{\rm mid}$ $({\rm int}Clk_1)$ and the high gain inverting amplifier is reset $({\rm int}Clk_{1e})$. During the conversion cycle $({\rm int}Clk_2)$ the input current is integrated on capacitor $C_{\rm int}$, changing $V_{\rm int}$. Each period of the $dsClk$, $V_{\rm int}$ is compared to $V_{\rm mid}$ and a decision (**D**) is made. The comparator is implemented using a correlated double sampling scheme (CDS) to reduce the dominant 1/f noise. The decision bit and the clock signal $dsClk$ control the time modulation feedback circuit which contributes either $\{+I_{\rm ref}, -I_{\rm ref}$ or $0\}$ to the input current. The digital gain, G, in the ADC is achieved by passing the feedback current for one clock cycle followed by $G-1$ clock cycles of shunting the feedback. The 1.5-bit effective DAC is realized by transistors M_7 and M_8. These transistors are sized large to improve matching of the reference currents across the channels. They are biased to be continuously active, rather than switched, to decrease the effect of charge injection.

In order to compensate for mismatch in the OTA and in the current feedback of the $\Delta\Sigma$ ADC, a second OTA pair is provided at the voltage-to-current conversion stage. The MSB from the decimator adjusts the direction of the offset current through an integrator implemented by charge pump CP and capacitor $C_{\rm off}$, once every conversion cycle. Larger or more frequent updates allows for further filtering of the 1/f noise outside the signal band.

There are two main sources contributing to the noise of the ADC: the DAC quantization noise and the OTA thermal noise. The input-referred noise power from DAC reference can be written as [27]

$$\overline{v_{\mathrm{ref},n}^2} = \frac{1}{g_{m1}^2} \sum_{i=1}^{\mathrm{OSR}-1} \frac{\overline{i_{\mathrm{ref},n}^2}}{G^2 \mathrm{OSR}^2} \tag{3}$$

where OSR is the oversampling ratio of the incremental ADC, the number of cycles required for data conversion. $I_{\mathrm{ref},n}$ can be written as

$$\overline{i_{\mathrm{ref},n}^2} = 4kT\frac{2}{3}g_{m7}\Delta f \tag{4}$$

For the OTA, the input-referred noise power can be written as

$$\overline{v_{\mathrm{OTA},n}^2} = \frac{16}{3}kT\frac{1}{g_{m1}}\left(1+\frac{g_{m5}}{g_{m1}}\right)\Delta f. \tag{5}$$

Thus the total noise at the input of the continuous-time ADC is

$$\begin{aligned}\overline{v_{adc,n}^2} &= \overline{v_{\mathrm{OTA},n}^2} + \overline{v_{\mathrm{ref},n}^2} \\ &\approx \frac{16kT}{3}\frac{1}{g_{m1}}\left(1+\frac{g_{m7}}{2g_{m1}G^2\mathrm{OSR}}\right)\Delta f\end{aligned} \tag{6}$$

The input referred noise of the ADC should be much smaller that the output noise of the amplifier. This can be achieved by increasing g_{m1}. However, the value of g_{m1} should not be chosen too large since that would decrease the operational range of the OTA. $M_1 - M_4$ were sized 3.6 μ/54 μ for a I_{biasn} of 4 μA. An increase in digital gain, G, will result in a G^2-fold decrease in the second term of (6) without a change in the dynamic range of the ADC. The ADC was designed to have a linear range of 250 mV and digital gain was used to reduce the quantization noise.

The time modulation feedback is controlled by $dsClk$. The gain is introduced by programming the duty cycle of $dsClk$. The reference current is integrated only when $dsClk$ is high while the input current is integrated during the whole period of $dsClk$. The duty cycle of $dsClk$ represents the digital gain of the input current with respect to the reference current which can be set anywhere from 1 to 2^{12}. The integration period and the rate of sampling are set by $\mathrm{int}Clk$, which is derived from $dsClk$. The clock signals $\mathrm{int}Clk_1$ and $\mathrm{int}Clk_2$ are nonoverlapping, derived from $\mathrm{int}Clk$. Clock $\mathrm{int}Clk_{1e}$ is a copy of $\mathrm{int}Clk1$ with the rising edge following and the falling edge preceding those of $\mathrm{int}Clk_1$. The ratio of the periods of $dsClk$ and $\mathrm{int}Clk$ determines the oversampling ratio OSR, ranging between 1 and 4096.

III. Experimental Results

The neural interface system was fabricated in a 0.5 μm 3M2P CMOS process through the MOSIS foundry service. The system was designed to run off a 3.3 V supply. The 16 channels occupy 3 mm $\times$ 3 mm of silicon area and consume 1.7 mW of power at the maximum bandwidth and speed. Fig. 4 shows the micrograph of the fabricated chip.

A. Benchtop Characterization

Fig. 5 shows the tunable amplifier's measured frequency response. The amplifier shows a midband gain of 39.6 dB, a maximum high-end cutoff frequency of 8.2 kHz, and a minimum low-end cutoff frequency of 0.2 Hz. The amplifier's bandwidth is adjusted in the 8.2 kHz–140 Hz range by varying I_{biasp} from 8 μA to 100 nA. The high-pass filter cutoff frequency can also be adjusted from 0.2 to 94 Hz by decreasing V_{hpf} from 1.65 to 1.25 V.

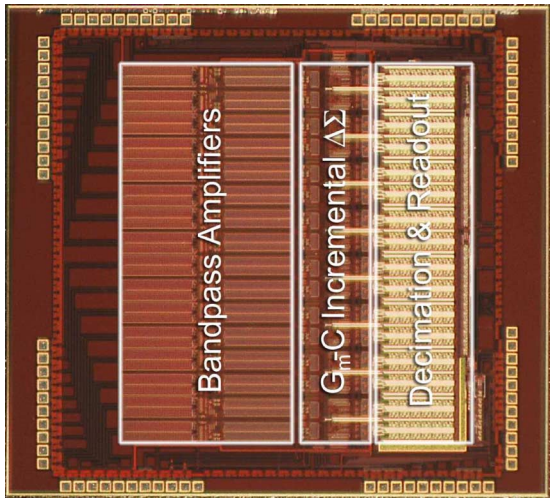

Fig. 4. Micrograph of the fabricated chip. Die size is 3 mm $\times$ 3 mm in 0.5 μm 3M2P CMOS technology.

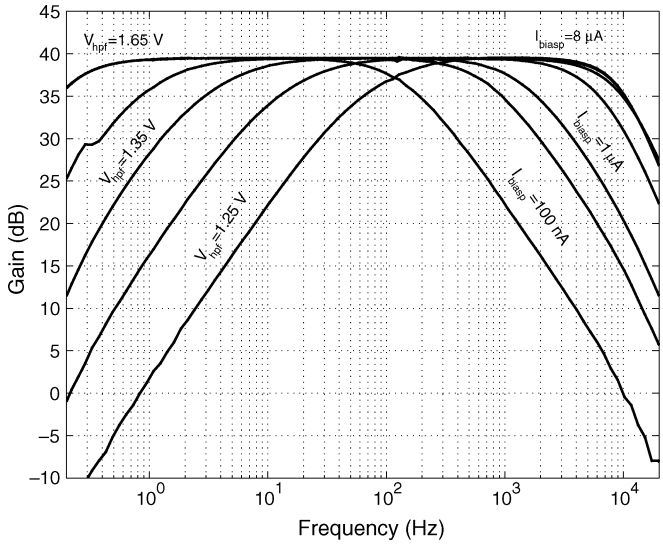

Fig. 5. Filter response for lowpass current bias I_{biasp} between 100 nA and 8 μA, and for highpass voltage bias V_{hpf} between 1.25 and 1.65 V.

Fig. 6 shows the measured output noise power spectral density (PSD) of the amplifier for different I_{biasp} values. For $I_{\mathrm{biasp}} = 8$ μA and $V_{\mathrm{hpf}} = 1.65$ V, the amplifier shows a thermal noise level of 18 $\mathrm{nV}/\sqrt{\mathrm{Hz}}$ and a 1/f corner frequency of approximately 1 kHz. A lower cutoff corner can be accomplished by chopping of the amplifier [20], [21], yielding further decreased noise power at some increase in circuit complexity and power consumption. Integration of the noise power spectral density from 0.5 Hz to 50 kHz, for the amplifier bandwidth setting of 8.2 kHz, gives an input-referred noise of 1.94 μV_{rms}. The noise efficiency factor (NEF) of the amplifier, a compound

measure of noise performance and energy efficiency defined as [29]

$$\mathrm{NEF} = V_{n,\mathrm{rms}}\sqrt{\frac{2I_{\mathrm{total}}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \tag{7}$$

yields 2.9 for the above settings, which compares favorably with NEF values between 3 and 10 reported in the literature (lower is better). As shown in Fig. 6, a decrease in I_{biasp} results in an increase of thermal noise floor of the amplifier and at the same time decreases the 1/f corner frequency and the bandwidth of the amplifier. For $I_{\mathrm{biasp}} = 100\ \mathrm{nA}$ and $V_{\mathrm{hpf}} = 1.65\ \mathrm{V}$, integration of the noise spectral density of the amplifier from 0.5 Hz to 5 kHz for a bandwidth setting of 140 Hz yields an input referred noise of 1.65 μV_{rms}, and an NEF of 3.2. Fig. 7 compares the NEF of the amplifier of this work to that of previous designs [8]–[12], [14], [19]–[21]. As can be seen, the amplifier in this work compares favorably both at high and low bandwidth settings. The amplifier has a common-mode rejection ratio (CMRR) of more than 76 dB for signals between 1 Hz and 10 kHz and an electrode offset of 50 mV. Power supply rejection ratio (PSRR) also measures above 70 dB for the same signal range. The amplifier's measured total harmonic distortion (THD) is below 1% for signals as large as 9.4 $\mathrm{m}V_{pp}$ yielding in a dynamic range of 70 dB.

Fig. 8 shows the signal to noise-distortion ratio (SNDR) for the ADC operated at an oversampling rate $\mathrm{OSR} = 2^{10}$, and at gain settings $G = 1$ and $G = 2$. As shown, an increase in G results in improved performance of the ADC. This improvement owes to reduced switch injection noise with larger gain modulation (lower duty cycle of current feedback) [27]. For typical lower signal levels where the quantization noise is dominant, the SNDR increases by 3.5 dB with the two-fold increase in G. For large signal levels near the limit of the range, the SNDR saturates to 55 dB, limited by harmonic distortion. The integral nonlinearity INL (differential nonlinearity DNL) of the ADC also decreases from 3 LSB (2.5 LSB)) for $G = 1$ and $\mathrm{OSR} = 2^{12}$, to 1.5 LSB (1 LSB) for $G = 4$ and $\mathrm{OSR} = 2^{10}$. Improvements in INL and DNL can be obtained by further increasing the digital gain G, at the expense of lower bandwidth.

Fig. 9 shows the power spectrum of the recorded digital output of one channel with a 1 $\mathrm{m}V_{pp}$ 50 Hz sine wave presented to the frontend amplifier input. The ADC was set for 10-bit resolution and $G = 1$. The resulting digital output showed a THD of 0.3%. The output channel noise is 0.9 LSB (2.5 μV_{rms}) for these settings. ADC thermal noise and quantization noise contribute to this increased noise level with respect to the amplifier noise. Lower quantization noise levels can be attained by higher gain settings G for smaller signal amplitudes.

B. In-vivo Experiments

Spike recording was performed on 250 gram male Sprague-Dawley rats using a protocol approved by the Johns Hopkins Animal Care and Use Committee. Fig. 10 illustrates the experimental setup, and shows spike data from an anesthetized rat somatosensory cortex recorded on the system using a 1 $\mathrm{M}\Omega$ tungsten electrode (FHC, ME). No significant difference was observed in comparison with similar recordings with a commercial acquisition device (Tucker Davis Technologies, FL). The system was also evaluated for recording of EEG signals from a human subject. The male subject was fitted with a 20-electrode cap with gel-based electrodes (Electro-Cap, OH) and the

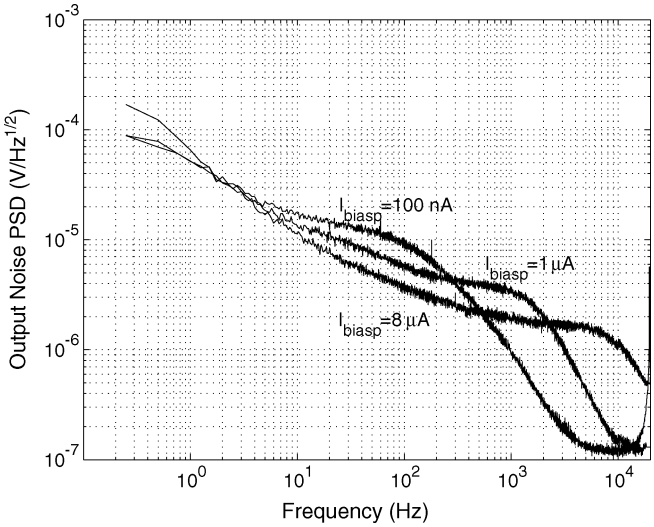

Fig. 6. Measured output noise density of the amplifier for different bias I_{biasp}.

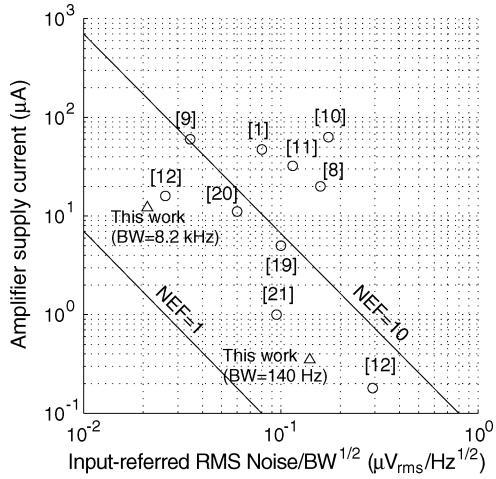

Fig. 7. Comparison of NEF between the presented amplifier (at two bandwidth settings, BW) and other designs in the literature.

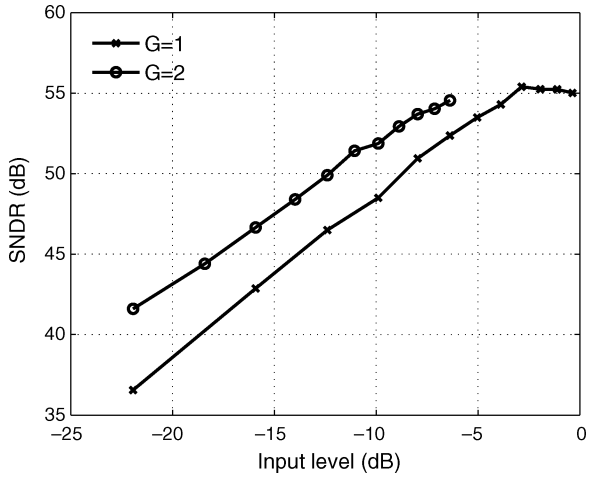

Fig. 8. Measured SNDR of the ADC for $G = 1$, and $\mathrm{OSR} = 10$. Input level is relative to full scale (125 mV_p sine wave input to the ADC).

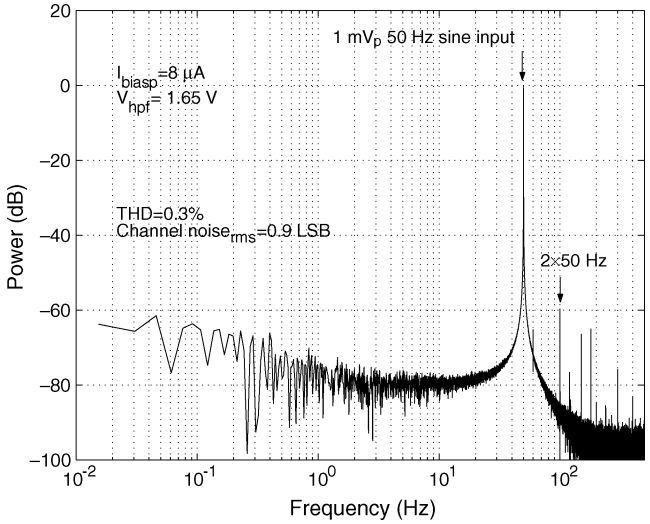

Fig. 9. Normalized power spectrum of digital output for 1 mV_p 50 Hz sine input to the frontend amplifier.

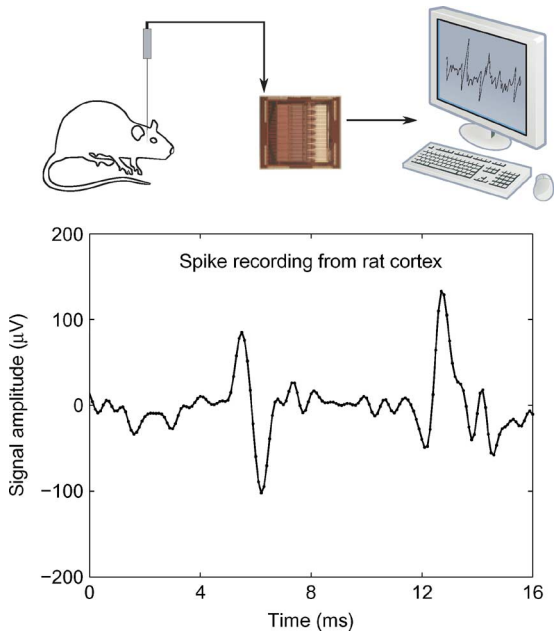

Fig. 10. *In-vivo* neural signal recording. Spikes were recorded from rat somatosensory cortex using a tungsten electrode. A screw electrode was used as signal ground.

O1 electrode was connected to the biopotential ADC, sampling the signal at 250 Hz and digitizing the resulting data to 10-bit. Fig. 11 shows the power spectrum of the recorded signal, obtained when the subject closed the eyes. The resulting peak at 11 Hz in the spectrum clearly reveals recorded α-wave brain activity which is typical in the absence of visual stimulus [7]. A fragment of the raw recorded EEG waveform is also shown as an inset in the figure.

IV. Discussion and Conclusion

The presented neural interface system addresses an emerging need, both in biomedicine and systems neuroscience, for simultaneous recording of various modalities of neural signals including EEG, ECoG, LFP, and spikes. There has been con-

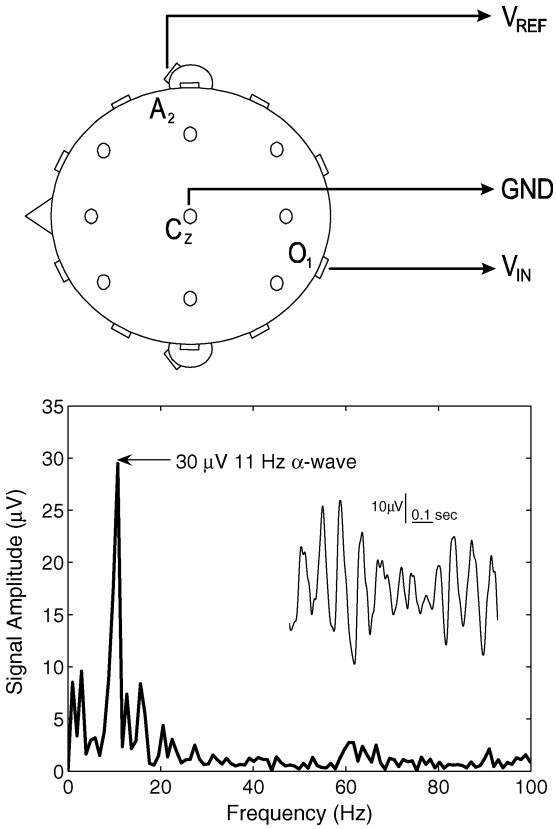

Fig. 11. Experimental setup for EEG recording and recorded waveform from occipital lobe, with the subject's eyes closed, showing alpha wave activity.

siderable effort to make use of the different signal modalities to decode movement or movement intention [30]–[35]. For instance, Hochberg *et al.* [36] demonstrated control of a prosthetic device using an ensemble of neuronal activity recorded from the primary motor cortex. Scherberger *et al.* [37] reported that LFPs can be used to predict behavioral state. The flexibility of recording these different signal modalities within the same neural interface hardware has been lacking in today's integrated recording microsystems.

In this paper we presented a 16-channel 3 mm $\times$ 3 mm neural acquisition system-on-chip, fabricated in 0.5 μm CMOS technology, capable of recording neural signals of various amplitudes and frequencies. Tunable filters were embedded in the amplifier front-end stage in order to selectively amplify the signal of interest. A two-stage voltage amplifier design with reduced current levels in the output stage, significantly lowered the current consumption of the front-end circuit, without affecting noise performance. The amplifier input referred noise across the frequency range is below 2 $\mu V_{\rm rms}$. For EEG signals at the lowest bandwidth setting of 140 Hz, each channel consumes 22 μA of current. For spike signals at the highest 8.2 kHz bandwidth setting, each channel consumes 35 μA of current.

The gain-modulated incremental ADC in each channel provides additional control over signal quantization, that can be tailored to the signal of interest. Higher digital gain in the ADC stage provides higher signal amplification and lower quantization noise, at the expense of signal bandwidth. The individually configurable gain/resolution setting for each channel allows

TABLE I
CHIP SUMMARY AND MEASURED CHARACTERISTICS

Technology	AMI 0.5 μm 2P3M CMOS	
Power Supply	3.3 V	
Amplifier	$A_v = 39.6\ dB$	
Lowpass cutoff	$140 - 8.2\ kHz$	
Highpass cutoff	$0.2 - 94\ Hz$	
Bandwidth	$8.2\ kHz$	$140\ Hz$
I_{biasp}	$8\ \mu A$	$100\ nA$
Input-referred noise	$1.94\ \mu V_{rms}$	$1.65\ \mu V_{rms}$
NEF	2.9	3.2
CMRR	$> 76\ dB\ (1Hz - 10kHz)$	
PSRR	$> 70\ dB\ (1Hz - 10kHz)$	
ADC		
Digital gain	$1 - 4096$	
Sampling rate	$\leq\ 16\ kS/s$	$\leq\ 500\ S/s$
Resolution	$7b$	$12b$
Supply current	$\leq\ 23\ \mu A$	$\leq\ 23\ \mu A$
Channel Total		
THD	$\leq\ 1\%\ (V_{in} \leq\ 10\ mV_{pp})$	
Output noise	$< 1\ LSB$	
Chip Total	16 channels	
Power consumption (maximum)	$1.8\ mW$	
Die size	3mm $\times$ 3mm	

optimum quantization based on the dynamic range and the frequency content of each signal of interest. The flexibility in bandwidth, gain and quantization allows the system to acquire various neural signals as selected in software, rather than by physical modification of the hardware.

Despite the necessary tradeoffs in the design to accommodate the wide operating range of neural signals of interest, the system offers approximately constant noise efficiency factor (NEF $\approx$ 3) across the entire frequency range, where noise power density and power consumption scale with the bandwidth setting, through adjustments of bias levels in the amplifier and gain/resolution settings in the ADC. This scaling is advantageous to the different requirements for acquisition of different types of neural signals across the spectrum. As shown in Fig. 6, for high current bias ($I_{\mathrm{biasp}} = 8\ \mu$A), the thermal noise level and 1/f noise corner are at acceptable levels for spike recording which requires higher voltage scale ($\approx$1 mV) and hence affords higher noise at high bandwidth setting ($\approx$1 kHz). At the other end of the spectrum of neural signals, the low bandwidth setting ($\approx$100 Hz) required for EEG acquisition ($I_{\mathrm{biasp}} = 100$ nA) leads to an increase in the thermal noise density, but to a slight decrease in the rms noise because of the compound effect of lower bandwidth and decreased 1/f corner frequency (Fig. 6). The lower rms noise together with higher ADC resolution (by gain modulation G) afforded by the lower bandwidth setting support increased amplitude resolution as required for EEG signals ($\approx 10\ \mu$V).

Benchtop characterization as well as *in vivo* testing were performed with this system. The recordings were comparable with those made by commercial devices, at significantly lower power consumption and smaller size. Other biopotential signals of interest, across the body, that are within the operating range of the chip include electromyograms (EMG) representative of muscle activity, electrooculograms (EOG) tracking eye motion, and electrocardiograms (ECG) conveying heart activity. For instance, monitoring EMG and EOG activity jointly with scalp EEG offers great improvements in specificity of noninvasive brain-machine interfaces [30], and further allows to compensate for various motion artefacts in reconstructed brain activity [38].

Table I summarizes the measured performance of the chip. To our knowledge, this is the only biopotential recording system reported to date capable of simultaneously acquiring, on a single microchip without external components, a wide range of neural signal modalities ranging from spike action potentials to EEG brain waves, where each channel of recording can be individually configured in-site for the signal of interest. Furthermore, the integrated system-on-chip is suitable for *in vivo* neural instrumentation in an implanted system, offering a digital output that is compatible with VLSI systems for digital telemetry and power harnessing. We expect these two attributes of the neuropotential recording chip to be of great use in understanding the mechanisms underlying brain function and information processing and propagation throughout the brain.

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