

# From Spikes to EEG: Integrated Multichannel and Selective Acquisition of Neuropotentials

Mohsen Mollazadeh, Kartikeya Murari, Gert Cauwenberghs, Nitish Thakor

**Abstract**—Electrical signals recorded from the brain cover a wide range of amplitudes, frequencies, and spatial scales, from spikes and local field potentials (LFP) inside the brain to electrocorticograms (ECoG) and electroencephalograms (EEG) outside. Each of these signal modalities represent different aspects of neural dynamics that can be combined to infer brain state and function in a broader context. We present a 16-channel interface circuit fabricated in a  $0.5\ \mu\text{m}$  CMOS process for the selective acquisition and digitization of any of the modalities. Each channel features a fixed gain bandpass amplifier with a tunable frequency response which allows isolation of the signal of interest without hardware modification and a programmable gain/resolution analog to digital converter (ADC). The bandpass amplifier analog front end has an input referred noise of  $1.94\ \mu\text{V}_{\text{rms}}$  for a bandwidth of 8.2 kHz while drawing  $12.2\ \mu\text{A}$  of current from a 3.3 V supply. Experimental recordings with the system show spike signals in rat somatosensory cortex as well as alpha EEG activity in a human subject.

## I. INTRODUCTION

Information processing and transmission in the central nervous system is mostly through electrical signals. These signals are generated by individual neurons as action potentials. The single unit activities can be recorded using a microelectrode which is placed very close to the neuron. As the recording site moves away from a single source and becomes larger, it captures the electrical activity from multiple sources in the brain. Due to volume conduction, high frequency components of the spiking activity are filtered out and a broader representation of the ongoing brain activity is produced. Each signal has advantages and limitations and can be used to understand the basic mechanisms underlying various brain function as well as in applications such as neuroprosthetics [1]–[6].

As it can be seen in Table I, different neural modalities are spread out over a wide range of frequencies and amplitudes; from  $\mu\text{V}$  to  $\text{mV}$  and from Hz to kHz. An interface circuit that can acquire and, on demand, isolate desired signals among all the modalities offers obvious advantages over one that is tailored to any individual signal. While the design can be made flexible to accommodate the different signals, it needs to maintain low-noise and low-power performance over all the ranges of operation. Also, any interface circuit should be able to acquire the low frequency content of the signal of interest while rejecting the large DC offset resulting from the electrode tissue interface.

M. Mollazadeh, K. Murari and N. Thakor are with the Biomedical Engineering Department, Johns Hopkins University, Baltimore, MD, USA. email: mohsenm@jhu.edu.

G. Cauwenberghs is with the Division of Biological Sciences, University of California San Diego, La Jolla, CA, USA. email: gert@ucsd.edu.

TABLE I  
AMPLITUDE AND FREQUENCY RANGES OF THE DIFFERENT MODALITIES  
OF ELECTRICAL SIGNALS FROM THE BRAIN [7]

| Signal | Location and description   | Amplitude and Frequency                           |
|--------|--|---|
| Spike  | Extracellular recordings from single neurons inside the cortex using a single electrode or a microelectrode array. | $500\ \mu\text{V}$<br>0.1-7 kHz                   |
| LFP    | Collective activity from several neurons inside the cortex.  | $< 1\ \text{mV}$<br>$< 200\ \text{Hz}$            |
| ECoG   | Activity recorded from disk electrodes on the surface of the brain.  | $0.01\text{-}5\ \text{mV}$<br>$< 200\ \text{Hz}$  |
| EEG    | Non-invasive recording of electrical activity from the scalp.  | $5\text{-}300\ \mu\text{V}$<br>$< 100\ \text{Hz}$ |

Over the years, several VLSI systems have been developed [8]–[18] to meet the requirements of acquiring neural signals. Typically the range of frequencies covered by any one of these systems is limited to one or two signal modalities, to accommodate high efficiency for that targeted application. A low noise neural recording amplifier with a bandwidth of 7.2 kHz was described by Harrison *et al.* [14]. The amplifier had an input-referred noise of  $2.2\ \mu\text{V}_{\text{rms}}$  while consuming  $80\ \mu\text{W}$  from a 5 V supply. A similar amplifier, but with hardware modifications, for acquiring EEG signals was also presented in the same work. The EEG amplifier had a bandwidth of 30 Hz and power dissipation of  $0.9\ \mu\text{W}$  while maintaining low input-referred noise. Yazicioglu *et al.* [16] reported a biopotential acquisition amplifier with a  $57\ \text{nV}/\sqrt{\text{Hz}}$  input-referred voltage noise density and  $60\ \mu\text{W}$  power consumption. The low noise figure was achieved using chopper stabilization technique and external components. Recently, Perelman *et al.* [17] showed on-chip amplification and separation of spikes from LFPs. The amplifier draws  $75\ \mu\text{A}$  from the supply for an input-referred noise of  $3\ \mu\text{V}$ .

Here, we present a 16 channel integrated acquisition system with adjustable filtering, amplification and digitization covering the entire spectrum of neural signals. The system was fabricated in a  $0.5\ \mu\text{m}$  2 poly, 3 metal CMOS process and offered low-noise and low-power performance over the entire range of settings. Results from *in vivo* testing are also presented.

## II. SYSTEM ARCHITECTURE

Fig. 1 shows the micrograph of the fabricated chip and the functional diagram for one of 16 channels. Each channel comprises of a fully differential bandpass filtering two-

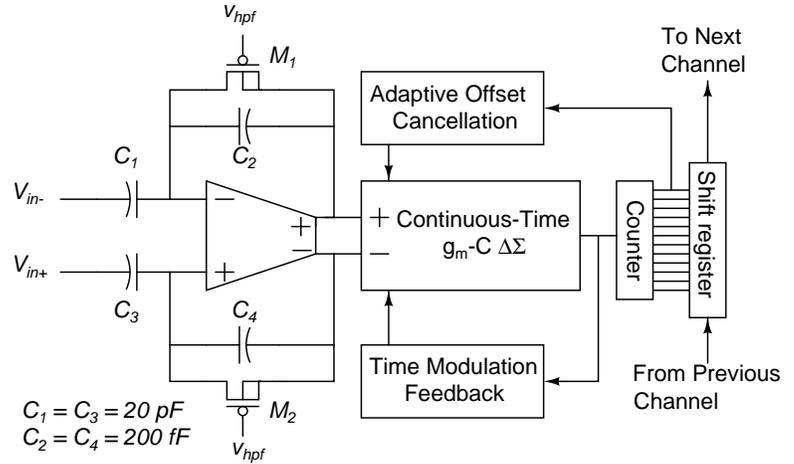
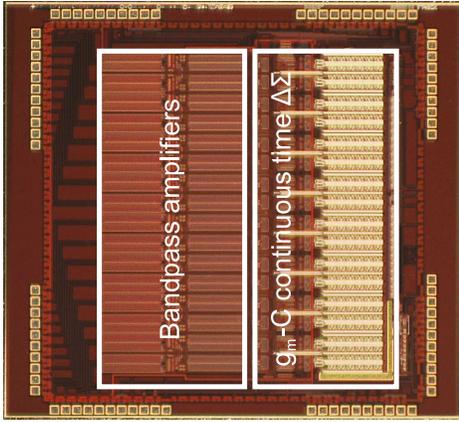


Fig. 1. Micrograph of the fabricated chip (left) and a functional block diagram of one of the 16 channels (right).

stage voltage amplifier, a Gm-C incremental  $\Delta\Sigma$  ADC, a decimating counter, and a daisy-chained parallel-to-serial output register. The amplifier midband gain is set to 40 dB by ratioed poly1/poly2 capacitors ( $C_1=C_3=20 \text{ pF}$  and  $C_2=C_4=200 \text{ fF}$ ). The PMOS transistors  $M_1$  and  $M_2$  in the feedback loop provide a large resistance in the  $G\Omega$  range for sub-Hz cutoff highpass filtering [14]. This cutoff frequency can be adjusted by changing  $V_{hpf}$  which in turn changes the resistance of  $M_1$  and  $M_2$ . The low pass filter cutoff frequency can be tuned for various modalities of neural signals by changing the  $g_m$  of the front-end amplifier which results in a change in its unity gain frequency,  $f_u$ .

The differential output of the amplifier is digitized using a continuous time Gm-C, incremental  $\Delta\Sigma$  ADC. Each channel has a dedicated ADC to decrease the operational frequency and thus the net power consumption. The front end of the ADC consists of an operational transconductance amplifier (OTA) which converts the differential voltage output of the amplifier to a current. This current is then compared to the reference current of the ADC and a decision is made [19]. The ADC incorporates a time modulation feedback which allows a digitally programmable gain between 1 and 4096. The structure also allows configuration of the ADC resolution. Both, ADC gain and resolution, are traded off with conversion rate *i.e.* spikes can be acquired at 16 kS/s with 7 bit resolution and digital gain of one whereas the slower and weaker EEG signals can be acquired at 500 S/s with 12 bit resolution with a digital gain of four. In order to remove any offset in the ADC output caused by mismatch in the ADC stage, a charge pump based circuit adaptively adds or subtracts a small current from the OTA based on the output of the ADC.

The decimator circuitry is implemented as a simple accumulate-and-dump circuit with the counter counting the number of  $\Delta\Sigma$  modulator decision bits that are high during a conversion cycle. At the end of the cycle, the number is shifted into a parallel-in serial-out shift register and the modulator is reset. The output registers for the channels are

daisy-chained and read out asynchronously in a bit-serial fashion.

### III. EXPERIMENTAL RESULTS

The neural interface system was fabricated in a  $0.5 \mu\text{m}$  3M2P CMOS process through the MOSIS foundry service. The system was designed to run off a 3.3 V supply. The 16 channels occupy  $3 \text{ mm} \times 3 \text{ mm}$  of silicon area and consume 1.8 mW of power at the maximum bandwidth and speed (8.2 kHz and 16 kS/s). The front end amplifier was characterized independent of the ADC using a lock-in amplifier (Signal Recovery, Oak Ridge, TN). For characterizing the system and *in vivo* recordings, the digital output of the chip was acquired using a DAQ card (National Instruments, Austin, TX) and read into a computer.

#### A. Chip characterization

Fig. 2 shows the magnitude and phase responses of the amplifier at its maximum and minimum bandwidths. The amplifier had a measured midband gain of 39.6 dB. For Fig. 2a the low pass and high pass cutoff frequencies were set to 0.2 Hz and 8.2 kHz respectively. At these settings, the amplifier consumed  $40 \mu\text{W}$  with an input referred noise of  $1.94 \mu\text{V}_{rms}$ . This results in a noise efficiency factor (NEF)<sup>1</sup> [20] of 2.9. In Fig. 2b the low pass and high pass cutoff frequencies were set to 0.2 Hz and 140 Hz. At these settings, the amplifier consumed  $1.1 \mu\text{W}$  with an input referred noise of  $1.65 \mu\text{V}_{rms}$  yielding an NEF of 3.2. The amplifier's CMRR and PSRR were greater than 76 dB (0.1 Hz-10 kHz). The total harmonic distortion (THD) was less than 1% for signals smaller than  $9.4 \text{ mV}_{pp}$ .

Fig. 3 shows the power spectrum of the recorded digital output of one channel with a  $1 \text{ mV}_{pp}$  50 Hz sine wave presented to the frontend amplifier input. The data indicate

<sup>1</sup>NEF is a measure of noise power density per unit power dissipation. NEF is defined as  $V_{n,rms} \sqrt{\frac{2I_{total}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \cdot V_{n,rms}$ ,  $I_{total}$  and BW are amplifier's input-referred noise, current consumption and bandwidth respectively

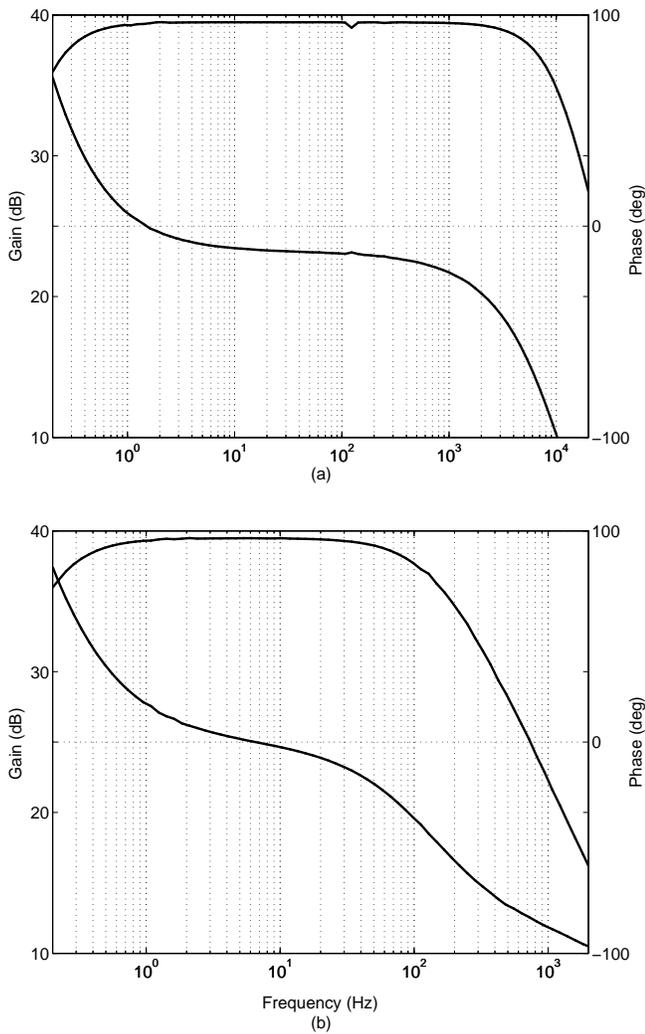


Fig. 2. Magnitude and phase response of the amplifier at the (a) maximum and (b) minimum bandwidths.

a THD of 0.3%, and a digital output noise of 0.9 LSB. OTA thermal noise and ADC quantization noise contribute to this increased noise level. Lower quantization noise levels can be attained by higher gain setting for smaller signal amplitudes.

### B. in vivo recordings

Spike recordings were performed in the somatosensory cortex of 200-250 gram male Sprague-Dawley rats using a protocol approved by the Johns Hopkins Animal Care and Use Committee. The rat was fixed in a stereotactic frame (David Kopf Inst., Tujunga, CA) and a window was opened above the somatosensory cortex. A  $1\text{ M}\Omega$  tungsten electrode (FHC, Bowdoin, ME) was mounted on a micromanipulator and connected to a commercial acquisition device (Tucker Davis Technologies, Alachua, FL). The electrode was moved to obtain spike activity from the somatosensory cortex. Once the electrode was in position, it was connected to the neural interface circuit. The recordings were comparable to the commercial device. One spike was manually isolated offline and template matching with Euclidean distance was

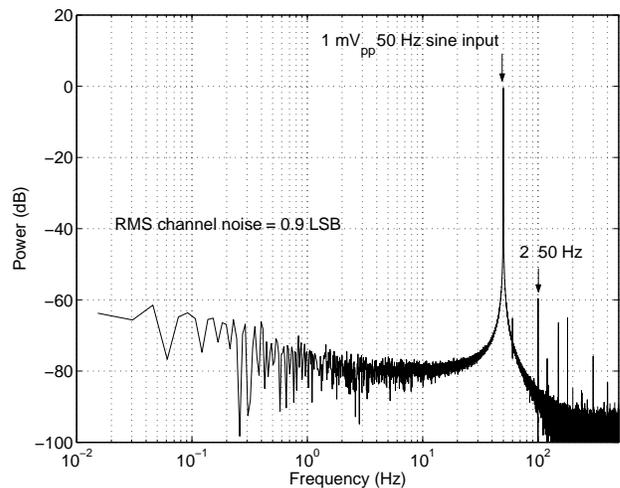


Fig. 3. Power spectrum of the digital output of the system with a 50 Hz  $1\text{ mV}_{pp}$  sinusoidal wave presented to the input.

performed to identify spikes over the entire recording. Fig. 4 shows forty time-aligned spikes from a single unit during the recording.

EEG recordings were performed on a male human subject fitted with a 20-electrode cap with gel-based electrodes (Electro-Cap, Eaton, OH). The O1 electrode located above the occipital lobe was connected to the interface circuit and the person was asked to periodically open and close his eyes for 30 s intervals. The  $\alpha$  activity in the EEG which is centered around 11 Hz is known to increase when the eyes are closed [7]. Fig. 5 shows the power spectral density of the recorded waveform in both states. As it can be seen, 11 Hz  $\alpha$  activity is present during eye closure.

## IV. CONCLUSIONS

We have presented a fully integrated multichannel neural acquisition system capable of recording a variety of neural

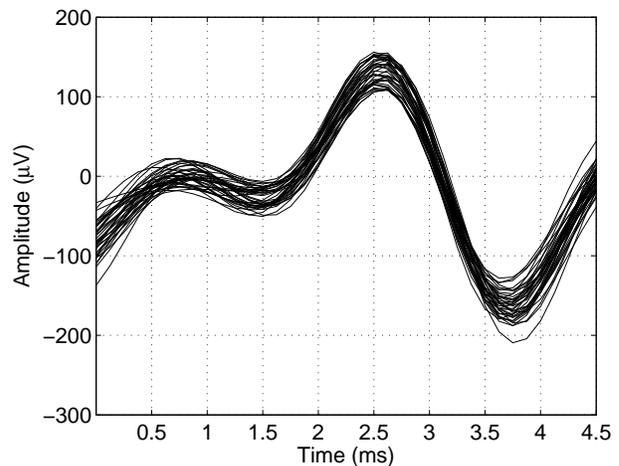


Fig. 4. Forty time aligned spikes recorded from the somatosensory cortex of a rat using the interface circuit. Spike sorting was done off-chip and offline.

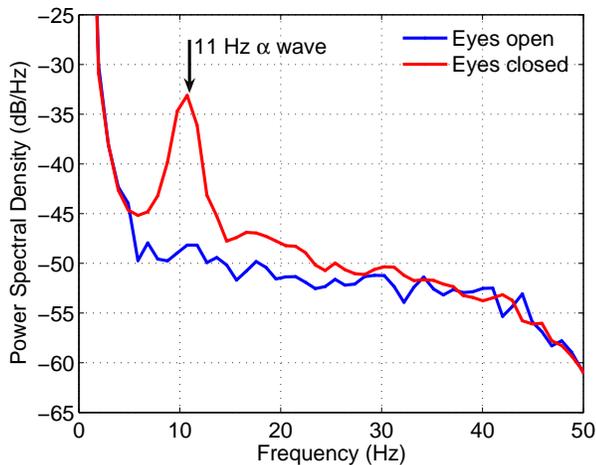


Fig. 5. Power spectral density of the recorded EEG while the subject eyes are open (blue trace) and closed (red trace). The 11 Hz  $\alpha$  wave is present during eye closure.

signals from spikes to EEG. The front-end amplifier had a fixed gain of 40 dB and incorporated a tunable filter for selective recording of neural biopotentials. The amplifier input referred noise for all bandwidth settings upto 8.2 kHz was below  $2 \mu V_{rms}$  resulting in a very low noise performance suitable for recording all neural biopotentials. The continuous time ADC in each channel provided additional control on signal amplification and quantization. The configurable resolution setting allows the optimum quantization based on the dynamic range and the frequency content of the signal of interest. The flexibility in bandwidth, gain and quantization allows the system to acquire various neural signals without any modifications in the hardware. The measured performance of the chip is summarized in Table II. The chip was used to acquire spikes from a rat as well as EEG from a human subject. Future work includes packaging and integration of the chip with electrode array for an implantable neural monitoring system.

#### V. ACKNOWLEDGEMENTS

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TABLE II

PERFORMANCE SUMMARY OF THE 16-CHANNEL NEUROPOTENTIAL ACQUISITION SYSTEM

|  |             |         |
|--|-------------|---------|
| Fixed gain   | 39.6        | dB      |
| Programmable gain                                      | 1-4096      |         |
| Lowpass cutoff   | 0.140 - 8.2 | kHz     |
| Highpass cutoff  | 0.2 - 94    | Hz      |
| Channel analog power (BW = 8.2 kHz)                    | 40.3        | $\mu W$ |
| Channel analog power (BW = 140 Hz)                     | 1.2         | $\mu W$ |
| ADC speed  | $\leq 16$   | kS/s    |
| ADC resolution   | $\leq 12$   | bits    |
| Total harmonic distortion ( $v_{in} \leq 9.4mV_{pp}$ ) | $\leq 1\%$  |         |
| Channel noise  | $\leq 1$    | LSB     |
| Chip power (maximum BW and speed)                      | 1.8         | mW      |

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