INTEGRATED 64-STATE PARALLEL ANALOG VITERBI DECODER

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ABSTRACT

We present a mixed-signal VLSI architecture for state-parallel analog Viterbi decoding, including an analog Add-Compare-Select (ACS) module and a digital survivor path memory (PM) module. A single-chip 64-state analog Viterbi decoder for $K = 7$ convolutional code has been implemented in $3.3V$ $0.5\mu m$ CMOS technology. The chip measures $5.05 \times 2.54mm^2$, and achieves a decoding speed of $40Mb/s$ ($20MHz$ clock) at $50mW$ power consumption as verified by post-layout transistor-level simulation. In addition, a behavioral model accounting for inaccuracies in the analog implementation is developed to simulate the bit error rate (BER) vs. signal-to-noise (SNR) performance, confirming superior error correction (coding gain) of the mixed-signal design over hard-decision and 3-bit soft-decision digital implementations.

1. INTRODUCTION

Convolutional coding and Viterbi decoding present a powerful Forward-Error-Correction (FEC) channel coding for digital communications, widely used in space, satellite, CDMA, Digital PCS and DVB systems. The need for efficient, low-power implementation of the Viterbi decoding algorithm prompts a study of alternative, mixed-mode VLSI solutions. [1]

In a previous paper [2] we presented the first analog VLSI implementation of the Add-Compare-Select (ACS) functional block as part of a long constraint length ($K = 7$) Viterbi decoder. In this work, we present a fully integrated, mixed-signal, Viterbi decoder including a digital Path Memory (PM) module. By integrating both ACS and PM modules on a single chip and and with an improved switched-capacitor implementation of the branch metric in the ACS module, we attain high-speed operation with a decoding rate up to $40Mb/s$. The chip has been implemented in $0.5\mu m$ CMOS technology, and the design is verified through post-layout transistor-level as well as behavioral simulations. To this end, we apply a computational model for analog decoding [5] that accounts for noise and imprecision in the analog implementation, quantified in terms of parameters extracted from the design.

2. ANALOG VITERBI DECODING

In a digital communication system, the communication channel is inherently analog, since modulation, transmission, and demodulation occur in the analog domain. This implies that the transmitted digital sequence at the sender is received as an analog sequence at the decoder. There are thus two important reasons to consider analog decoding, *i.e.*, perform decoding computations in the analog domain. First, analog decoding has (in theory) the best performance (BER vs. SNR performance) because conversion from analog to digital format introduces quantization noise which causes performance loss. Second, analog VLSI implementation is in general more area and energy efficient than digital implementations, since fewer transistors are needed to implement the same functions, and since high-speed A/D conversion is avoided.

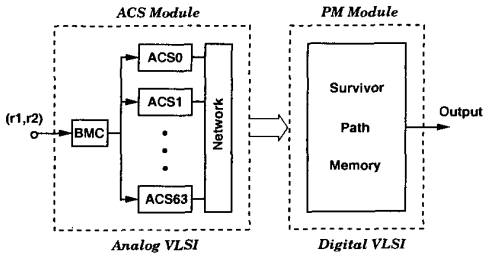

Figure 1: *Viterbi decoder architecture for rate $R = 1/2$, length $K = 7$ convolutional code.*

Different architectures are available to design a Viterbi decoder in VLSI. The most often adopted architecture in practical systems is the memory-based Viterbi decoder architecture, which has two functional blocks: Add-Compare-Select (ACS) and Survivor Path Memory (PM). For high-speed operation, a state-parallel architecture is used for the ACS module, and a trace-back architecture for the PM yields lowest power dissipation.

3. MIXED-MODE VLSI DECODER ARCHITECTURE

For the implemented Viterbi architecture, we chose a rate $= 1/2$, $K = 7$ convolutional code $(171, 133)$, the standard code in digital satellite systems, with 64 states in its trellis. The block diagram of the mixed-signal state-parallel architecture is shown in Figure 1. The ACS module performs the core of the Viterbi algorithm (to prune paths though the trellis), including branch metric calculation, path metric accumulation, and path metric compare and select operations. Since it operates directly on the received analog input, the ACS module is an analog VLSI design. The PM module stores survivor path information and generates the decoded information bits, and thus is best implemented in digital VLSI.

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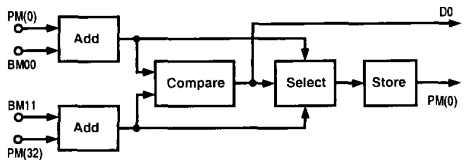

Figure 2: *Block diagram of ACS processor, shown for state 0 (ACS0).*

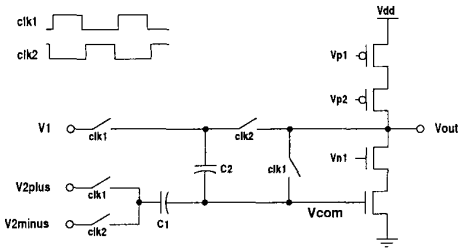

Figure 3: *Branch metric calculation (BMC) adder circuit.*

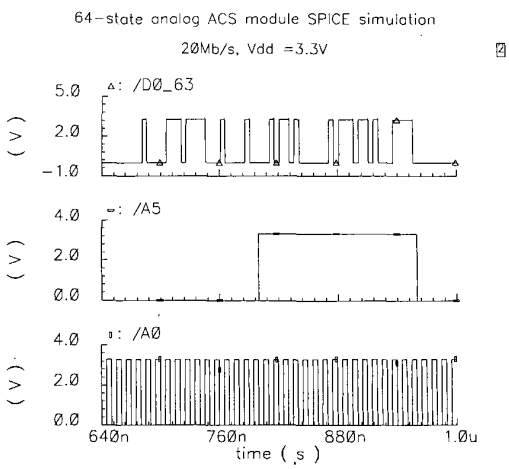

Figure 4: *ACS module SPICE simulation: decision bits D0, D1,..., D63.*

3.1. Add-Compare-Select

The decoder shown in Figure 1 uses a state-parallel ACS architecture. In previous work [2] we have demonstrated a state-parallel architecture with compact and low-power implementation in analog VLSI, the first analog implementation of a large-constraint length (64-state) Viterbi ACS module. The chip measures $2.2 \times 2.25mm^2$ in $2\mu m$ CMOS technology and dissipates $14mW$, a fraction of digital alternatives. The present design includes the PM module on the same chip, and improves on the circuit design of the branch metric calculation (BMC) unit in the ACS module, to yield significantly higher decoding speed.

The circuit block diagram of one ACS processor (ACS0) is shown in Figure 2. All 64 ACS processors are internally identical, and are interconnected according to the 64-state trellis diagram, and corresponding branch metrics. Circuits implementing the compare and select functions, as well as metric renormalization, are identical to the ones presented in [2]. The current-mode implementation of the branch metric calculation and addition are replaced with switched-capacitor circuitry, described next.

The branch metric calculation unit (BMC) generates, in response to the pair of received inputs $(Y1, Y2)$, analog branch metrics corresponding to four types of transitions in the trellis: 00, 01, 10 and 11. The switched-capacitor circuit implementing the 00 branch is shown in Figure 3, calculating $Y1 + Y2$. It is a standard design operating with two nonoverlapping clocks, $clk1$ and $clk2$. The inputs $Y1$ and $Y2$ are presented at the $V1$ and $V2plus$ terminals. $V2minus$ serves as a common-mode offset for proper biasing of the single-ended amplifier, of which the precise value is immaterial. During the $clk1$ phase, $Y1 - Vcom$ and $Y2 - Vcom$ are sampled on two capacitors $C2$ and $C1$. During the $clk2$ phase, charge sharing across $C1$ and $C2$ generates the sum at the output. The other three metrics are generated in similar fashion, and the branch metric addition block is implemented using the same switched-capacitor circuit.

We have conducted SPICE simulation of the netlist extracted from the analog ACS module chip layout, using process parameters supplied for the MOSIS $0.5\mu m$ CMOS process. Figure 4 illustrates the ACS output — the 64-bit decision vector when both inputs $Y1$ and $Y2$ are all-zero sequences at $20MHz$ $(40Mb/s)$. For debugging purposes, the 64 decision bits are scanned out serially, time-multiplexed at a rate synchronous with the system clock. The result shown fully complies with the decoding simulation we conducted in software.

3.2. Survivor Path Memory

To implement the survivor path memory architecture, three types of path memory management schemes are commonly used: register-exchange (RE), trace-back (TB), and RE-TB-combined. The RE approach is suitable for fast decoders, but occupies large silicon real-estate and consumes lots of power. On the other hand, the TB path memory usually consumes less power, but is slower than its RE counterpart, or requires a clock rate higher than the decoding throughput. The RE-TB-combined approach, as described in [3], is a good alternative to the RE approach for high-speed applications.

Since we selected a high-speed Viterbi decoder architecture, and power consumption is a major consideration, we decided to implement a full-speed TB path memory, which can achieve the throughput of RE without the need of a faster clock. A special case of the multi-pointer TB path memory described in [4], the number of read pointers is equal to the trace-back depth. The PM structure is illustrated in Figure 5. Since the write pointer and read pointer move in opposite directions at the full speed of the decoder master clock, the length of the PM is twice the trace-back depth. We implemented a 64-stage path memory, which gives a trace-back depth of 32. The chip layout including branch metrics, ACS and PM, is shown in Figure 6, and chip characteristics are given in Table 1. The chip simulates functional at $40Mb/s$ with a power consumption of $50mW$.

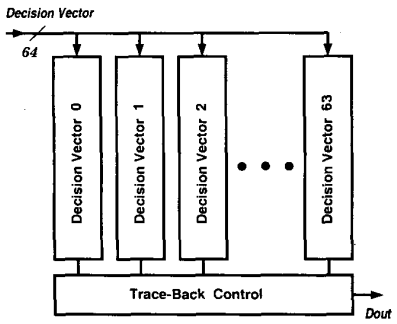

Figure 5: *Full-speed trace-back path metric (PM) architecture.*

Table 1: Chip Characteristics

Technology	$0.5\mu m$, 3-metal CMOS
Convolutional code	$(2, 1, 7)$, rate=$1/2$,$K = 7$
Core size	$5.05mm \times 2.54mm$
Supply voltage	$3.3V$
Decoding Speed	$40Mb/s$ ($20MS/s$ information rate)
Power Consumption	$50mW$

4. BIT ERROR RATE (BER) DECODING PERFORMANCE

4.1. Behavioral Model

Coding theory tells us that unquantized, or analog, Viterbi decoding gives the best performance. On the other hand, an ideal analog decoder achieving the theoretical limit cannot be realized with actual hardware because analog VLSI circuits are subject to imperfection effects, such as noise and nonlinearity. We have previously studied the performance of analog decoding using an analog channel model that includes saturation effects, and accounting for analog imprecision in the implementation of the decoder [5]. We will here apply the same tools to assess the BER vs SNR performance of the decoder chip, in terms of the implementation inaccuracy of the decoder as estimated from process parameters. Random coding simulations are performed to obtain realistic results. Our work

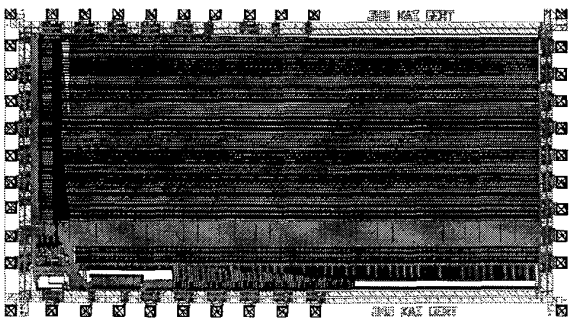

Figure 6: *Layout of the mixed-signal integrated 64-state Viterbi decoder chip.*

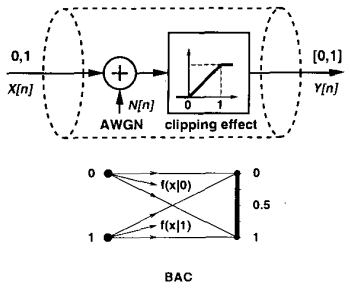

Figure 7: *Binary Analog Channel (BAC) Model.*

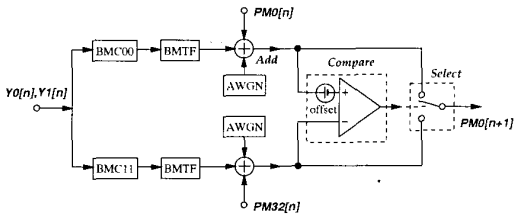

Figure 8: *A practical ACS processor (ACS0) model*

makes use of a new concept in coding theory [5]: the Binary Analog Channel.

4.2. Binary Analog Channel (BAC) Model

To analyze analog decoding, the traditional Binary Symmetric Channel (BSC) model used in coding theory is no longer valid, and an appropriate analog channel model needs to be used instead. An Additive-White-Gaussian-Noise (AWGN) model could be used, although it does not account for saturation effects which bound the amplitude of the analog signal. To account for various physical mechanisms of saturation, which we refer to as the **clipping effect**, we introduced the Binary Analog Channel (BAC) [5], represented schematically in Figure 7. BAC is considered a more accurate to analyze and simulate a coded communication systems.

4.3. Analog Viterbi Decoder ACS Model

By abstracting the essential operations involved in analog Viterbi decoding, based on the circuit we designed, we developed a simple and generic analog Viterbi decoder ACS model, accounting for imprecision in the analog implementation. The model for state-0 ACS processor is shown in Figure 8. The model is generic, and can be applied to analyze other analog Viterbi decoder implementations. We used this model in random coding simulations, in order to assess the bit-error-rate (BER) performance.

Analog circuit imperfections are modeled into three categories. The first accounts for nonlinear effects in the BMC, which is defined by the Branch Metric Transfer Function (BMTF), as shown in Figure 9. The second is circuit noise (mostly thermal noise) in the signal loop, which for simplicity is lumped into two independent AWGN sources in the adders. The third imperfection is the presence of comparator offset, which also lumps together other sources of fabrication mismatch. For a 64-state ACS, the set

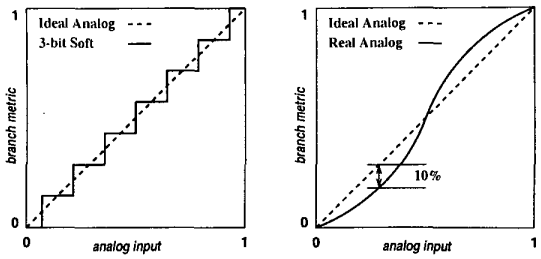

Figure 9: *Illustration of branch metric transfer function (BMTF).*

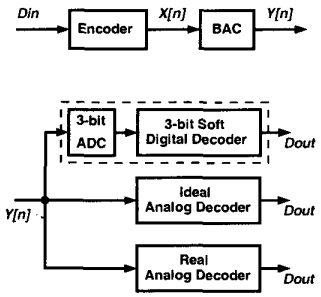

Figure 10: *Benchmark Viterbi decoders used in random coding simulation.*

of parameters in the model comprises 64 comparator offsets, 128 independent AWGN sources, and a BMTF.

4.4. Random Coding Simulation

We used the BAC and analog ACS models to conduct a random coding simulation. Figure 10 illustrates the configuration used to assess the BER performance of three types of Viterbi decoders: ideal analog, real analog, and three-bit soft-decision digital.

A random digital input sequence of length N is sent to the encoder. The encoded sequence (N bits) then goes through the BAC, which adds channel AWGN shaped by the clipping function to yield a sequence of analog values contained in the interval $(0, 1)$. This analog sequence, $Y[n]$, is input to the decoders. The same path memory of length 35 is used in all three decoders.

Three parameters in the analog decoding model are characteristic of the circuit and process used in the implementation, and must be determined from the layout. They are nonlinearity in the BMTF, comparator offset, and the level of (thermal) noise inside the ACS processor. For the implemented analog ACS, nonlinearity in the BMTF mainly comes from the operational amplifier. Based on SPICE simulation of the opamp, nonlinearity as estimated from peak distortion accounts for less than 1 % of the signal range. Comparator offsets are due to fabrication mismatch, and vary for each of the ACS processors. A conservative worst-case offset of $\Delta v = 10\%$ is used. The level of thermal noise in the switched-capacitor circuits is dominated by the size of the capacitors, estimated at 0.2% of the signal range at room temperature.

Figure 11 shows the simulation results for the real analog Viterbi decoder using the extracted parameters, in comparison with the other Viterbi structures. The bit-error-rate curves demonstrate that the implemented analog decoder achieves 3-bit effective de-

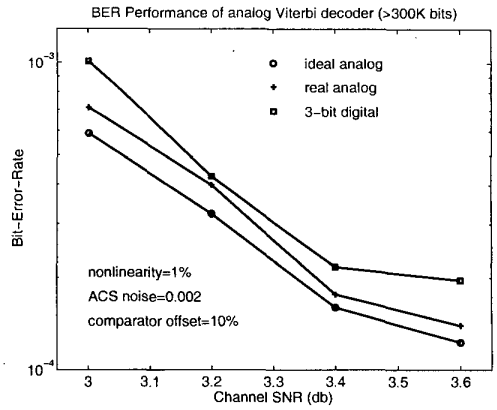

Figure 11: *BER performance of analog and benchmark Viterbi decoders.*

coding resolution or better. In other words, the absence of quantization noise makes up for more than the combined deteriorating effects of analog circuit noise, mismatch and nonlinearity. Since the analog ACS implementation is significantly more compact and energy efficient than a 3-bit digital design, this indeed presents an attractive alternative. (The reason of the flattening of the curves at the highest SNR points is not clear, probably due to changing data size from 300K to 600K.)

The individual effect of each of these sources of error on the coding (BER) performance has been studied in more detail in [5], indicating a wide margin in the admissible range of the parameter values so that a more aggressive analog design is possible.

5. CONCLUSION

We have presented a mixed-signal VLSI architecture for analog Viterbi decoder. A single chip 64-state analog Viterbi decoder chip has been fabricated in a $0.5\mu m$ CMOS process. A systematic random coding simulation method was provided for evaluating BER performance. Both efforts demonstrate practical use of analog VLSI decoding as a viable solution for efficient, large-constraint length digital communication systems.

6. REFERENCES

[1] M. H. Shakiba, D. A. Johns, and K. W. Martin, "An Integrated 200MHz 3.3V BiCMOS class-IV partial-response analog Viterbi decoder", *IEEE J. of Solid-State Circuits,* vol. **33-1**, pp 61-75, January, 1998.

[2] Kai He and Gert Cauwenberghs, "An area-efficient analog VLSI architecture for state-parallel Viterbi decoding", *Proceedings of ISCAS'99*, vol. II, pp. 432-435, June, 1999.

[3] E. Paaske, S. Pedersen, and J. Sparso, "An area-efficient path memory structure for VLSI Implementation of high speed Viterbi decoders", *Integration, the VLSI journal 12 (1991)*, pp 71-91..

[4] G. Feygin, P. G. Gulak, "Architectural Tradeoffs for Survivor Sequence Memory Management in Viterbi Decoders", *IEEE Trans. Commun.*, vol. **41**, No. **3**, pp 425-429, March, 1993.

[5] Kai He and Gert Cauwenberghs, "Performance of Analog Viterbi decoding", *Proceedings of MWSCAS'99*, Student Paper Contest Session. August, 1999.