

Adaptive Delay Compensation in Multi-Dithering Adaptive Control

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Abstract—Recently, a delay-insensitive architecture for gradient descent adaptive control, based on parallel synchronous detection for model-free gradient estimation was presented [1]. The key to delay insensitivity in the gradient estimation is careful selection of the phase of the local oscillator in the mixer of synchronous detection, amounting to a single parameter to be estimated per control channel. In this contribution we present a practical adaptive phase selection algorithm for delay compensation in the adaptive control architecture, and present experimental results from a SiGe BiCMOS implementation of the architecture demonstrating sub-microsecond response time in closed-loop adaptive control.

I. INTRODUCTION

Synchronous detection is fundamental to many systems which perform analog decoding of an amplitude-modulated carrier by measuring the component of the received signal in phase with the carrier. Synchronous detection is also abundant in sensory neural information processing, for instance for hyperacuity visual processing [2] and biosonar echolocation [3], to extract signals of interest buried in noise. This principle extends to *model-free* [4] adaptive control of an unknown plant, in which the effect of a control variable on the measured control objective (“metric”) is estimated by injecting a ‘dither’ carrier signal into the control variable. Synchronous detection is then performed by correlating the objective returned by the plant with the same dither signal. For multiple control variables $\mathbf{u} = (u_1, u_2, \dots, u_n)^T$, the gradient of the metric $J = J(\mathbf{u}, t)$ is estimated by applying mutually orthogonal dither signals to the control variables in parallel, and performing synchronous detection for each of the control variables. Since gradient estimation is performed without using any system model (model-free), the adaptation is immune to hardware mismatches or non-idealities.

With broad-band random dither signals, this technique is known as stochastic parallel gradient descent [5]-[8]. With narrow-band sinusoidal dither signals, this technique known as multi-dithering [9] has been used extensively in adaptive optics for wavefront correction. Most analog hardware implementations of model-free adaptive controllers perform stochastic parallel gradient descent using Bernoulli distributed dither signals [10]-[12]. Broad-band excitation, however, suffers from two major downfalls. First, the adaptation speed is limited by the delay in the plant and, in general, in the propagation

path. And second, the time-varying transfer function of the unknown plant affects non-uniformly the amplitude and delay of the frequency components of the excitation, leading to signal dispersion.

Narrow-band excitation and more specifically sinusoidal multi-dithering circumvents these limitations, since any delay in the propagation path reduces to a single parameter, phase delay in the perturbed portion of the received metric, that is easy to compensate, using phase-shifted copies of the dithers in the synchronous detection scheme. Delay compensation leads to continuous-time high-speed adaptation as demonstrated in [13], [1], where the need for a real-time phase selection process for the dithers in synchronous detection had been stressed. Recognizing this need, the work presented here proposes an adaptive algorithm for phase (and therefore time) delay compensation nested to, and one level higher than, that of the adaptive control of the plant.

The algorithm is meant for signed gradient descent adaptation and relies on the existence of limit cycles after convergence. In Section III the dependence between the frequency of the limit cycles and the delay in the loop is discussed. Section IV clarifies the necessity of a multi-phase oscillator with at least 6 phases and the proposed algorithm is presented. Finally, in Section V experimental results from application of the algorithm in a plant controlled by a SiGe BiCMOS adaptive controller are shown.

II. CONSIDERED FRAMEWORK

The considered system architecture for which the algorithm is developed was introduced in [13], is based on sinusoidal multi-dithering and is shown in Fig. 1. It consists of n channels in parallel, each serving one of the control variables u_i of the plant. The sinusoidal dithers perturbing the variables u_i are generated at distinct frequencies ω_i for each channel by 3-phase sinusoidal oscillators. The oscillator phase superimposed to the control variables is fixed, considered as reference and arbitrarily chosen to be 0° .

The perturbed control variables $\tilde{\mathbf{u}} = (\tilde{u}_1, \tilde{u}_2, \dots, \tilde{u}_n)^T$ are presented to an external plant which returns a metric signal $J = J(\tilde{\mathbf{u}})$, applied in differential form to all channels. Each channel has a linear multiplier, to keep spurious signal

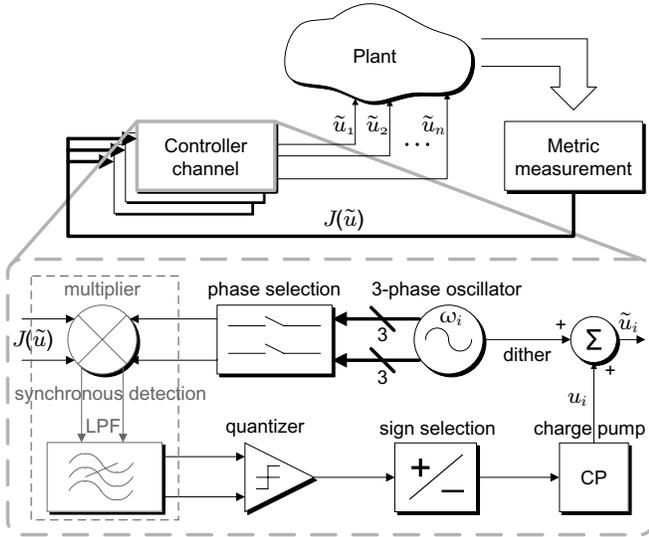


Fig. 1. System architecture of the considered framework.

levels minimal, and an adjustable high-order low-pass filter for synchronous detection.

A comparator extracts the signum of the metric's derivative $\partial J/\partial u_i$. The signum controls the direction of the current in the charge pump which continuously updates the value of the control variable u_i . A phase selection circuit preceding and sign selection circuit following the synchronous detector provide 6 alternative phases of the dither, equally spaced and spanning the entire phase domain, and allow to compensate for unknown delays in the metric.

III. SYSTEM STABILITY AND LIMIT CYCLES

Any delay in the adaptation loop introduced either by the controller or the propagation path leads to a corrupted estimate of the gradient that can potentially throw the system to instability. More specifically, time delays τ_i are mapped to phase delays φ_i [1] in the perturbed portion of the metric and result to a scaled estimate of the gradient after synchronous detection¹

$$\overline{J(\tilde{\mathbf{u}})_{\tau\text{-delay}} \cos(\omega_i t - \varphi_{oi})} = \frac{\alpha}{2} \frac{\partial J}{\partial u_i} \Big|_{\mathbf{u}} \cos(\varphi_i - \varphi_{oi}),$$

where φ_{oi} is the selected dither phase for the synchronous detection scheme. If the phase error $\varphi_i - \varphi_{oi}$ is between $\frac{\pi}{2}$ and $\frac{3\pi}{2}$ (modulo 2π), a wrong estimate of the sign of the gradient is retrieved and the system diverges from its optimum state. Minimization of the phase error (within $\pm 30^\circ$) and thus adaptation can be achieved by appropriate selection of φ_{oi} , which is discussed in the next Section.

Assuming that the delay has been compensated, in the sense that $\cos(\varphi_i - \varphi_{oi})$ is positive and a correct estimate of the gradient's sign is extracted, the control system will start converging to the optimum values for the variables u_i . Due

¹Overline denotes low-pass filtering.

to the hard-limiting nature of the comparator, convergence will be slow-rate driven and limit cycles are expected at steady state. In principle, limit cycles can be eliminated by adopting a proportional control architecture, however the L-1 norm adaptation of the signed update is robust to impulsive noise, and the limit cycle oscillations are useful for delay compensation as will be shown next.

The expected time evolution of the control variables in a delay-compensated mode is shown in Fig. 2. The variables u_i will converge at a constant rate G set by the charge pump to their optimum value and will then settle to a limit cycle of triangular shape around that value. The frequency of the limit cycles ω_{LC} depends on the loop delay τ which consists mainly of delay in the comparator, the low-pass filter and the evaluation of the metric. The amplitude of the limit cycles A_{LC} is determined both by the loop delay as well as the convergence rate G . Note the trade-off between convergence time t_s and A_{LC} , for a given loop delay τ .

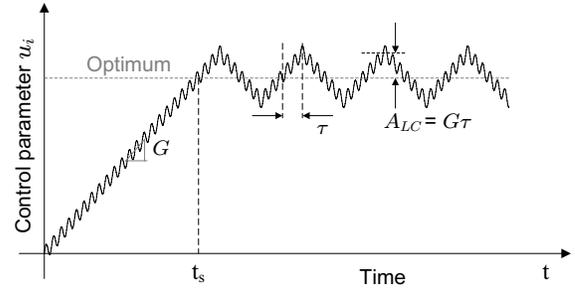


Fig. 2. Expected time evolution of the control variables during convergence.

Assuming a plant represented by a quadratic function, that leads to an inherent 180° phase-shift in the synchronous detection scheme, and taking into account the 90° phase shift due to integration at the charge pump, limit cycles will occur when the total phase shift in the loop is 360° , i.e.,

$$90^\circ + 180^\circ + \angle H(\omega_{LC}) + \omega_{LC} \cdot \tau_p = k \cdot 360^\circ \quad (1)$$

where $H(\omega)$ is the transfer function of the filter, k is the minimum integer for which (1) holds and τ_p represents any other delay in the loop, mainly due to propagation. It is obvious that for a filter of any order there is a $k > 0$ for which (1) holds. Equation (1) can be used to derive the frequency of the limit cycles ω_{LC} .

IV. ADAPTIVE DELAY COMPENSATION ALGORITHM

The proposed algorithm for delay compensation assumes that the system is already in a state where convergence has been reached and limit cycles are observed. The algorithm is therefore meant for compensation of run-time variations of the delay in the loop that can drive the system to divergence.

System convergence implies that a correct phase φ_{oi} for delay compensation has been selected, in the sense that the estimated sign of the gradient is correct. Having 6 available phases φ_{oi} to choose from, this means that at least 1 and at most 2 of the neighboring phases will also give a correct

estimate, maintain convergence and also exhibit limit cycles. Figure 3 shows the best and worst case for phase delay compensation; in case φ_i completely coincides with one of the available φ_{oi} , $\cos(\varphi_i - \varphi_{oi})$ is positive for 3 different φ_{oi} , whereas if φ_i lies in the mid-distance between two available φ_{oi} , $\cos(\varphi_i - \varphi_{oi})$ will be positive for only 2 different φ_{oi} .

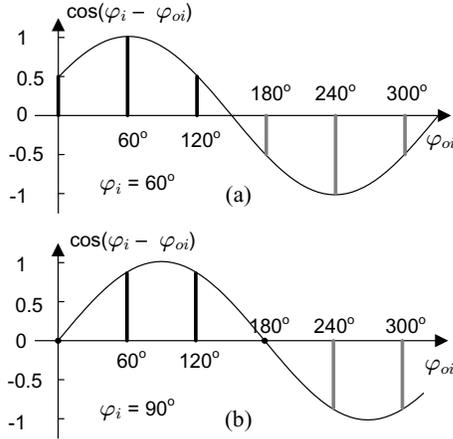


Fig. 3. (a) φ_i aligns exactly with one of the available phases φ_{oi} . (b) φ_i lies exactly in between two available phases φ_{oi} . In (a) 3 values of φ_{oi} give a positive $\cos(\varphi_i - \varphi_{oi})$, whereas in (b) only 2.

The actual selection of φ_{oi} is based on the frequency of the observed limit cycles. More specifically, smaller phase errors $\varphi_i - \varphi_{oi}$ result in higher values of $\cos(\varphi_i - \varphi_{oi})$, and consequently a larger input is presented to the comparator which, in turn, achieves lower switching times. Thus, the total delay in the adaptation loop is reduced and according to (1) a higher frequency for the limit cycles should be expected.

Based on the above observation, the steps of the proposed algorithm are the following

- 1) Starting from an arbitrary initial condition, scan sequentially all possible phase combinations for all channels and find the combination for which a limit cycle is observed and has the highest frequency among any other combination. This combination comprises of the primary selected phases φ_{oi}^p , $i = 1, \dots, n$ for each channel. If n channels are used, 6^n combinations have to be scanned.
- 2) For each channel choose as secondary phase $\varphi_{oi}^s = \varphi_{oi}^p + 60^\circ$, $i = 1, \dots, n$.
- 3) Iteratively and sequentially for each channel i measure the frequency of the limit cycle using first the primary phase φ_{oi}^p and then the secondary phase φ_{oi}^s .
- 4) If no limit cycle is observed using φ_{oi}^s , then set $\varphi_{oi}^s = \varphi_{oi}^p - 60^\circ$. It is certain that the new secondary phase will exhibit a limit cycle, since at any moment, at least two neighboring phases will be able to compensate for phase delay in a particular channel.
- 5) Compare the limit cycle frequency of primary and secondary phase. If the secondary phase exhibits limit cycles with higher frequency, then $\varphi_{oi,new}^p = \varphi_{oi,old}^s$ and $\varphi_{oi,new}^s = \varphi_{oi,old}^p$.

- 6) Repeat steps 3 through 5 for the next channel.

It should be noted that the above algorithm operates on a larger time scale than that of the actual plant adaptation and its speed is limited by the measurement of the limit cycle frequency. Therefore “slow” variations in the loop-delay must be considered.

V. EXPERIMENTAL MEASUREMENTS

The algorithm has been applied on a SiGe BiCMOS adaptive controller implemented in a $0.5\mu\text{m}$ technology according to the architecture presented in Section II. For the experiment, the plant under optimization was a four-input diode metric implementing the function $f(V_1, V_2, V_3, V_{ref}) = \max(V_1, V_2, V_3, V_{ref}) - \min(V_1, V_2, V_3, V_{ref}) - 2V_F$, where V_1, V_2 and V_3 are the voltage outputs from 3 channels of the controller, V_{ref} is a reference signal and V_F is the forward voltage drop on the diodes. Function f has a global minimum when $V_1 = V_2 = V_3 = V_{ref}$ and purpose of the experiment was to observe all 3 channels of the controller converging to the reference value V_{ref} .

Adaptation of the plant was observed under varying delay conditions. The delay was varied by inserting an RF variable length transmission line between the control output of one channel, and one of the input terminals of the four-input diode metric circuit used in the above experiments. This introduced a 0-80 ns variable delay in one of the channels, while the delay of the two other channels was kept fixed. The experiments were performed setting the dither frequencies of the 3 control channels at 86MHz, 118MHz and 149MHz, with a cut-off frequency of the filter at 20MHz.

Figure 4 shows the observed limit cycle frequency of the channel perturbed at 86MHz, as a function of the inserted delay, for all 6 phase selection values, while the other two channels are set to optimal phase selection values. The delay is varied in 11 steps with increments of approximately 1.2ns, that correspond to phase steps of $\sim 37^\circ$ for the phase delay φ_i . Unstable states resulting in no limit cycles have low frequency values that are outside the range of the graph. As shown, the phase φ_{oi} that exhibits the highest limit cycle frequency cycles sequentially from 60° at an added delay of 0ns to 120° at 10.1ns following a monotonically decreasing trend and covering all possible values of φ_{oi} in the intermediate steps. Note also the decrease of the highest limit cycle frequency as the delay increases, predicted by (1).

Delay compensation through real-time switching of the phase φ_{oi} used for synchronous detection is shown in Fig. 5. For the experiment, optimal values for the dither phases φ_{oi} of all channels were initially set, and the adaptive phase selection algorithm of Section IV was applied as the delay in one channel (the one perturbed at 86MHz) was again sequentially varied in 11 steps at increments of $\sim 1.2\text{ns}$. Both the primary and secondary phases selected by the algorithm are shown. Clearly, the channel at which the delay is inserted tracks the delay introduced in its loop, whereas the other channels remain locked to their constant loop delays.

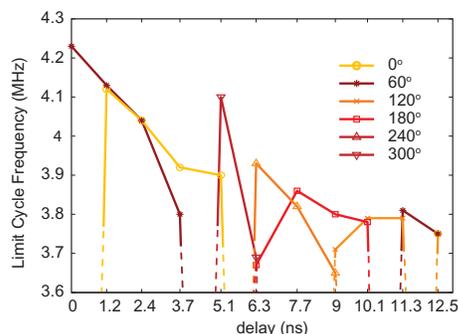


Fig. 4. Frequency of the limit cycle as a relation of the introduced delay in a channel, for all possible selected phases in the synchronous detection scheme.

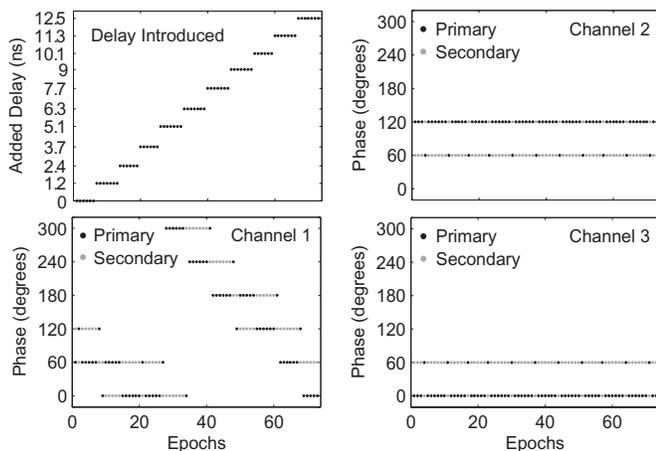


Fig. 5. Algorithm application for the case of 3-channel control and of inserted delay in one channel of the system. The phase selected for compensation changes only at the channel the delay is introduced (channel 1).

Oscilloscope traces for the adaptation of the metric, both for the case of no added delay and for the case of a significant delay (~ 80 ns) added to one of the channels, are shown in Figs. 6(a) and (b), respectively. Note that the adaptation time is below $1\mu\text{s}$ and due to delay compensation the same in both cases. Delay compensation operates in a ms timescale and is limited by the host computer interface and data logging.

VI. CONCLUSION

An adaptive algorithm for real-time delay compensation in a sinusoidal multi-dithering adaptive scheme has been presented based on compensation of phase delays in the under optimization metric. The algorithm relies on the existence of limit cycles in the control variables after convergence and runs on top of the actual system adaptation. Measurements from application of the algorithm on a multi-dithering SiGe BiCMOS controller show delay compensation in a millisecond time scale, while a nonlinear plant metric is optimized in sub-microsecond time scale.

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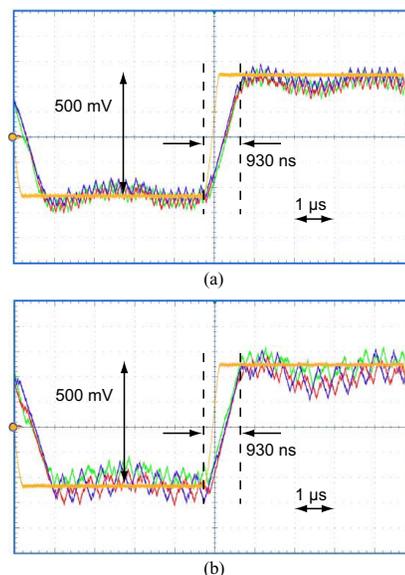


Fig. 6. Optimization of the min-max metric function for the case of 3 input controls and a 100kHz square wave reference. (a) Optimization without any added delay. (b) Optimization for an 80ns delay added in one of the channels. The frequency of the limit cycle drops while its amplitude increases, however the adaptation speed remains the same due to delay compensation.

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