Intensity Histogram CMOS Image Sensor for Adaptive Optics

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***Abstract*— We present a high-speed CMOS active pixel sensor (APS) image sensor with focal plane histogram computation. The 128x128 4-transistor active pixel sensor array produces cumulative intensity histograms, at the focal-plane, with speeds in excess of 10,000 frames per second for low-latency, real-time control applications without the need for pixel digitization of external processing. In addition, an on-chip 10-bit column parallel analog-to-digital converter with a read noise of 0.6LSB and negligible fixed pattern noise facilitates conventional imaging operations and data acquisition. Each pixel occupies 19.5 m x19.5 m with a fill factor of 43%. Power consumption is 1.5mW during imaging mode and 4.6mW in high-speed histogram mode. Applications include real-time adaptive optics control for laser communications.**

I. Introduction

Adaptive optical systems are highly useful for correcting for the distortions introduced by atmospheric turbulence in a wide class of applications including high speed laser communications and ground based astronomy [1]. One class of algorithms, stochastic gradient descent [2] [3] has been shown to be effective for correcting optical aberrations.

One challenge, in particular, is generating the quality metric used in a closed loop adaptive system. Image quality metrics that measure the sharpness or focus of the image are critical for adaptively optimizing the system. Producing metrics at high frame rates using conventional image sensor technologies becomes highly demanding due to the need to acquire and process a large number of pixels. As an example, one effective metric, the J_2, is defined as the squared value of each pixel, summed globally. For a sensor size of 128 x 128 pixels running in a closed loop control application at 10,000 frames/sec, a pixel clock of 164 MHz is required to digitize all the pixels alongside a suitable high speed digital processor. In addition, acquisition and processing must occur after frame exposure, introducing additional lag into the control loop. To date, most high speed control systems have relied on the use of desktop PCs and expensive, scientific grade image sensors [1].

As an alternative, previous works have demonstrated the use of focal-plane processing to produce image/beam metrics directly at the sensor [3]. In this paper, we present a high speed image sensor (excess of 10,000 frames/sec) designed for real-time closed loop optical control systems (Fig. 1). The sensor directly outputs image statistics in the form of the image histogram without the need to scan and read out pixels in the array. Computing the metrics used in adaptive optics, such as the J_2, in the histogram domain is much more computationally efficient since the number of data points processed is set only by the bit depth of the pixel (typically only 256 to 1024) and is independent of the array resolution.

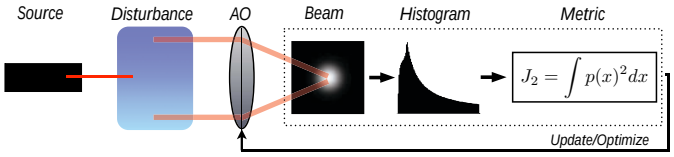

Fig. 1. Intended real-time optical control application. The sensor computes histogram based beam quality metrics which are used to adaptively optimize the optical system at a very high frame rate.

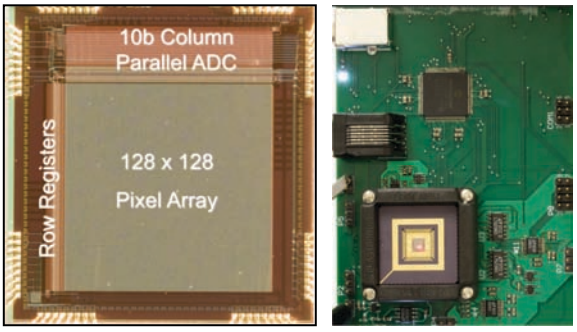

Fig. 2. Micrograph of the histogram image sensor and sensor integrated as part of a test system.

The scope of this paper focuses on the core functionality of the CMOS image sensor, describing the operation of the pixel-level histogram circuit and the 10-bit column-parallel ADC.

II. Chip Description

A micrograph of the sensor is shown in Figure 2. The core of the chip is an 128 by 128 pixel array containing the circuits for focal-plane histogram circuit. Row and column registers at the periphery facilitate timing and optional windowing operations. The ADC is located at the end of each column of pixels.

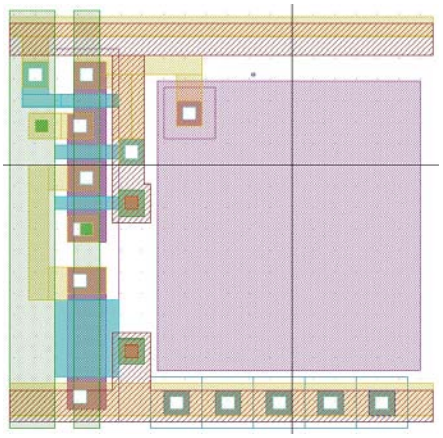

Fig. 3. Layout of the 19 5 m by 19 5 m pixel.

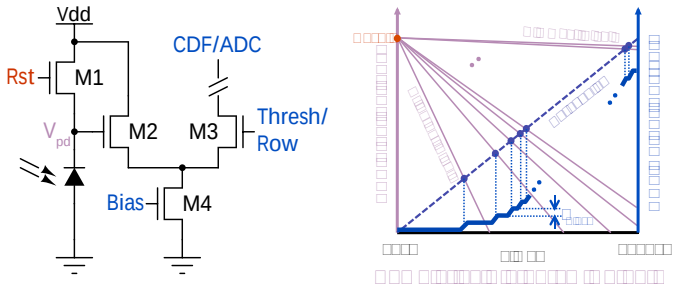

Fig. 4. Schematic of the histogram APS circuit along with an illustration showing the generation of a cumulative histogram by summing the currents from all the pixels in the array.

A. APS with Focal-Plane Histogram Computation

The pixel design (Fig. 4) is based on the standard 3-T APS [4] (M1-M3), but with the addition of just a single extra transistor (M4). In histogram mode, transistors M2 and M3 operate as a differential pair with M4 providing the tail bias current. The devices are biased in sub-threshold for low power operation. The drain of M3 is the pixel's output and is joined together globally to sum the currents from all pixel into an output pin. Since the histogram circuit incurs only a single additional transistor at the pixel (Fig. 3), impact on fill-factor and image quality is minimal. For high-speed imaging, it is especially important to minimize the impact on the sensor's sensitivity.

Histogram computation operates in tandem with photocurrent integration and begins immediately after reset. The differential pair in the pixel can be thought of, roughly, as a comparator between the discharging photodiode voltage, V_{pd}, at the input of M2 and a global threshold, V_{th}, at the input of M3. For simplicity, the circuit is first analyzed with V_{th} as a fixed value, although different wave forms can be used to obtain different histogram responses (a ramp is illustrated in Fig. 4).

The photodiode voltage, V_{pd} during the frame can be written as,

$$V_{pd} = V_{rst} - \frac{i_{pd}}{C_{pd}} t \tag{1}$$

where V_{rst} is the reset voltage, i_{pd} is the photocurrent, C_{pd} is the integrating capacitance and t is the time into the current integration cycle. The time it takes to cross the threshold V_{th} is then,

$$t_{cross} = \frac{C_{pd}(V_{rst} - V_{th})}{i_{pd}} \tag{2}$$

Thus, brighter pixels (those with larger i_{pd}) drop below the threshold faster than dimmer ones. At point, t_{cross} the pixel outputs its bias current, I_{bias} to the global summing line at the drain of M3 for the remainder of the integration period.

The aggregate effect of all the pixels in the array operating in this fashion results in a global current, I_{cdf}, which represents a time encoded, cumulative histogram (CDF) of the image. The current, I_{cdf}, at time t is the sum of all pixels, I_{cdf} I_{bias}, with a photocurrent greater than,

$$i_{pd} > \frac{C_{pd}(V_{rst} - V_{th})}{t} \tag{3}$$

In contrast to a conventional histogram, the index bins are reversed and displayed in decreasing, rather than increasing order. However, simply differentiating and then reversing all the samples of I_{cdf} results in a conventional histogram.

Devos et al. [5] implemented a video frame rate histogram sensor using a broadly similar architecture for exposure correction. In their version, the differential pair was configured as a full CMOS comparator, including the complementary active load. By removing the active load, the histogram becomes smoothed at lower light intensities due to the $tanh$ response of the differential pair. However, the simplification of the circuit allows this implementation to maintain a high pixel fill factor and image quality. At the same time, response to the bright intensities that contain the useful metric information remains unaffected.

As mentioned previously, different waveforms can be used for V_{th} to change the mapping between the time index and pixel intensity value. In practice, a simple fixed value or linear ramp produces good results without introducing additional circuit complexity.

Power consumption for this circuit is dominated the need for each pixel to be actively biased with a current source, approximately 50nA, and scales directly with array size. The amount of power consumed does not vary significantly with frame rate. Only a simple medium speed amplifier and ADC are required to process the CDF data from the sensor. Since the number of samples/bins is relatively small (256 for 8-bits), a simple microcontroller can handle all the data processing operations.

B. 10-bit Column-Parallel ADC

Aside from the histogram mode, the imager can also function as a conventional APS with the on-chip 10-bit column-parallel ADC for characterization and image acquisition purposes. In imaging mode, transistor M4 is turned off and M3 functions as a row-select switch, connecting the source follower M2 to a column bias current, reverting the pixel to a standard 3-T APS [4].

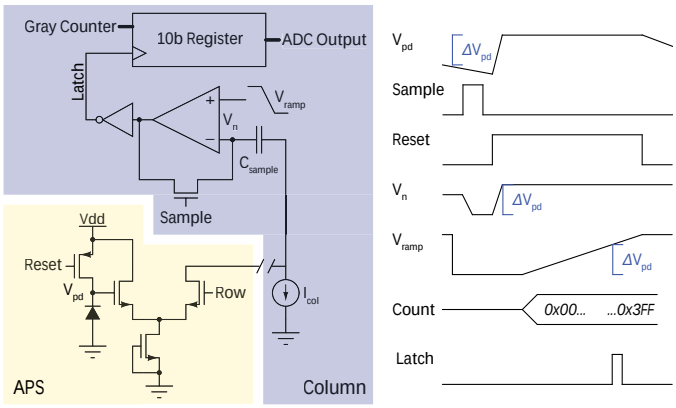

Fig. 5. Schematic of the column-parallel ADC and timing signals.

Figure 5 shows the block diagram of the ADC along with its timing diagram. The integrated photodiode voltage from reset, ΔV_{pd} is stored on C_{sample} by asserting the feedback switch around the opamp at the end of the frame cycle. After sampling, the opamp now functions without feedback as a comparator and the pixel is reset, pulling the inverting input of the opamp, V_n, up by ΔV_{pd} and forces the output low. While the pixel is held in reset, a global ramp signal, V_{ramp} connected to the non-inverting input begins to increase alongside with a count signal. As the ramp increases by amount ΔV_{pd} from its initial state, the comparator's output goes high, triggering the ADC's latch circuit to store the count, which is the digital representation of ΔV_{pd}.

The ADC, in the described mode, performs delta difference sampling (DDS) by subtracting the pixel voltage from the next frame's reset voltage rather than correlated double sampling (CDS). While this doubles the amount of $\frac{kT}{C}$ reset noise, the operation still effectively removes offset fixed pattern noise (FPN), producing clean images.

The concept and implementation of the ADC circuit is similar to previous work [6] [7] but with one main difference - the ramp is coupled to non-inverting input of the opamp/comparator rather than through a capacitor network that connects both the APS signal and ramp both to the inverting input. This reduces the number of switches required as well as the need for two matched capacitors.

III. Results

The image histogram sensor was integrated on to a test board (Fig. 2) containing a transimpedance amplifier and ADC to digitize the CDF current along with a USB data acquisition system.

To test the functionality of the histogram circuit, the sensor was illuminated by a laser beam of constant intensity but at varying degrees of focus. Figure 6 shows the oscilloscope traces of the CDF current for two different extremes of focus along with the reset timing signal for 10,000 frame/sec operation.

In the upper trace, the beam was completely unfocused across the array. Accordingly, the CDF output exhibited a large

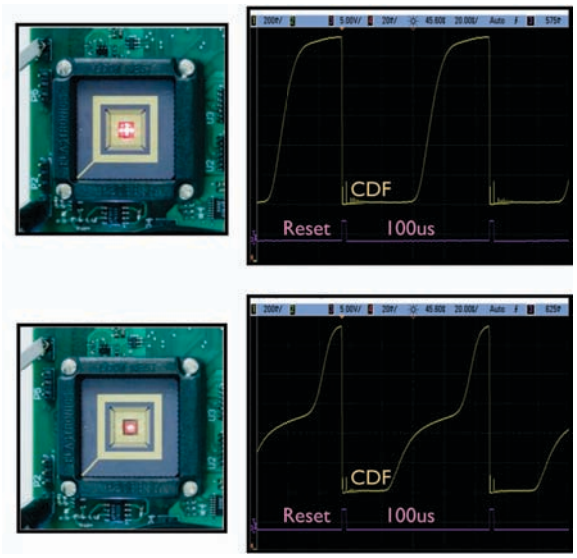

Fig. 6. Oscilloscope traces of the CDF output is shown for two beam profiles along with reset timing for 10,000fps frame rate.

step towards the end of the integration period corresponding indicating a large distribution of relatively dim pixels in the image. In the lower plot, the beam was projected so that it was focused on the center of the array. The CDF output showed two steps – one near the start of the frame corresponding to the bright pixels illuminated by the beam and a step at the very end corresponding to the pixels at the periphery.

A more detailed plot of the CDF, digitized and acquired into the computer, is shown in Figure 7. For comparison, a digitally generated version CDF of the same beam images was made from the sensor's ADC output. The beam image from the ADC is also shown on the side. As expected, the cumulative histogram directly from the pixel's analog circuit matches closely with the one from sampling each pixel and computing it digitally. The only deviation is a slight offset, along with a smoothing at lower light intensity bins due to the $tanh$ response of the differential pair.

To characterize the response pixel and ADC, the image sensor was illuminated by a diffuse, uniform light source at various intensity levels. At each light step, the temporal noise variation and mean ADC code was recorded to obtain the photon transfer curve (PTC), shown in Figure 8. From this plot, the dynamic range and resolution of the sensor is 9.4-bits matching well with the column-parallel ADC design. Fixed pattern noise was measured to be negligible.

Figure 9 shows two sample images taken from the sensor under indoor room illumination at standard video rates. The pictures are both qualitatively clean and free of noise, showing the image quality of the sensor even with the addition of the pixel-level histogram circuit.

IV. Conclusion

We present a CMOS image sensor with high-speed, low complexity, focal-plane histogram computation. A summary of the sensor's specifications can be found in Table I. The 128

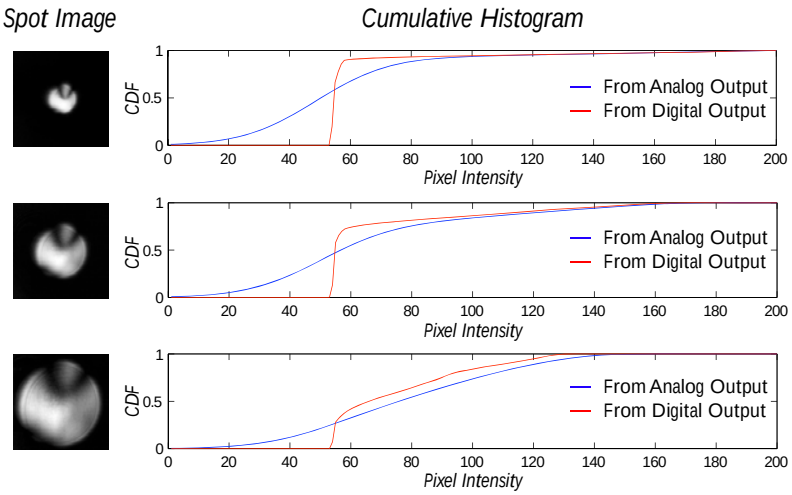

Fig. 7. Cumulative histogram of three beam profiles along with the image, acquired through the on-chip ADC. The analog CDF computed directly on the focal plane is compared with the digitally generated CDF from the ADC output.

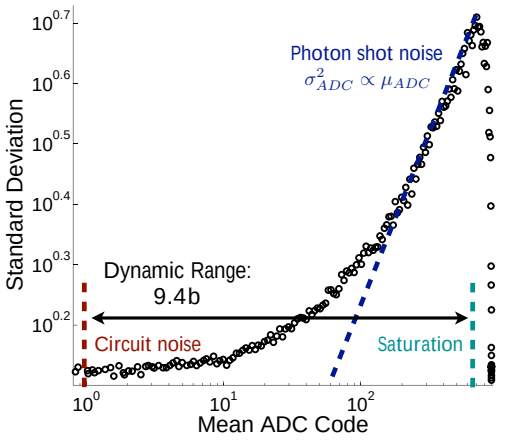

Fig. 8. Photon transfer curve of the pixel and ADC characterizing the dynamic range of the image sensor.

Fig. 9. Two sample images from the sensor.

by 128 array directly produces a cumulative histogram output, without the need for external processing at rates beyond 10,000 frames per second while consuming only 4.3mW. Future work will address the use of the sensor as part of a closed loop, adaptive optics, control system.

TABLE I
CHIP SUMMARY

Process	0.5 m CMOS
Chip Area	13.4mm^2
Resolution	128 $\times$ 128
Pixel Size	19.5 m^2
Fill Factor	43%
Full Well Capacity	23,000e^-
Read Noise	34.8e^-
ADC ENOB	9.4b
Power Consumption	4.6mW (CDF), 1.5mW(ADC)
Voltage Supply	3.3V

V. ACKNOWLEDGEMENTS

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