

VLSI DELTA-SIGMA CELLULAR NEURAL NETWORK FOR ANALOG RANDOM VECTOR GENERATION

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ABSTRACT

We present a cellular neural network architecture for parallel analog random vector generation, including experimental results from an analog VLSI prototype with 64 channels. Nearest-neighbor coupling between cells produces parallel channels of uniformly distributed random analog values, with statistics that are truly uncorrelated across channels and over time. The cell for each random channel emulates an integrating nonlinearity essentially implementing a delta-sigma modulator, and measures $100 \mu\text{m} \times 120 \mu\text{m}$ in $2 \mu\text{m}$ CMOS technology. Applications include analog encryption and secure communications, analog built-in self-test, stochastic neural networks, and simulated annealing optimization and learning.

1. INTRODUCTION

On-line random analog signal generation is an essential component in many of today's analog VLSI systems for signal or information processing. An on-line supply of random analog vectors comes handy, for instance, to support testing and characterization of the hardware, or as part of the implemented algorithms. Examples of applications include encryption and secure communications [1], analog VLSI built-in self-test [2], and neural computation [3, 4], simulated annealing optimization [5] and stochastic model-free learning [6, 7].

Most commonly used in VLSI are arrays of random binary sources implemented with linear feedback shift registers (LFSR) [8, 9] or cellular automata (CA) [10, 11], which yield compact and scalable parallel VLSI architectures [12]. High-bandwidth, low-power analog noise generators in VLSI are obtained by means of chaotic oscillators [13, 14], or through recursion of a nonlinear map such as the logistic map or a linear congruential map [15, 16].

In this paper, we consider cellular arrays of cascaded delta-sigma modulators for the purpose of random analog vector generation. The particular form of nonlinear coupling between cells not only avoids correlations across cells, but in addition produces a truly random sequence in the sense that the outcome of a cell at a given time is statistically independent of its history. The interactions are nearest-neighbor as in cellular automata, and permit a simple scalable and parallel VLSI architecture. Our motivation to study these structures is inspired by remarkable noise-shaping properties observed in "MASH" cascade structures of delta-sigma modulators [17, 18, 19], as used for stable higher-order oversampled A/D conversion [20, 21].

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The following section introduces the basic cellular architecture and its variants, and relates delta-sigma modulation to a congruential linear analog version of additive cellular automata. Section 3 presents a compact analog VLSI implementation, and Section 4 includes experimental results from a 64-channel (and 65-channel) CMOS prototype. Finally Section 5 concludes the results.

2. NONLINEAR NOISE-SHAPING AND CELLULAR ARCHITECTURE

The general structure we consider combines additive cellular automata [10] and cellular neural networks [11], together with linear congruential (*i.e.*, modulo residue) maps or, as shown to be equivalent [18], delta-sigma modulation [21]. The interactions between cells are of the form

$$x_i(k+1) = f\left(\alpha + \beta \sum_{j \in \mathcal{N}(i)} x_j(k)\right) \quad (1)$$

where $\mathcal{N}(i)$ defines a neighborhood of cells interacting with cell i including itself, and where $f(\cdot)$ defines a nonlinear map. Besides careful choice of the constants α and β , the form of $f(\cdot)$ is critical to the randomness properties of the sequence $x_i(k)$. The map $f(\cdot)$ is defined, as the quantization residue in single-bit delta-sigma modulation:

$$\begin{aligned} f(x) &= x - \text{sign}(x) \\ &= x - 1 && \text{if } x > 0; \\ &= x + 1 && \text{if } x \leq 0. \end{aligned} \quad (2)$$

It can be shown [17, 18] that this map is functionally equivalent to a modulo operation, which can be analyzed with the standard rules of residue arithmetic.

2.1. Cascade and Cellular Structures

The general template of nearest-neighbor interactions (1) allows to formulate cellular networks of various topologies. The simplest case to be possibly considered is a neighborhood of two cells: one cell and one of its neighbors. With $\alpha = 0$ and $\beta = 1$ we obtain

$$x_i(k+1) = f(x_i(k) + x_{i-1}(k)). \quad (3)$$

This is functionally equivalent to a "MASH" cascade of first-order, single-bit delta-sigma modulators [22], where the quantization "noise" of the integrator of one stage feeds into the next [20]. Cascaded structures of the MASH type are attractive for stable higher-order oversampled A/D conversion since the modulators do

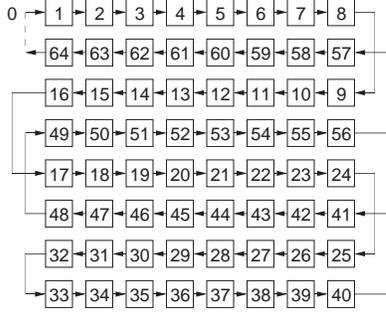


Figure 1: Array of 64 MASH random generating cells. Linear cascaded chain or ring topology implemented on a 2-D grid.

not overload and the “noise” does not appear to correlate with the input at least for constant and sinusoidal inputs [17] and iid random inputs [19].

We consider two special cases of boundary conditions for the cascade structure of N cells $x_1 \cdots x_N$: a “chain” topology with a constant input supplied to the first element x_1 , and a “ring” topology with cyclic boundary conditions where the output of the last element x_N feeds into the input of the first x_1 ($x_0 \equiv x_N$ in (3)). The ring structure is preferable because of symmetry which provides more uniform random noise properties across the array, although stability of noise-shaping in the feedback loop is an issue which will be addressed below.

The linear cascaded chain and ring topologies can be implemented in scalable cellular VLSI architectures on either a 1-D and 2-D grid. To realize the chain and ring topologies on a 2-D grid, shown in Figure 1, two sets of linear cascade segments are interleaved in opposing directions, and external connections at the periphery of the array span no more than two adjacent cell spacings on the grid.

Theory on the statistical and dynamical randomness properties of both topologies is presented in [23]. This paper focuses on circuit architectures and VLSI implementation.

3. IMPLEMENTATION

Analog VLSI implementation offers potentially higher integration density and higher energy efficiency than equivalent digital VLSI implementations. Unlike more conventional analog designs, where high precision and high noise rejection are primary design constraints, the circuits can be implemented with minimum-size, noisy and imprecise components biased at lower currents.

3.1. Architecture

We have adopted an implementation style using low-power, high-density switched-capacitor circuits, producing a voltage output format, $V_i(k)$. In principle, compact alternative realizations using current-mode technology, of the type used in [16], can be derived as well.

The switched-capacitor architecture implementing the MASH cell is shown in Figure 2 (a), and the corresponding signal timing diagram is given in Figure 2 (b). The state $V_i(k)$, corresponding to $x_i(k)$, is stored across capacitor C_2 . To save power and silicon real-estate, the amplifier A serves the dual purpose of accumulator $\frac{1}{z-1}$ and quantizer f , controlled by the COMP signal. When COMP is

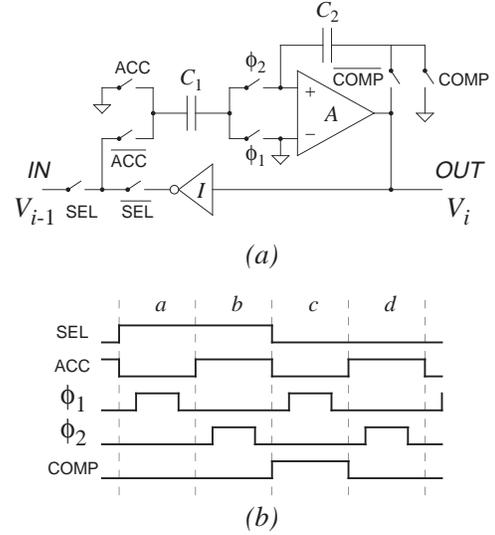


Figure 2: Switched-capacitor MASH modulator cell. (a) Simplified circuit diagram. (b) Timing diagram.

active high, amplifier A compares V_i with zero, and presents the result (sign of V_i) to the accumulator input through the inverting one-bit D/A converter I . When COMP is inactive (low), $V_i(k)$ is presented to the output OUT. The accumulator functions as a standard switched-capacitor non-inverting integrator [21], where in the sampling phase the capacitor C_1 is precharged to the input, and in the accumulate phase this charge is transferred onto capacitor C_2 . This operation is controlled with signals ACC, ϕ_1 and ϕ_2 , repeated twice as shown in Figure 2 (b) (Phases a - b , and c - d). The input to the accumulator is controlled by the SEL signal, which first selects the output from the preceding stage $V_{i-1}(k)$ presented to IN, and then the output from the comparator. The four-phase operation is summarized as follows:

- a : Sample input $V_{i-1}(k)$ from previous stage;
- b : Accumulate;
- c : Compare with zero; and sample inverted result;
- d : Accumulate; yielding $V_i(k+1)$.

Functionally, the first accumulate produces $x_i(k) + x_{i-1}(k)$, and the second accumulate subtracts the sign of the first. The net operation thus yields $f(x_i(k) + x_{i-1}(k))$ as desired.

3.2. CMOS Implementation

The transistor-level circuit diagram of the MASH cell is shown in Figure 3. For low-power operation and compatibility with digital interface circuitry, the circuit uses a single supply V_{dd} , set to 5 V for the experiments. The signal ground level is set to $V_m = 2$ V, and the signal range is ± 1 V as determined by the D/A levels, $V_{ref}^- = 1$ V and $V_{ref}^+ = 3$ V, symmetric around V_m . Thus,

$$V_i(k) = V_m + V_{range} x_i(k) \quad (4)$$

where $V_{range} = 1$ V.

The amplifier A is implemented as a single, non-cascoded pseudo- n MOS inverter M1-M2. The relatively low gain of this design is adequate for the purpose of a random generator, where

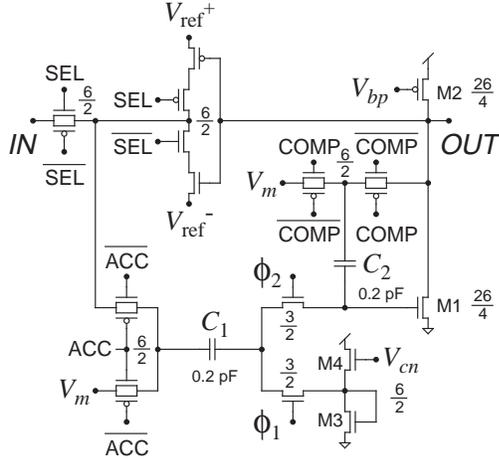


Figure 3: CMOS switched-capacitor circuit diagram of MASH modulator cell.

linearity and gain errors are less important than power dissipation and size. The virtual ground voltage of the amplifier, used for the precharge in the sampling phase of the accumulator, is obtained from circuit M3-M4, of which the V_{cn} bias is generated from the unity-gain connected amplifier is because the accumulator output is needed simultaneously to precharge the next cell, occupying the amplifier. This introduces $1/f$ noise in the accumulator which otherwise would have been cancelled by a correlated double-sampling technique. Finally, the capacitances C_1 and C_2 are 0.2 pF in $2 \mu\text{m}$ technology, enough to provide adequate matching, and to avoid excessive switch-injection and clock-feedthrough noise contributed by the switches ϕ_1 and ϕ_2 .

4. EXPERIMENTAL RESULTS

Figure 4 shows a micrograph of the Tiny ($2.22 \text{ mm} \times 2.25 \text{ mm}$) double-metal, double-poly $2 \mu\text{m}$ CMOS chip prototyped through MOSIS, which integrates a two-dimensional array of 64 MASH cells configured as shown in Figure 1, plus one extra MASH cell and additional test circuitry. The cell for each random channels measures $100 \mu\text{m} \times 120 \mu\text{m}$ in $2 \mu\text{m}$ technology.

All experimental results reported in this paper were obtained from this chip. Experiments were performed on chain and ring topologies with 64 and 65 cells, using the array of 8×8 modulators plus the extra modulator.

Transfer Characteristics: The measured transfer characteristic of a single MASH modulator cell, implementing (3), is shown in Figure 5, for a spectrum of input and output voltages in the range of the $[V_{ref}^-, V_{ref}^+]$ interval. The combined gain errors are in the order of 5%, and their effect on the random statistics is evaluated next.

Statistics: The hypothesis of statistical independence $p_{i,j}^{k,l}$ across channels and over time was tested experimentally, illustrated in Figure 6 for two concurrent neighboring outputs in the ring topology. The scatter-plot shows $x_i(k)$ vs. $x_{i-1}(k)$, corresponding to the joint probability density which clearly is uniform as expected. For the chain topology, the obtained results were qualitatively similar, except for the first

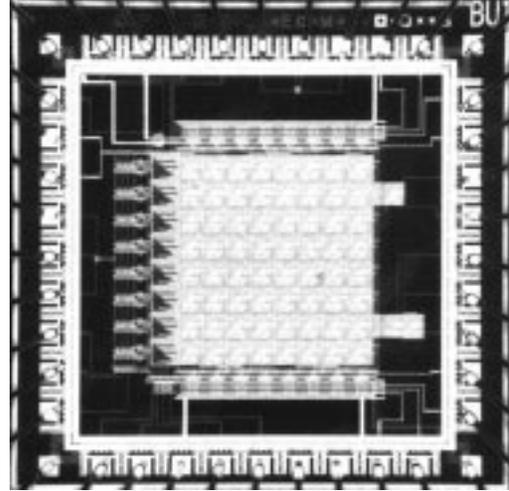


Figure 4: Micrograph of the 64(+1)-channel VLSI parallel random analog vector generator, including an 8×8 array of MASH modulators plus one extra modulator. Dimensions are $2.22 \text{ mm} \times 2.25 \text{ mm}$ in $2 \mu\text{m}$ CMOS.

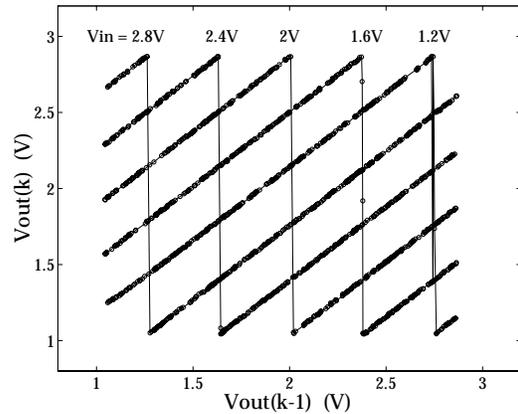


Figure 5: Transfer characteristic of a single MASH modulator cell.

few channels which showed systematic correlations, due to transient effects studied next.

Dynamics: We extensively studied the effect of chain and ring topologies on the transient and steady modulation dynamics. Spectral analysis of experimental data over a 1024-point time window, shown in Figure 7, reveals that effects of limit cycle oscillations or other colored spectral features are limited to no more than the first three stages of the chain, and are absent in the ring.

System-Level Issues: The operation of the chip has been verified over a range of speeds from 2 Ksamples/s to 50 Ksamples/s per channel. The maximum of 50 Ksamples/s per channel that we obtained is affected by external capacitive loading of the (multiplexed) output which has not been buffered. Measurements of supply currents yield power dissipation levels ranging from $16 \mu\text{W}$ to $245 \mu\text{W}$ per cell, corresponding to 6 nJ of energy dissipated per sample.

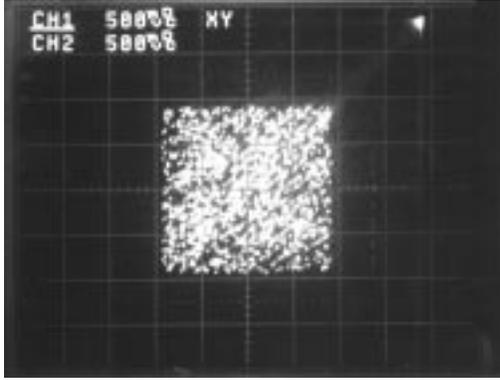


Figure 6: Oscilloscope X - Y plot showing outputs from two neighboring channels in the 65-channel ring.

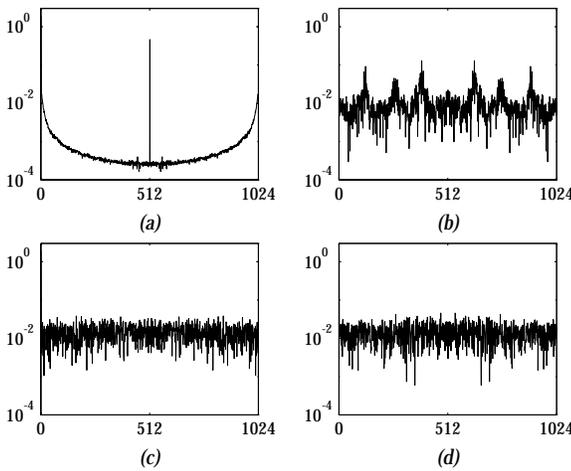


Figure 7: Fourier spectra of cell sequences. (a) First cell in the 65-cell chain, with zero-level (V_m) input. (b) Second Cell. (c) Fourth Cell. (d) 65-cell ring.

5. CONCLUSION

Delta-sigma modulation and residue arithmetic have been combined into a cellular network architecture for parallel analog random vector generation, with statistical properties that are unique to the functional form of interactions across cells and not found in arrays of separate analog random generators: statistical independence over time, and across channels. We have presented cellular architectures, and experimentally verified the results on a 65-channel VLSI prototype.

The cell layout supports the integration of over half a million random generators on a 1 cm^2 die in $0.2 \mu\text{m}$ CMOS technology. Besides the excellent statistical properties, the small size and low energy consumption of the random cell make it particularly well suited for large-scale integrated applications of parallel distributed analog signal and information processing, where an on-line supply of random values is embedded locally with each processing element.

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