AN AREA-EFFICIENT ANALOG VLSI ARCHITECTURE FOR STATE-PARALLEL VITERBI DECODING

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ABSTRACT

An area-efficient analog VLSI architecture is presented to implement a low-power, state-parallel, rate $R = 1/2$, constraint length $K = 7$ Viterbi decoder. A combination of current-mode and switched-capacitor techniques are used in designing the Add-Compare-Select (ACS) module, resulting into a very compact VLSI architecture, implemented in a 64-state hard-decision Viterbi ACS VLSI chip fabricated in a 2μm CMOS process through MOSIS. The chip has been tested to operate at 500 kbps data rate and 7.65 mW power dissipation.

1. INTRODUCTION

Convolutional coding and Viterbi decoding are widely used in modern digital communication systems, such as space communication, satellite communication, and mobile communication, to achieve low-error-rate data transmission. The essential features of a digital communication system are described in Figure 1.

The Viterbi algorithm is commonly used in signal processing and communications. In digital communication systems, the Viterbi algorithm is utilized in the maximum likelihood decoding of convolutional codes and is called Viterbi decoding. It is a recursive optimal solution to the problem of estimating the state sequence of a discrete-time finite-state Markov process observed in memoryless noise [1]. In terms of computation complexity, it presents the most efficient way to find an optimal path through a convolutional code trellis, and is suitable for hardware implementation.

Different architectures are available to design a Viterbi decoder in VLSI. Which one to choose mainly depends on the convolutional code chosen for the communication system and requirements of the specific application. Fast developments in telecommunications have created a rising demand for high-speed, low-power and low-cost Viterbi decoder VLSI chips for large convolutional codes (long constraint length codes). Owing to advances in CMOS semiconductor technology, a large Viterbi decoder can now be built on single chip, or even as an integrated part of a system-on-a-chip. But the limits of technology still leave us trade-offs to make in choosing the architectures. One important trade-off in Viterbi decoder design is between speed and area. High-speed can be achieved by applying parallelism, while this dramatically increases the chip area and power consumption.

The add-compare-select (ACS) unit comprises the core in all types of Viterbi decoders. The critical path in the ACS feedback loop presents the bottleneck of the decoder speed, and efforts have been made to better design the ACS unit by introducing parallelism at different levels [2]. Two of the most commonly used ACS architectures are state-parallel and state-sequential. The state-parallel approach is the choice for high-speed Viterbi decoders, such the NTT NUFEC [3], while the state-sequential approach is always adopted in low-speed low-power applications, such as a recent work on CDMA by Kang and Wilson [4]. Another choice has to be made when designing a Viterbi decoder is the memory management. There are basically two types of memory management schemes, register-exchange (RE) and trace-back (TB). The RE approach is suitable for fast decoders [3], but its complexity and power consumption dramatically increases with the constraint length K. On the other hand, the TB path memory consumes less power and silicon area [4] but is much slower than the RE counterpart.

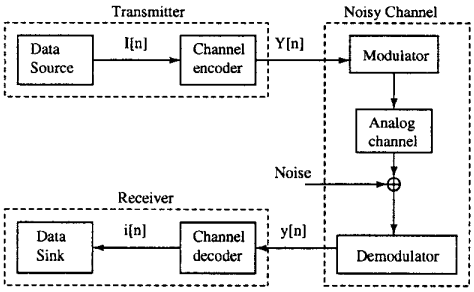

Figure 1: *Model of a coded digital communication system.*

There have been some effort on applying analog circuit techniques to design better Viterbi decoders as early as 20 years ago [5]. The advantages of analog computation depend on the application in which the decoder is to be used. Analog Viterbi detectors have so far been used for memory reading channels [6] [7], for relatively small constraint length codes. In this paper, a general-purpose analog Viterbi decoder ACS module is presented. Various analog VLSI circuit design techniques have been used to design a low-power area-efficient 64-state ACS module VLSI chip for rate $R = 1/2$, length $K = 7$ convolutional code. The chip consumes just a portion of the power and silicon area of a traditional digital counterpart, and is probably the most compact 64-state ACS ever built. The improvements in implementation efficiency are due to a combination of analog VLSI current-mode and switched-capacitor techniques which offer superior speed and area-efficiency margin

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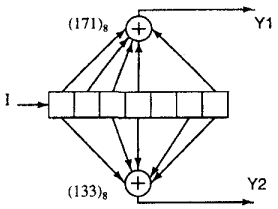

Figure 2: *Configuration of the encoder for rate $R = 1/2$ and length $K = 7$ convolutional code.*

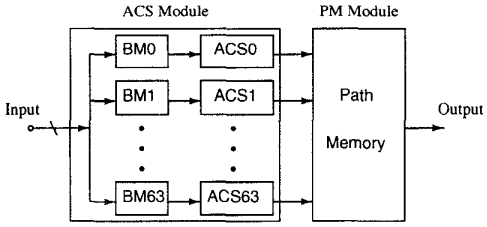

Figure 3: *A Viterbi decoder architecture for rate $R = 1/2$ and length $K = 7$ convolutional code.*

over digital VLSI.

2. THE VITERBI DECODER ARCHITECTURE

2.1. Convolutional Encoding

The $(2, 1, 7)$ convolutional code, or the rate= $1/2$ $K = 7$ convolutional code, is a commonly used code in NASA space programs and satellite communication systems. Its generation polynomial is $(171, 133)_8$ expressed in octal expression. The encoding is mathematically defined by defined by

$$\begin{aligned} G^{(1)} &= 1 \oplus D \oplus D^2 \oplus D^3 \oplus D^6 \\ G^{(2)} &= 1 \oplus D^2 \oplus D^3 \oplus D^5 \oplus D^6 \end{aligned}$$

where "D" denotes delay operator and "$\oplus$" denotes modulo-2 addition.

The convolutional encoder is illustrated in Figure 2, implemented by a 7-bit shift-register and two multiple-input modulo-2 adders. The encoder is a finite-state machine with the last 6-bit shift-register as the state vector and the first bit as the input, and a 64-state trellis is associated with this convolutional code. In general, the number of states in the trellis N is determined by $N = 2^{K-1}$.

2.2. Viterbi Decoder

A block diagram of the proposed state-parallel Viterbi decoder is shown in Figure 3. The Viterbi decoder consists of two function blocks: ACS module and path memory (PM) module. The ACS module accomplishes most part of the Viterbi decoding algorithm such as the branch metric calculation, the add-compare-select and path metric update. The PM module stores survivor path information and outputs the decoded information bit.

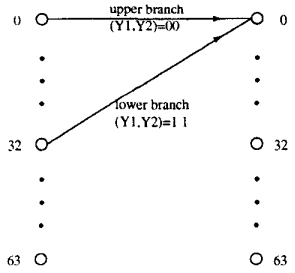

Figure 4: *Trellis of (2,1,7) convolutional code (only shows 2 input connections for state 0; the 126 other connections are not drawn).*

2.3. Add-Compare-Select

The proposed decoder shown in Figure 3 is a state-parallel design. It has 64 ACS processors operating in parallel, with each state having its own dedicated ACS processor. In one add-compare-select computation cycle, 64 decision bits are generated simultaneously, in contrast to a state-sequential decoder where only one ACS processor is implemented. This implies that the parallel architecture is a factor 64 faster than the equivalent state-sequential decoder, at the expense of 64 times larger area. Nevertheless. a compact implementation is still obtained by virtue of the analog architecture.

The add-compare-select operation can be clearly shown through the trellis. Only two connections are shown in Figure 4 for clarity. The ACS operation for state 0 will be discussed in detail as an example. The two connections in Figure 4 are two inputs to the node of state 0 from the previous state 0 and state 32.

In a hard-decision Viterbi decoder, and in the assumption of a memoryless channel, the metric can be defined directly as the inverse of the Hamming distance. Thus the survivor path is just the one with the smallest Hamming distance, or the biggest path metric. Path metric is the accumulation (sum) of previous branch metrics in the trellis. Branch metric is the inverse of the Hamming distance between the received code word (y1,y2) and the code word associated with the branch (Y1,Y2). It is defined by

$$BM = -[(y1 \oplus Y1) + (y2 \oplus Y2)] \qquad (1)$$

where "$\oplus$" is modulo-2 addition and "+" is normal addition.

For state 0, the upper branch $(Y1, Y2) = 00, BM_{\text{upper}} = -(y1 + y2)$, and the lower branch $(Y1, Y2) = 11, BM_{\text{lower}} = -(\overline{y1} + \overline{y2})$. Then the optimal path metrics are calculated recursively through the following add-compare-select operation, for given state 0:

Add:

$$\begin{aligned} PM_{\text{upper}} &= PM(0) + BM_{\text{upper}} \\ PM_{\text{lower}} &= PM(32) + BM_{\text{lower}} \end{aligned}$$

Compare:

$$D(0) = (PM_{\text{upper}} > PM_{\text{lower}})$$

Select:

$$PM(0) = \max\{PM_{\text{upper}}, PM_{\text{upper}}\}$$

where PM(n) denotes the path metric of state n.

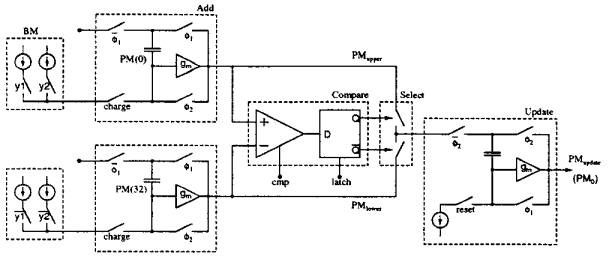

Figure 5: *Add-Compare-Select Simplified Circuit Diagram.*

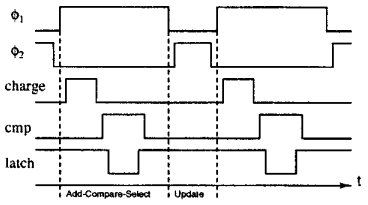

Figure 6: *Clock Diagram for the Add-Compare-Select Circuit.*

3. ANALOG VLSI IMPLEMENTATION

Figure 5 shows the block diagram of the implemented ACS cell, in the case of state 0. The corresponding clock diagram is given in Figure 6.

3.1. Branch Metric Calculation

Figure 7 shows the branch metric computation implemented with current-mode circuitry. Lateral PNP bipolar transistors are used for improved matching over pMOS transistors, in a standard digital CMOS process. The implemented circuit is shown in Figure 7 (a), which can be used either for digital hard-decision or for analog soft-decision inputs. In the analog case, it is assumed that voltage on the emitter logarithmically encodes the metric, such that the resulting collector current is proportional to the metric. The current is integrated on a capacitor over a fixed time interval, to accumulate the branch metric to the path metric. A digital soft-decision can be likewise implemented by extending the circuit to a D/A converter shown in Figure 7 (b).

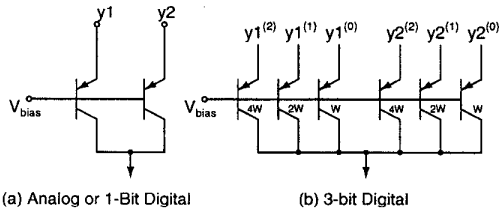

Figure 7: *Current-mode computation implementing the branch metric calculation (BMC) for both digital and analog hard-decision and soft-decision Viterbi decoders. (a) 2-transistor BMC circuit for digital hard-decision and analog soft-decision Viterbi decoders. (b) 6-transistor BMC circuit for 3-bit digital soft-decision Viterbi decoder.*

3.2. ACS

The ACS cell, Figure 5, combines the current-mode branch metric computation with switched capacitor techniques for the add, compare and select operations. The path metrics $PM(0)$ and $PM(32)$ are stored in form of charges on the capacitors. The survivor path metric is stored in the PM survivor unit for updating. Figure 6 shows the clock diagram for the ACS circuit. Φ_1 and Φ_2 are non-overlapping clocks. One add-compare-select-update operation cycle is completed in one clock period. After the branch metric is added into the path metric during the charge phase, the comparator gives the decision bit, the selector chooses the biggest metric which is sent to the PM survivor unit for temporary storage. During the Φ_2 phase, the metric update is performed.

3.3. Global Path Metrics Reset

To avoid overflow in the path metrics caused by the integrated accumulation of negative branch metric over time, the path metrics are have to be renormalized at each cycle by monitoring the largest of all metrics. This is achieved by finding the maximum path metric by means of a "winner-take-all" (WTA) circuit.

3.4. CMOS Circuit Implementation

Figure 8 shows the complete circuit diagram for one ACS cell (ACS0). Compact, single-ended CMOS circuits are used to implement amplifiers for the integrators and switched-capacitor blocks. The comparator is latched for high-speed operation.

With g_m denoting the transconductance of the amplifiers and C the capacitance of the path metric, the time constant of the system τ is mainly determined by C/g_m. As expected, high g_m and low C yield optimal speed and power dissipation, where C is constrained by noise and mismatch. Imprecision is an important consideration in the implementation of a system which is intended for use in error correction, so this is an important consideration in the design. We have formally analyzed the effect of analog imperfection on the accuracy of ACS computation. A conservative estimation shows when the combined effect of noise, nonlinearity and mismatch Δv is less than $V_{\text{range}}/10K(K-1)$, the probability of a wrong decision bit is extremely small and negligible for all practical purposes. For $K = 7$ and $V_{\text{range}} = 1V$, The tolerance is $\Delta v = 2.5mV$. To make thermal noise below $2.5mV$, $C = 10^{-15}F = 0.001pF$ is large enough in principle. This means we can achieve high-speed and low-power analog Viterbi decoders using compact CMOS circuits. In practice, the capacitor C is determined by considerations of switch charge injection noise, and mismatch. We found that the choice $C = 0.5pF$ gives good performance in terms of both the accuracy and efficiency of the implementation.

4. CHIP CHARACTERISTICS

The layout of the CMOS chip implementing the Viterbi ACS is shown in Figure 9. The floorplan is symmetrical around the center vertical axis, with units ACS0 through ACS31 placed on the left side, and ACS32 through ACS63 placed on the right side of the chip. The trellis connection network is in the center. We found this to be the most efficient and convenient way to layout the massive shuffle-exchange type interconnection network defined by the trellis. The connections take less than 14% of the total core area.

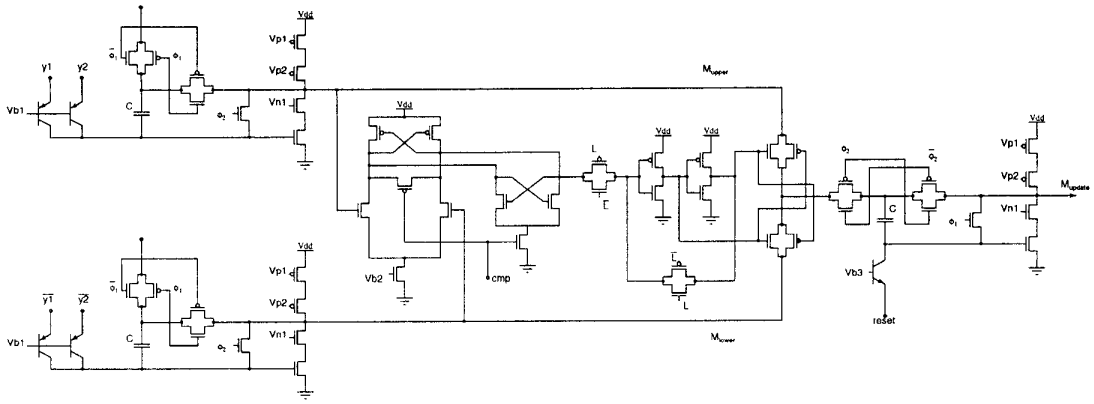

Figure 8: *Complete Circuit of the Add-Compare-Select Cell (ACS0).*

Table 1: Chip Characteristics

Technology	$2.0\mu m$, 2-metal n-well CMOS
Convolutional code	$(2, 1, 7)$, rate=$1/2$,$K = 7$
Generation polynomial	$(171, 133)$ (octal)
Input level	analog soft decision
Core size	$1900\mu m \times 1900\mu m$
Die size	$2220\mu m \times 2250\mu m$
Transistor counts	$4.5K$
Supply voltage	$5V$
Power consumption	$7.65mW$
Decoding Speed	$500Kbps$

The ACS chip tested functional in correctly decoding ideal (clean and uncontaminated) test sequences, for decoding speeds up to the limit of the teststation instrumentation used in the experiments. Results are summarized in Table 1. Further experiments are currently underway to characterize the error correcting capability of the chip under noisy and contaminated analog inputs.

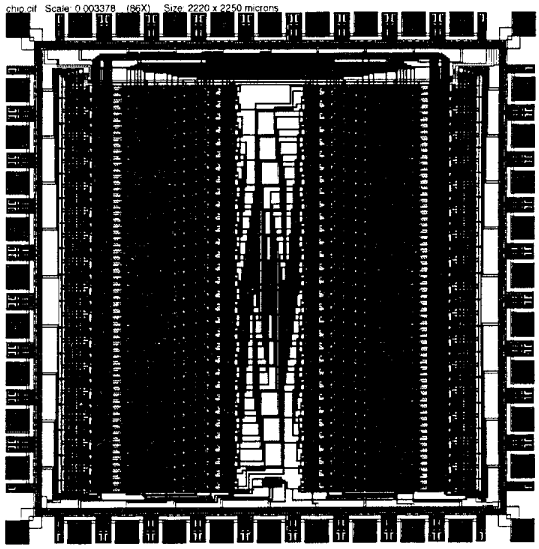

Figure 9: *Layout of the 64-state analog ACS module chip.*

5. CONCLUSION

We have presented an area-efficient analog VLSI architecture for the ACS part of a state-parallel Viterbi decoder, implementing a (2,1,7) convolutional code as commonly used in deep-space communications. A complete 64-state ACS module has been integrated onto a MOSIS $2\mu m$ TinyChip, and has been fabricated and tested. This analog Viterbi ACS VLSI clearly demonstrates significant savings in silicon size and power consumption compared to conventional digital Viterbi decoders. It appears to be the first long constraint-length ($K \geq 7$) analog VLSI Viterbi decoder with state-parallel ACS architecture. To the best of our knowledge, it has the lowest power consumption and smallest core area in its class.

6. REFERENCES

[1] G. David Forney, Jr., " The Viterbi Algorithm", *Proceedings of the IEEE*, vol. **61**, No. **3**, pp 268-278, March, 1973.

[2] Gerhard Fettweis and Heinrich Meyr, "High-Speed Parallel Viterbi Decoding: Algorithm and VLSI-Architecture", *IEEE Commun. Magazine*, , pp 46-55, May, 1991.

[3] Shuji Kubota, Shuzo Kato and Tsunehachi Ishitani, "Novel Viterbi Decoder VLSI Implementation and its Performance", *IEEE Trans. on Communications*, vol. **41**, No. **8**, pp 1170-1178, August, 1993.

[4] Inyup Kang, Alan N. Willson Jr., "Low-Power Viterbi Decoder for CDMA Mobile Terminals", *IEEE J. of Solid-State Circuits*, vol. **33**, No. **3**, pp 473-482, March, 1998.

[5] Anthony S. Acampora and R. P. Gilmore, "Analog Viterbi Decoding for High Speed Digital Satellite Channels", *IEEE Trans. on Communications*, vol. **COM-26**, No. **10**, pp 1463-1469, October, 1978.

[6] Richard R. Spencer, "An Integrated Analog CMOS Viterbi Detector for Digital Magnetic Recording", *IEEE J. of Solid-State Circuits*, vol. **28**, No. **12**, pp 1294-1301, December, 1993

[7] Mohammad H. Shakiba, David A. Johns and Kenneth W. Martin, "An Integrated 200-MHz 3.3-V BiCMOS Class-IV Partial-Response Analog Viterbi Decoder", *IEEE J. of Solid-State Circuits*, vol. **33**, No. **1**, pp 61-75, January, 1998.