CMOS Camera With In-Pixel Temporal Change Detection and ADC

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***Abstract*—An array of 90 × 90 active pixel sensors (APS) with pixel-level embedded differencing and comparison is presented. The nMOS-only 6T 2C 25 μm× 25 μm pixel provides both analog readout of pixel intensity and a digital flag indicating temporal change at variable thresholds. Computation is performed through a pixel-level capacitively coupled comparator which also functions as analog-to-digital converter. The chip, fabricated in a 0.5 μm 3M2P CMOS, process consumes 4.2 mW of power while operating at 30 fps. Change sensitivity is 2.1% at an illumination of 1.7 W/cm^2. Gating of raster-scanned pixel output by change detection typically produces a 20-fold compression in the data stream, depending on image conditions and reconstruction quality set by the change detection threshold.**

***Index Terms*—CMOS image sensor, computation-on-readout (COR), delta-difference sampling (DDS), pixel-level analog-to-digital conversion (ADC), temporal difference imager.**

I. Introduction

WHILE recent advancements in CMOS technology have allowed for the realization of image sensors with processing elements on a single chip, the efficient transmission of video rate data still presents a challenge, especially in cost and power constrained environments. Traditional video compression techniques rely on complex algorithms to achieve the data reduction rates needed to operate over a low-bandwidth network, making it impossible to operate on low-power electronics or to be implemented on the small areas available for computation at the focal plane.

The need for networked, low-bandwidth yet high-quality imaging has become more urgent in recent years, particularly in the form of surveillance systems. Ideally a remote monitoring system would operate across a rapidly deployable ad hoc wireless network. We propose an image sensor suited for such a scenario by incorporating many of the necessary data processing elements into the focal plane. To reduce the data output rate, a change detection circuit is built into the pixel, providing a wake-up on motion capability that compresses the data stream and minimizes the power consumption. At the same time it is also necessary to maintain a high image quality by reducing the impact of the processing elements on the pixel's area and fill factor. To that end, we use a computation-on-readout (COR) approach that distributes the processing circuits between the three extra transistors in the pixel and circuits at the column level.

The imager is a 90 × 90 array of nMOS-only pixels that includes both the three-transistor APS [1] and a three-transistor, two-capacitor comparator. In the change/motion detection (C/MD) mode, the pixel stores the previous brightness level and provides an output of the intensity change direction only when motion is detected. A FIFO stores the address and event type alongside the analog value of the pixel signaling a motion event. Previous implementations for temporal intensity transient sensing are either significantly larger and/or more complex than the proposed architecture [3], [4] (28, 13 transistor pixel, respectively), do not provide rectified ON and OFF output channels [4]–[6], or do not provide an analog image output alongside the detection indicator [3], [5], [6]. Unlike previous change-coding imagers, intensity change events are used to gate data transmission, leading to efficient transmission of task relevant information.

In addition to outputting the intensity change, full images can be extracted from the embedded pixel-level comparator, eliminating the need for an external ADC and further simplifying the sensor design. Pixel-level ADCs offer several significant advantages [9], [10] since it eliminates the necessity of high-speed converters and outputting analog signals to external circuitry in addition to offering higher dynamic range [12], [14]. An image sensor operating autonomously must be able to adapt and function across a multitude of ambient lighting conditions. Whereas biological systems enjoy upwards of 200 dB of dynamic range, typical CMOS image sensors can only achieve around 60 dB. Successful approaches to overcoming this limitation involve pixel level processing using variable rate integration time [12], taking multiple exposures [11] or outputting pixel saturation time [14], instead of a voltage. Biologically inspired imagers [13] have emulated octopus retinal systems by again using pixel level processing to output a time encoded intensity value, achieving wide dynamic range operation.

Unlike previous pixel-level ADC designs, the proposed architecture operates with a minimum of electronics, sharing the same circuits as the intensity change detection. Using the pixel-level comparator and taking advantage of the photocurrent integration ramp, it is possible to operate the pixel as a single slope

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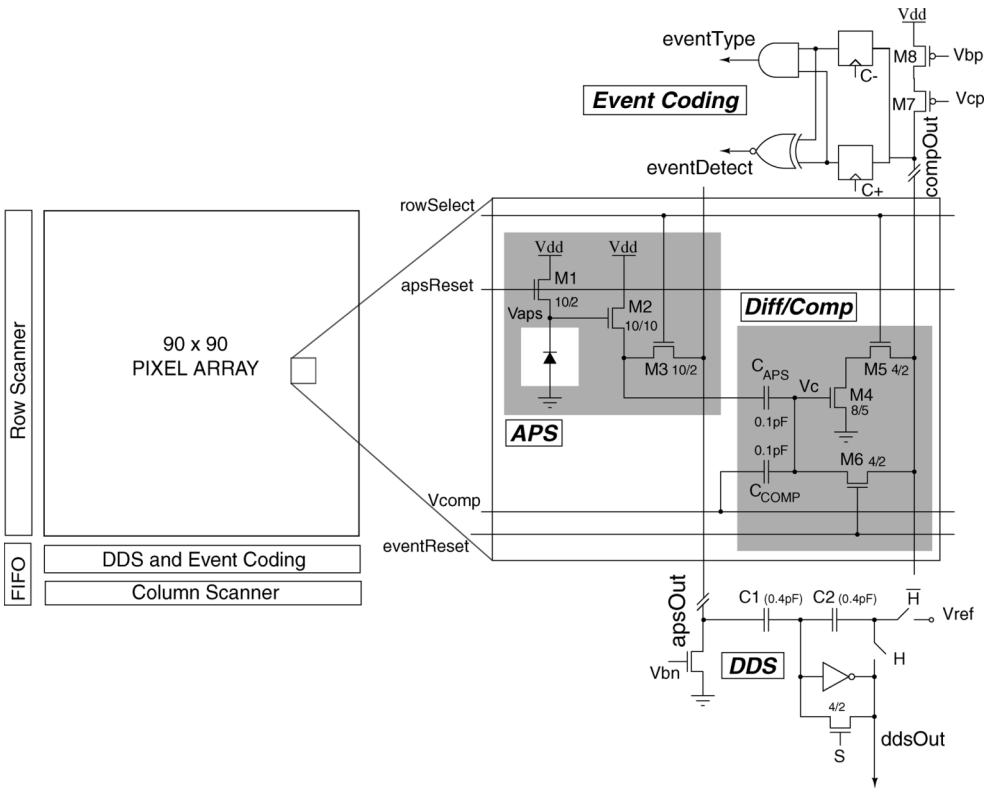

Fig. 1. Chip system diagram and circuit schematics.

ADC. Image quality is noticeably superior to using board level external ADCs in both spatial resolution and dynamic range while reducing the complexity of the system.

The basic operation of the CM/D and pixel-level ADC has been described at previous conferences [16], [17]. This paper provides a complete analysis on the chip's operation and performance by examining the effects of noise on computation error, image quality and speed, and the limits of the architecture.

II. Circuit Description

Overall chip layout and organization is shown in Fig. 1. All computations are performed following a column parallel architecture. Each pixel includes an APS, sampling capacitor and circuitry implementing part of the comparator. At the edge of the array, column level circuits include the delta difference sampling (DDS) [1] circuit for image output, the comparator's active load and data latches. Image readout is facilitated by serially clocked row and column scanners.

A. APS Imager

At its core, the chip contains an array of 90×90 APS pixels that include the photodiode and the essential circuitry of the pixel level comparator. The pixel is based on the basic three transistor configuration [1] containing a photodiode, reset switch (M1), output buffer (M2), and access switches (M3, M5). The common-source amplifier used as the comparator includes the input (M4), the pMOS active load (M7, M8) and comparator reset (M6). Distributing the pMOS transistors to the column level eliminates the need for a well and maximizes both pixel density and fill factor. It also reduces power by a factor asymptotically equal to the number of rows, since only a single comparator is supplied current for each column.

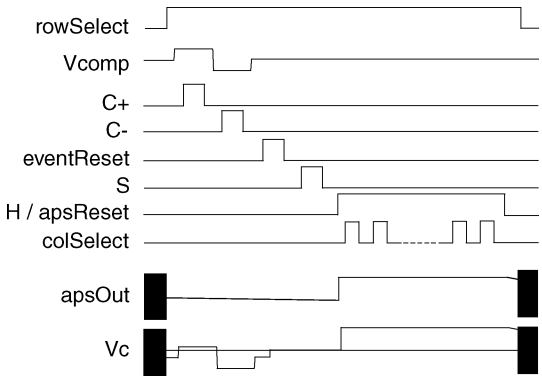

Fig. 2. Timing diagram for DDS readout and intensity change detection.

Analog image readout is accomplished by column level circuits implementing delta-difference sampling [1] (DDS) for fixed pattern noise (FPN) suppression. Closing "S" samples the integrated APS voltage $V_{\rm aps}$ across C_1 and C_2 with respect to an external voltage $V_{\rm ref}$. Closing "apsReset" and opening "S" establishes feedback across the common-source amplifier through C_2, subtracting the pixel reset voltage from the stored image to output the difference between pixel reset and the integrated voltage (Fig. 2). The performance of this design is limited by the mismatch between its capacitors resulting in column-wide FPN artifacts. DDS output assuming infinite amplifier gain is

$$\mathrm{ddsOut} = V_{\rm ref} + \frac{C_1}{C_2}(V_{\rm reset} - V_{\rm aps}). \tag{1}$$

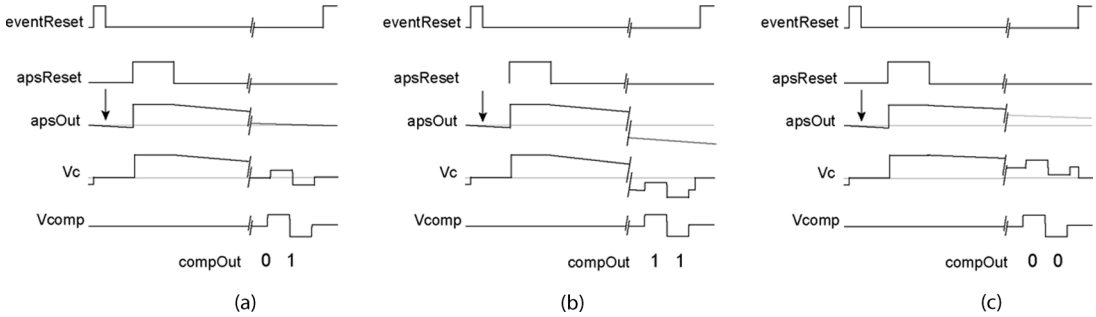

Fig. 3. Comparator timing and output for ADC for (a) pixel exhibiting no brightness change, (b) increasing intensity, and (c) decreasing intensity.

B. Pixel-Level Comparator

In addition to the standard APS circuits, the pixel utilizes a cascoded common-source amplifier as a comparator. Closing M6 samples the voltage difference between the output of the APS pixel and the threshold of the amplifier across $C_{\rm aps}$ and the voltage between $V_{\rm comp}$ and the threshold across $C_{\rm comp}$. The input impedance of M4 is very high and opening M6 leaves the input of the comparator V_c floating which conserves the charge on both capacitors. Voltage excursions at the APS and $V_{\rm comp}$ transfer to V_c via a simple capacitive voltage divider

$$\Delta V_c = \frac{C_{\rm aps}\Delta V_{\rm aps} + C_{\rm comp}\Delta V_{\rm comp}}{C_{\rm aps} + C_{\rm comp}}. \tag{2}$$

Since both capacitors are designed to be equal, the effective input is just the average of the two changes, each with weight 1/2. By conserving the charge across the capacitors it is possible to use this amplifier as a comparator between the voltage changes in each input. Resetting the circuit by closing the feedback loop sets the input of the comparator to its switching point. A change at one input immediately forces the comparator output to assume a logic high or low, because of the high gain (50 dB). A comparison is made by bringing the other input, $V_{\rm comp}$, in the opposite direction. If the change in the second input is greater than the first in magnitude, the comparator will be forced to again switch states.

Although many comparators have been implemented at the pixel level, this architecture employs the minimum of area overhead since only three nMOS transistors and two capacitors are needed in addition to the standard elements in an APS.

C. Change Motion Detection

Temporal intensity change variations are detected by comparing the brightness of the current frame against that of the previous. The cycle begins at the end of photocurrent integration with the comparator reset, sampling the APS voltage across $C_{\rm aps}$. The switch is then opened followed by pixel reset which then pulls the comparator input high, resulting in a "0" output. As the photocurrent is integrated, the voltage at the comparator input begins to drop in proportion to the incident light at the pixel. Should the photocurrent in the current frame be greater than the previous, then the comparator input will drop below the switching point resulting in a "1" output. Similarly, less photocurrent in the frame will cause the input to remain above the switching point for a "0" output.

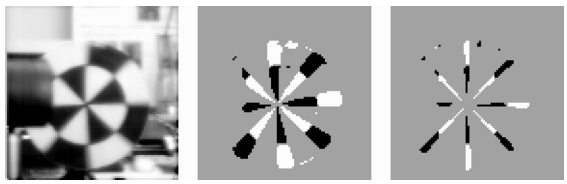

Fig. 4. Fast and slow rotating flywheel edges.

While this operation results in a direct, brighter/darker change output for each pixel, it does not define a state for no pixel change since the comparator output is a single bit. In situations where the change in light is very small or nonexistent, noise and mismatch begin to dominate the comparison, thereby producing spurious errors. For better control over the change detection, it is desirable to have a user-defined threshold below which temporal variations are rejected.

Taking advantage of the second control input at the comparator, $V_{\rm comp}$ is moved by $\pm\Delta V_{\rm reject}$ during the readout process (Fig. 3). The two comparisons with relative thresholds $+\Delta V_{\rm reject}$ and $-\Delta V_{\rm reject}$ are performed in sequence by presenting a positive then negative step in $V_{\rm comp}$ in sequence, as shown in Fig. 3. For two images with integrated APS voltages within $\pm\Delta V_{\rm reject}$ of each other, the comparator will have different outputs. If the difference in the pixel brightness is greater than the rejection band, then the comparator will output the same value since the control voltage is insufficient to cause the input to cross over the amplifier's switching threshold.

Two logic gates are used to encode the comparator results for output to the chip's pins. The XNOR of the comparator output indicates the presence of change events since it has a logic high when both computations have the same result. Likewise the NAND gate indicates the direction of change, "1" for current frame brighter and "0" for current frame darker.

As a visual demonstration of the temporal change sensitivity, a rotating, radial and concentrically alternating flywheel pattern, placed in a cluttered static environment was presented to the imager. In Fig. 4 from left to right, are the image, the detected edges with the flywheel rotation at three revolutions per second, and its edges at one revolution per second. Note that the static background does not trigger any detection.

Data for the CM/D circuitry is shown in Fig. 5. For an incident light power of 1.7 $\mu{\rm W}/{\rm cm}^2$, various combinations of uniform intensity variation and rejection band thresholds are plotted. Higher rejection band thresholds result in lower change

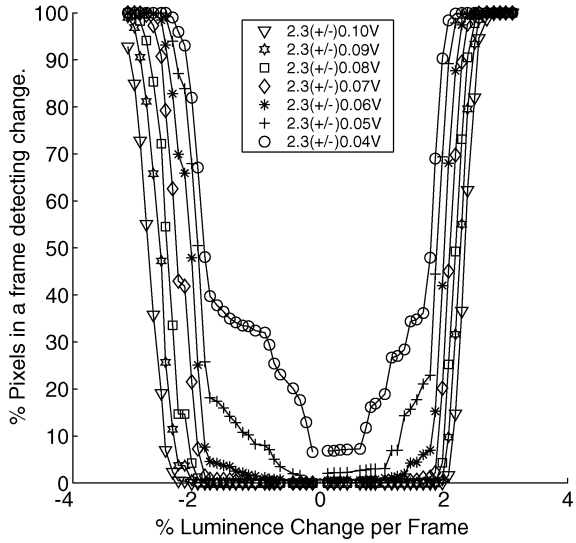

Fig. 5. Intensity change sensitivity.

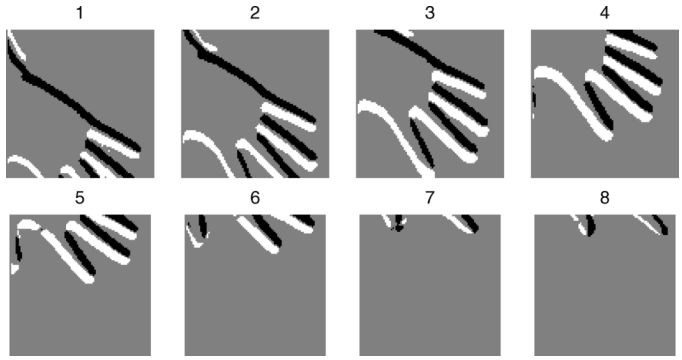

Fig. 6. A moving hand displayed every five frames.

sensitivity. Reducing the rejection band increases sensitivity, but is more susceptible to noise and mismatch effects.

The variability in the pixels responding to intensity changes is due to the temporal noise and FPN mismatches. A minimum rejection band of ± 50 mV is needed to eliminate random fluctuations in the change detection output. Above ± 50 mV, a constant mismatch error is observed for all thresholds, mainly arising from gain errors in the pixel's comparator.

D. Change Event Based Image Coding

Frame difference encoding is widely used as a method for video compression. Typical video sequences, especially in a surveillance context, are comprised of a few moving objects superimposed on a static background. Transmitting only the areas that undergo motion results in a large compression gain. Normally, this is done by subtracting the current frame from the previous, either directly or with motion compensation, and transmitting the much reduced residual information.

In the most basic form, the imager provides a processed output indicating the presence and direction of change as the array is scanned out (Fig. 6). Since temporal differences arise in moving areas with nonzero spatial gradients, the change output provides a picture of the boundaries of objects in motion. It is also possible to take advantage of this output for target tracking. The difference output can be used to segment and track the motion of edges in time.

To perform full video compression, the location of changed pixels is combined with the actual intensity. Reporting only changed pixels is a form of difference encoding, reducing the temporal redundancy in the data. Although the lack of feedback in the encoder control loop results in steady-state error accumulation, this is not a significant problem, and is alleviated by sending keyframes, which is a necessity in any video coding scheme.

In Fig. 7, a video of a moving person is shown. Following the initial key frame, image updates occur by transmitting *only the values of pixels which report a temporal change* of a given positive and negative threshold. Although an error trail is seen in the areas which undergo motion, the image still remains usable. In this low motion type example, an average of less than 5% of pixels was updated, resulting in a significant bandwidth reduction. Typically, the PSNR of the reconstructed image is highly dependent on the characteristics of the video, and is not meaningful since the goal of the image sensor is to alert and direct attention upon scene changes. However in this example, the PSNR remains above 27 dB across 30 frames of pixel change updates following a keyframe.

A variety of data coding methods can be used to transmit the residual data. The simplest form is by using the internal FIFO which stores the address of the change and an updated analog value of the pixel's brightness. Changes are sent only as necessary, and all the decision making and data processing are located on the imager. In addition, the de-correlated nature of the resulting temporal difference can be exploited through run length coding. The only extra hardware necessary would be an external counter, which can also easily be incorporated into the chip itself. Finally, he architecture is not limited to pixel based frame updates. A temporally compensated macroblock based approach can also be used, for example, by DCT coding the image and using the change detector as an analog memory. Regions that do not undergo change can either be sent progressively higher frequency coefficients or not transmitted at all. Blocks that do report a significant change would be flagged for a complete refresh.

In effect, the image sensor can be used to perform motion compensated video coding, but with an absolute minimum of hardware and complexity overhead. The pixel level change detection avoids the necessity of external digital processing.

E. Pixel-Level ADC

As previously mentioned, the C/MD circuitry is functionally a 1.5-bit ADC of relative changes in the APS. Slight alterations in the timing of the comparator will output the pixel's change from the initial reset value, rather than the change from the previous frame (Fig. 8). APS and comparator reset now occur simultaneously, sampling the initial reset voltage across the control capacitors. Photocurrent integration immediately brings the input of the comparator below the threshold point resulting in a "1" output. At readout, V_{comp} is used to raise the input by an amount $\Delta V_{\mathrm{thresh}}$. Photocurrents large enough to cause an APS voltage drop of greater than $\Delta V_{\mathrm{thresh}}$ will allow the comparator to remain in the "1" state. For lower light intensities, $\Delta V_{\mathrm{thresh}}$

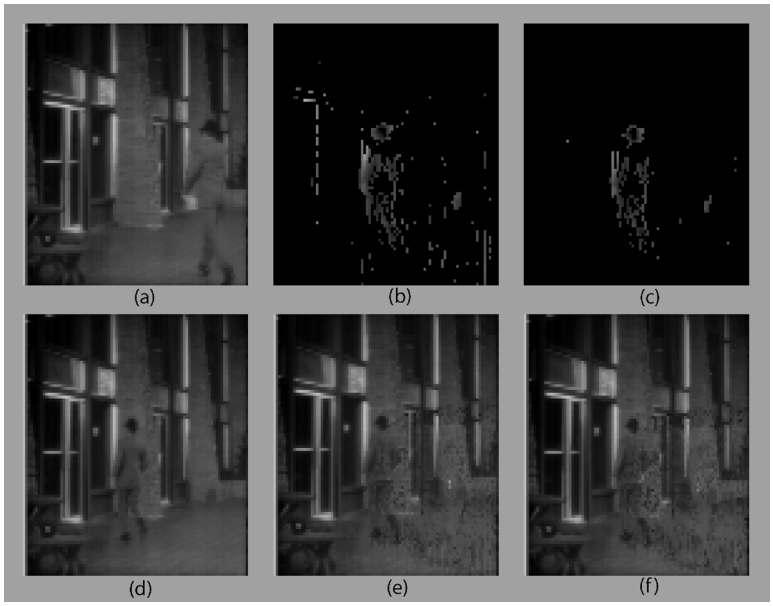

Fig. 7. Reconstruction of video from updating only pixels that detect a change. Images (a) and (d) show the first and last frame of the video. Images (b) and (c) show the pixels that are updated with rejection thresholds of 100 mV and 150 mV, respectively. Images (e) and (f) are the reconstructed final frames.

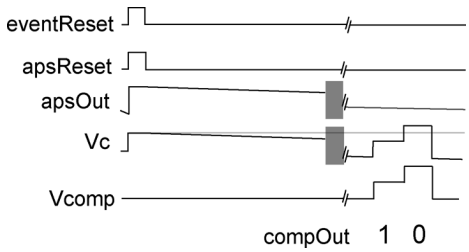

Fig. 8. Comparator timing and output for the ADC showing the use of two different thresholds by varying $V_{\rm comp}$.

is large enough such that the input is brought back above the switching point resulting in a "0" output. It is important to note that this mechanism, unlike the column level DDS readout, is still performing a correlated double sampling—*the ADC samples the initial reset value and quantizes the voltage change from reset within the same integration cycle.*

At this point, the pixel-level comparator is operating as a very coarse 1-bit ADC of the photocurrent, which is insufficient to construct any meaningful image. Taking advantage of the fact that two latches are available, it is trivial to perform two threshold computations per frame readout by simply using two different values for $\Delta V_{\rm thresh}$ in the same manner as the change detection. However this only results in one more quantization step for a 1.5-bit ADC. More resolution is needed to obtain images with less visual artifacts.

A form of oversampling can be used to significantly increase the resolution. Because photocurrent integration generates a voltage ramp, it is possible to construct a single slope ADC. In this scheme the APS is not reset after each frame but allowed to integrate across m frames resulting in $\log_2 3m$ bits of resolution since each frame resolves three quantization steps. The output is a pulsewidth modulated signal with three intensity values. Averaging the pulse over the integration period and decimating produces the final high-resolution output, albeit at a much reduced frame rate.

The single slope effectively implements a form of variable time integration as well as electronic exposure control [13]. Readout is in a bit serial pattern where each frame represents two quantization intervals. Large photocurrents are immediately captured in the initial frames, and smaller ones are given multiple frame periods to integrate past the comparator threshold. Electronic exposure control is facilitated by changing the threshold used for the comparator. Lower thresholds will exhibit greater sensitivity to smaller photocurrents, whereas higher thresholds prevent saturation in bright light sources (Fig. 9). Combining these two methods allows the imager to operate in wide ambient lighting conditions without the need for a mechanical shutter control or frame rate change (Fig. 10).

In addition, a ramp ADC can also be implemented in the pixel by increasing $V_{\rm comp}$ at readout and recording the point where the comparator switches states. However, since a single row is read out multiple times, an unusually long integration period is needed. This eliminates the variable time integration and programmable threshold control of the single slope ADC and results in images inferior to both the single slope and analog outputs.

To characterize the ADC, the image sensor is subjected to an arbitrary amount of constant illumination. The transfer curve is obtained by varying the comparator's threshold. The ADC is operating at 6 bits with an integrating time of 8.17 ms per frame. Recalling that the ADC is a time encoded representation of the photocurrent intensity,

$$\mathrm{ADC} = \mathrm{TMAX} - \frac{C_{\rm diode}}{i_{\rm photo}} V_{\rm thresh} \tag{3}$$

where TMAX is the maximum integration time for the converter, the ADC output should be linearly proportional to the

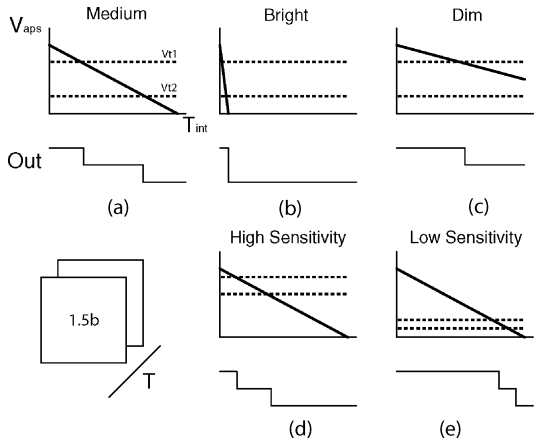

Fig. 9. The ADC is read through successive 1.5 bit frames. Comparator output is a 3-level pulsewidth modulated signal corresponding to the photocurrent intensity. The top row illustrates ADC output signals for a medium (a), large (b) and small (c) photocurrents. Thresholds can be moved to change the ADC transfer characteristics to favor darker (d) or brighter scenes (e).

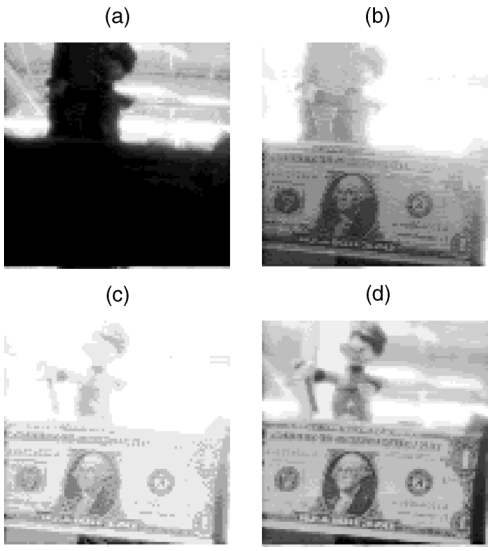

Fig. 10. Electronic exposure control. The foreground is unlit against a bright background in (a). Adjusting the threshold to the high sensitivity setting resolves the dark portions (b). In the bottom pictures the foreground is now lit against the same bright background (c). Correct exposure can be accomplished by resetting to the low sensitivity setting (d).

threshold of the comparator (Fig. 11), assuming linear photocurrent integration.

For the usable range of the APS, the threshold versus ADC code output should be related by a constant factor of the photodiode capacitance divided by the photocurrent. From the plot, the sensor has a integration range of about 1 V from pixel reset, and the overall transfer curve of the ADC is largely linear. In addition, this also illustrates the programmable exposure feature of the pixel level ADC. The conversion gain from photocurrent to ADC output codes is set by the adjustable threshold of the comparator.

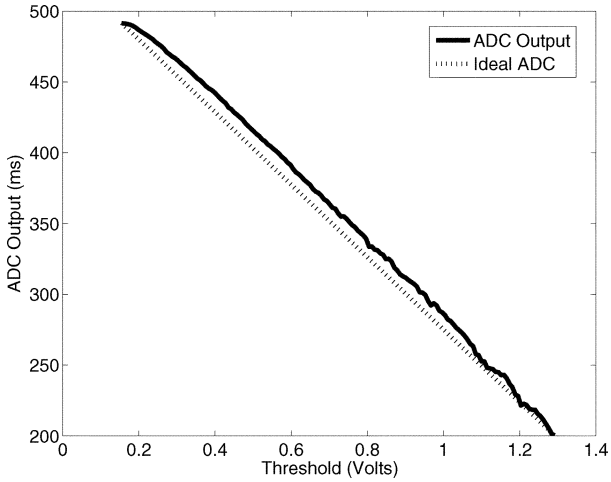

Fig. 11. ADC transfer curve.

III. Sensitivity and Noise Analysis

A. Pixel and Comparator

The total area of the photodiode is 1.1 μm^2 with an integrating capacitance of 39 fF, setting the gain from electrons to photodiode voltage at 4.1 μV/e$^-$. For a quantum efficiency of 20% with incident light at a wavelength of 600 nm, the resulting ratio between light irradiation and photocurrent is 100 fA per μW/cm^2. Assuming linear photocurrent integration

$$V_{\rm aps} = \int_0^t \frac{i(t)_{\rm photo} dt}{C_{\rm diode}} \tag{4}$$

the total conversion from light to voltage at the integrating node becomes 26 mV per millisecond of integration under a constant illumination of 10 μW/cm^2.

Following the photocurrent integration, a source-follower is used as a buffer to isolate the photodiode from the column line, with a gain dependent on the biasing current and output impedance of the current source

$$V_{\rm col} = V_{\rm aps} \frac{g_{m2} r_{o4}}{1 + g_{m2} r_{o4}} \tag{5}$$

which is calculated to be .74. At this point, the APS voltage can be either read out directly via the DDS circuit or used for computation in the pixel-level comparator. The output of the APS source-follower is AC-coupled to the comparator input via a capacitive divider with equal values.

$$V_c = V_{\rm col} \frac{C_{\rm comp}}{C_{\rm aps} + C_{\rm comp}} \tag{6}$$

$$\approx \frac{V_{\rm col}}{2}. \tag{7}$$

A common-source amplifier with a current source load has a high voltage gain at the threshold on M4, $g_{m4} r_{o4}$. Since the amplifier's output must switch from near rail-to-rail, the large signal gain is considered. A total voltage excursion of 4 mV to either side of the switching point is needed to drive the output to the appropriate logic threshold, or $A_v = 370$.

The control input is also capacitively coupled to the comparator input through the same network

$$|\Delta V_c| = \pm \Delta V_{\text{comp}} \frac{C_{\text{aps}}}{C_{\text{aps}} + C_{\text{comp}}}. \tag{8}$$

The overall expression for the input of the comparator for a given change in light intensity, ΔI_{photo}, and shift in ΔV_{comp} can be written as

$$V_o = \frac{1}{2}\left(\frac{\Delta I_{\text{photo}} t_{\text{int}}}{C_{\text{diode}}}(0.74) - \Delta V_{\text{comp}}\right)(370). \tag{9}$$

To assess the overall sensitivity of the change detection system, it is necessary to find the equivalent minimum voltage change at the photodiode's integrating node to cause a comparator change event. Assuming noiseless conditions, the voltage difference between two frames at the comparator input must be greater than $4\text{ mV} + |V_{\text{reject}}|/2$ in order for the column latches to register a change. Referring it back to the photodiode line by dividing by the capacitive ratio and the source-follower gain

$$\Delta V_{\text{aps}} > 10.8\text{ mV} + V_{\text{reject}}. \tag{10}$$

For the single slope ADC mode, a similar figure can be obtained. A threshold crossing occurs if

$$\frac{I_{\text{photo}} \Delta t_{\text{int}}}{C_{\text{diode}}} > 10.8\text{ mV} + V_{\text{thresh}}. \tag{11}$$

B. Temporal Noise

The imager uses the well-understood and characterized [1], [15] 3-T design including the photodiode, reset switch, buffer and access switch. The total temporal noise contribution from the APS, mostly a result of shot noise is 1.38 mV rms at 1 pA of photocurrent. The source-follower also adds 263 μV rms of thermal noise to the source of M2.

The final noise source in the computation pathway is from the pixel's cascoded amplifier. Thermal noise current is computed using the model in Fig. 12. The active load is comprised of a cascoded current source for high gain, and the output resistance is considered infinite in comparison to the resistance of the nMOS branch. The noise power contribution at the output from the pMOS current source is

$$< V_{\text{cur}}^2 > = \frac{2}{3}\frac{kT}{C_{\text{col}}}(g_{m7} + g_{m8})(r_{o4} + r_{ds5}). \tag{12}$$

For the access switch transistor

$$< V_{m5}^2 > = \frac{kT}{C_{\text{col}}}\frac{r_{ds5}}{r_{ds5} + r_{o4}}. \tag{13}$$

Lastly the input transistor's thermal noise contribution is

$$< V_{m4}^2 > = \frac{2}{3}\frac{kT}{C_{\text{col}}}\frac{r_{o4}^2 g_{m4}}{r_{o4} + r_{ds5}}. \tag{14}$$

Referred to the comparator input, the comparator's noise contribution, 12 μV rms, is negligible.

More significantly, the comparator introduces additional kT/C thermal noise components at reset and when the voltage at the V_{comp} is switched during computation. At comparator reset, C_1 and C_2 appear in parallel for a total of 2×100 fF with an rms noise voltage of 144 *uV*. During computation, V_{comp} is switched from its initial value to two different thresholds before being switched back to its nominal value. During this operation C_1 and C_2 form a series capacitance (50 fF) with respect to V_{comp}. The kT/C noise added to V_c can be expressed as

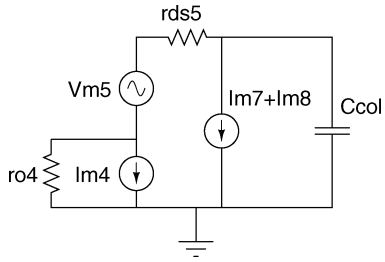

Fig. 12. Small-signal noise model for pixel comparator.

$$< V_c^2 > = 3\left(\frac{1}{2}\right)^2 \frac{kT}{50\text{ fF}} \tag{15}$$

since V_c is divided by the two capacitors and three switching operations take place per computation. The rms noise voltage is 250 μV per computation and is not a significant figure for the change detection mode, in light of the FPN mismatch. However, for the pixel-level ADC, where multiple frames are readout per complete image without resetting node V_c, this noise accumulates and presents a fundamental limit on the resolution for this type of ADC architecture. Independent of other noise sources and integration length, the uncertainty from comparator operation in this implementation becomes comparable to the LSB of the ADC at approximately 9 bits of resolution.

To assess the impact of temporal noise in the pixel, it is convenient to refer all of these noise sources to the comparator input through the transfer functions in the previous section. The initial kT/C are reset can be omitted since it represents and offset and the comparator performs CDS by quantizing the change from the initial reset value. The noise power at the comparator input can be expressed as

$$< V_{\text{noise}}^2 > = \left(\frac{1}{2}\right)^2 ((.74)^2\left(\frac{I_{ph}\Delta t_{\text{int}} q}{C_{\text{diode}}^2}\right) + \tag{16}$$

$$(263\text{ uV})^2) + N_f(250\text{ uV}^2) \tag{17}$$

where N_f is the number of comparator operations per image (one for change detection and multiple for ADC).

For the imager operating the comparator in change detection mode, it is shot noise that dominates terms of temporal noise. Using the previous conditions for photocurrent, a typical noise rms voltage is, 774 μV with $N_f = 1$ in change detection mode. For the pixel-level ADC, the comparator kT/C becomes more significant than shot noise for more than 10 computations per image (5 bits of resolution).

Although $1/f$ noise is also a contributing factor, it is assumed to be small in comparison, especially since much of it can be removed through CDS. It is important to note, however, that since the comparator input node is also capacitively coupled to the board level through an input pin, care must be taken to ensure that noise from the board level is not transmitted to the pixel.

C. Additional Noise Sources

Aside from the fundamental temporal noise in the circuit, spatial FPN is a problem in CMOS imagers, since manufacturing mismatches are unavoidable. Aside from the expected FPN sources from the photodiode and readout circuits in a standard APS, the comparator introduces a significant component of FPN. Mismatches arise at both the column and pixel level.

Manufacturing variations in the photodiode, control capacitors and the transistors in the comparator result in pixel level mismatches. Of these sources, the offset mismatch from the thresholds of M1 and M4 are most innocuous since it sets the initial conditions for the pixel. Since the comparator is only looking at the change from reset, it performs CDS and subtracts this error.

More significant are gain errors at the pixel which occur due to mismatches between $C_{\rm aps}$ and $C_{\rm comp}$ inside a pixel since they cannot be removed through subtraction. A deviation in the ratio of the two capacitors directly changes the gain from the APS to the comparator input. It also likewise changes the gain from $V_{\rm comp}$ to V_c. It is easy to analyze the effect of a capacitor mismatch. Recalling the expression for the capacitive divider

$$V_c = \frac{C_{\rm aps}}{C_{\rm comp}+C_{\rm aps}}\Delta V_{\rm comp} + \frac{C_{\rm comp}}{C_{\rm comp}+C_{\rm aps}}\Delta V_{\rm aps}, \quad (18)$$

and differentiating with respect to $C_{\rm comp}$

$$\frac{dV_c}{dC_{\rm comp}} = \frac{(\Delta V_{\rm aps}-\Delta V_{\rm comp})C_{\rm aps}}{(C_{\rm aps}+C_{\rm comp})^2} \quad (19)$$

and $C_{\rm aps}$

$$\frac{dV_c}{dC_{\rm aps}} = \frac{-(\Delta V_{\rm aps}-\Delta V_{\rm comp})C_{\rm comp}}{(C_{\rm aps}+C_{\rm comp})^2} \quad (20)$$

gives the voltage error at the comparator input for a change in each capacitor. To estimate the worst case scenario for the entire array, the rms equivalent noise value is calculated for the comparator input by taking the square root of the squares of the two preceding equations. In change detection mode a estimated value of 200 mV is used for $\Delta V_{\rm aps}$ with a threshold of ± 80 mV corresponding to an rms noise value of 424 μV for each femto-Farad of mismatch in the capacitors.

Switch injection and leakage are the two final sources of error. Switch injection occurs through M3 which connects and disconnects the pixel's source-follower from its active load. Leakage is a function of light intensity. In bright scenes, the charge on the control capacitors is lost due to the diodes on M2, M3 and M6 becoming active, and special care must be taken to shield these diodes.

D. Noise Measurements

The image sensor was again irradiated by a constant non-saturating light source across the array to compute the FPN for the pixel-level ADC. Over a thousand samples were acquired to eliminate temporal noise. Dividing the standard deviation of the pixel values by the maximum, the FPN is calculated to be 1.5%. To eliminate the irregularities from the edges of the array, a border of 10 pixels was cut from each side before computing the FPN.

It is now useful to refer the FPN to a noise voltage source inside the pixel. The 1.5% FPN corresponds to an rms noise value of 0.65LSB at 6 bits. The comparator threshold was set at 683 mV setting a LSB at 10.7 mV resulting in an rms noise value of 6.9 mV at the pixel. To verify the noise measurements between the change detection and ADC modes, the peak-to-peak noise value is used instead of the rms. Under constant illumination, the difference between the maximum observed ADC value and the minimum is 4 LSB or 42.6 mV, which matches the 50 mV minimum rejection band necessary to eliminate spurious comparator threshold readings.

For comparison purposes, the temporal and FPN noise of the column level DDS sampling circuits are also computed in a similar fashion, but digitized with high-resolution external ADCs. After acquiring thousands of samples, the temporal noise in the observed video output is computed to be about 1 mV rms. The FPN in the DDS is mainly a function of column level mismatches resulting in visible banding artifacts with a total FPN of 0.5% at 30 fps. However, it is important to note that the lower FPN number is also partially due to spatial low-pass filtering due to the slow response of the readout circuits in the analog video output.

E. ADC Resolution and Dynamic Range

The dynamic range of the ADC can be defined as the ratio between the largest non-saturating photocurrent to the minimum detectable photocurrent. The lower bound of operation is set by the gain of the comparator and the noise present at the comparator input. In other words, the threshold of the comparator must be set such that it is greater than the noise floor, and the integrated photocurrent must be sufficiently large such that it causes a comparator change event

$$V_{\rm min} = V_{\rm noise}. \quad (21)$$

Converting the minimum detectable comparator input to photocurrent

$$i_{\rm min} = \frac{V_{\rm noise}C_{\rm diode}}{t_{\rm max}}. \quad (22)$$

The upper bound is ultimately limited by the speed of the readout circuitry, or the shortest integration period $t_{\rm min}$ before the first frame is scanned out and the high threshold of the comparator

$$i_{\rm max} = \frac{V_{\rm thresh}C_{\rm diode}}{t_{\rm min}}. \quad (23)$$

When the imager is operating in single-slope mode, two thresholds are available, and the integration period spans multiple frame readouts. Expressing the dynamic range of the ADC as the ratio of the two photocurrents

$$\mathrm{DR} = \frac{V_{\rm thresh}}{V_{\rm noise}}\frac{t_{\rm max}}{t_{\rm min}}. \quad (24)$$

In practice, the lower threshold is set to be much higher than the rms noise value. The dynamic range is simply determined by the ratio between the time to first frame out to the total number of frames acquired [13], multiplied by scale factor dictated by

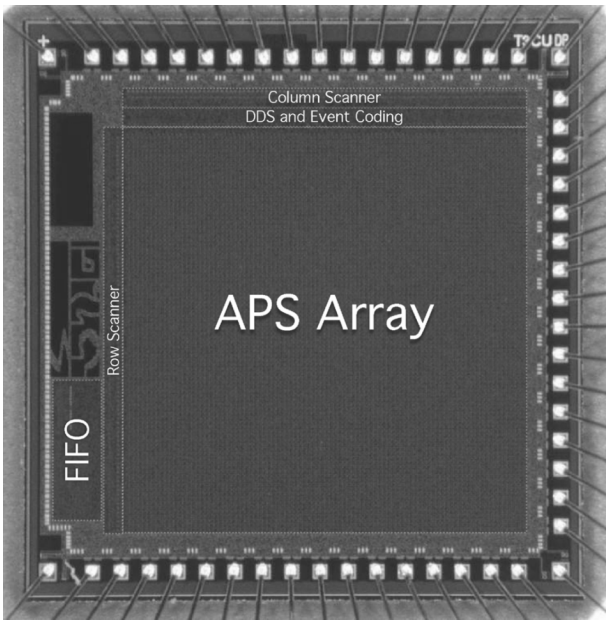

Fig. 13. Chip micrograph.

the ratio of the upper threshold to the lower threshold. In a typical operating scenario, the lower threshold is set to be about 300 mV and the upper threshold is set at 1200 mV. For six bits of resolution, the total dynamic range is 48.2 dB. If this range is insufficient, the pixel level ADC is flexible enough to compensate by capturing more frames to increase the dynamic range. For example, if 128 frames were acquired instead, the dynamic range increases to 54.2 dB. The thresholds of the comparator can be likewise adjusted to alter the exposure settings.

IV. Limitations and Scalability

The main limitation in the present design is the speed of the pixel level comparator. While the impedance of the amplifier's load is large for high gain, this reduces the bandwidth of the circuit since the comparator must directly drive the column line's capacitance. Redesigning the column level readout circuits would yield significantly improved performance. Faster scan out rates would increase the frame rate in the change detection mode. As a result, temporal aliasing would be reduced, making it easier to resolve object edges based solely on the temporal difference. More importantly, the ADC would also enjoy significantly better bright light performance and increased bit resolution.

In terms of scalability, the architecture scales well to larger sizes because the processing elements are distributed to the pixel and column levels and processed in a column parallel manner. No high-speed array level circuits are required for the operation of either the change detection or analog-to-digital conversion. Increasing the image resolution would only necessitate a faster digital latch readout speed to maintain the same frame rate, which is not significantly difficult.

Shrinking to a 0.18 μm from the present 0.5 μm process would result in a reduction of pixel size to approximately 9 μm$\times$ 9 μm which is sufficiently compact for an array of 320×240 pixels on a standard compact 1/4 inch CMOS sensor die—a good fit for the intended application of low-bandwidth security imaging.

TABLE I
Chip Parameters and Characterization Summary

Technology	0.5μm 3Metal 2Poly CMOS
Array Size	90×90
Chip Area	3mm$\times$3mm
Pixel Area	$25.2\mu\text{m} \times 25.2\mu\text{m}$
Fill Factor	17%
FPN (DDS)	0.5% @ 30fps
FPN (Pixel ADC)	1.5% @ 6-bits
Dynamic Range	51db
Saturation	1V
Temporal Noise (DDS)	3mV RMS
Change Sensitivity	2.1% per Frame @ $1.7\mu\text{W/cm}^2$
Max INL	1.5 LSB
Max DNL	.5 LSB
Power	4.2mW @ 30fps and 3V

Power consumption is dominated in large by the DC biasing of the pixel's source-follower and amplifier, the distribution of the clock signals and the operation of the comparator, which must charge and discharge the column line capacitances. Given faster column level readout circuitry, increasing the imager clock rate and power consumption will result in improved images in terms of bit resolution.

V. Conclusion

We present a compact pixel design that integrates a three-transistor, two-capacitor comparator that can function as both a method to detect scene changes and perform pixel level analog-to-digital conversion. A micrograph of the chip is shown in Fig. 13 and a summary of the chip's performance is provided in Table I. The change motion detection provides a compact and efficient means of compressing the data output stream for operation across low-bandwidth wireless networks. The pixel's comparator design can also be used, unmodified, to perform analog-to-digital conversion. Overall impact on the pixel is minimized through a computation-on-readout approach and incurs a minimal impact on the standard three-transistor APS. Since the processing is pixel based, the design is highly scalable to larger array sizes

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