Performance of Analog Viterbi Decoding

Kai He and Gert Cauwenberghs
Department of Electrical and Computer Engineering
The Johns Hopkins University, Baltimore, MD 21218
E-mail: {hek,gert}@jhu.edu

Abstract— **We propose the Binary-Analog Channel (BAC) as a model for a binary communication channel accounting for analog saturation effects, and use the model to analyze analog Viterbi decoding. We also model imperfections in the VLSI implementation of the analog decoder, to estimate practical performance. Extensive random coding simulations indicate that an analog Viterbi decoder implemented in a typical CMOS process easily outperforms its digital counterpart with 3-bit or higher soft-decision decoding resolution.**

I. Introduction

Convolutional coding and Viterbi decoding are widely used in modern digital communication systems, such as space communication, satellite communication, and mobile communication. A digital communication system model is depicted in Figure 1. For coding system analysis, the modulator, demodulator and physical channel are combined into one block, shown as the analog channel in Figure 2.

The (2,1,7), or rate $1/2$, constraint length $K = 7$ convolutional code is widely used in satellite communications. The generation polynomial is $(171, 133)_8$. Configurations of the encoder and Viterbi decoder, including add-compare-select (ACS) and path memory, are illustrated in Figure 3.

In recent years, analog Viterbi decoding has received increasing attention owing to the promise of high-speed performance and significant savings in power consumption and silicon area. Recently, a 64-state, $K = 7$ analog ACS decoder has been implemented on a single chip [1].

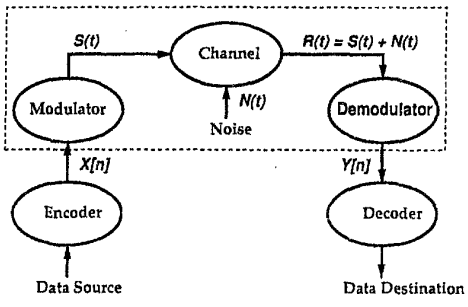

Fig. 1. *Digital communication system model*

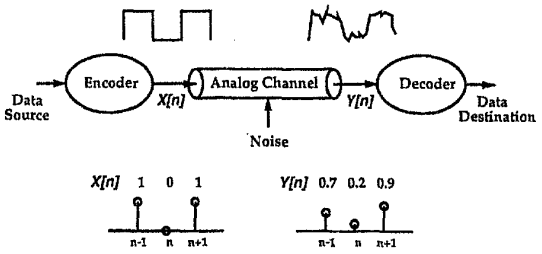

Fig. 2. *A simplified digital communication system model with analog channel*

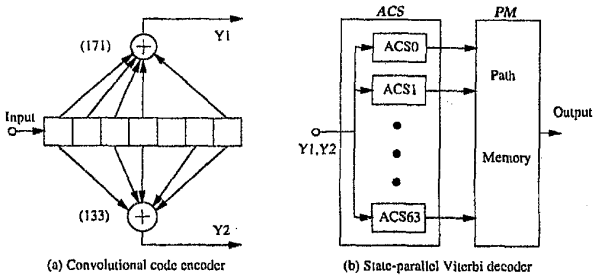

Fig. 3. *(a) Encoder (b) State-parallel Viterbi decoder for (2,1,7) convolutional code*

II. Analog Viterbi Decoding in BAC

In traditional systems where digital Viterbi decoders are used, the analog outputs of the demodulator have to be quantized by A/D converters. A hard-decision decoder requires a 1-bit quantization, while n-bit A/D converter is used in an n-bit soft-decision decoder. 3-bit soft-decision is usually adopted in practical systems because it provides a 2-3 dB coding gain over hard-decision decoders at normal error-rate, very close to the performance of analog Viterbi decoding [2]. When the A/D converter is included as part of a Viterbi decoder diagram, then any Viterbi decoder, analog or digital, could be considered an "analog-input," although quantized, Viterbi decoder.

An **analog Viterbi decoder** is a Viterbi decoder whose ACS module is analog, that is, all metrics are computed and stored as analog signals by analog ACS circuits. An ideal analog Viterbi decoder has the highest performance due to its infinite resolution, but such a decoder cannot be implemented with real hardware.

Figure 4 shows four types of analog-input Viterbi decoders:

0-7803-5491-5/99/$10.00 © 1999 IEEE

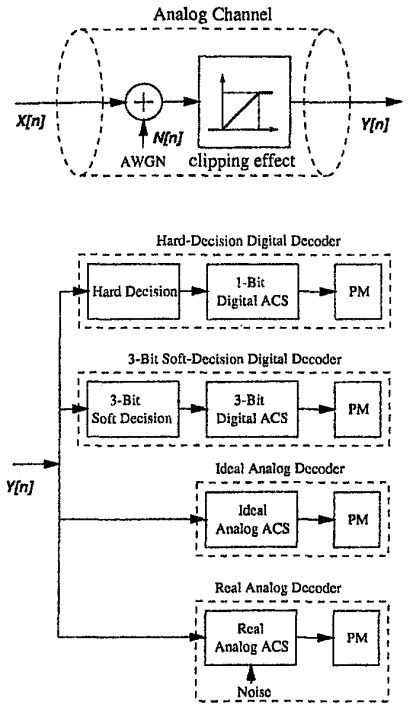

Fig. 4. *Binary Analog Channel (BAC) and four types of analog-input Viterbi decoders: hard-decision digital decoder, 3-bit soft-decision digital decoder, ideal analog decoder and real analog decoder*

hard-decision, 3-bit soft-decision, ideal analog and real analog. By introducing the concept of analog-input Viterbi decoder, comparison among different decoders becomes easier. It is clear that digital decoders cannot achieve the performance of an ideal analog decoder due to the quantization noise. This is also why a real analog Viterbi decoder with analog circuit imperfections can still perform as well as a 3-bit soft-decision digital decoder, or even better.

A. *Clipping Effect and Binary Analog Channel (BAC)*

Assuming the channel is subject to additive white Gaussian noise (AWGN), the digital input is converted into an analog signal as the output of the channel. The signal, however, can not take any unbounded analog value. It is subject to saturation effects common in VLSI and many other electronic and optical systems. We call this the **clipping effect**.

The clipping effect in VLSI systems is a direct result of the fact that any voltage signal is bounded by the power supplies, through several physical mechanisms. For example, over-voltage protection diodes on IC pins limit the signal between Vdd and GND; and amplifier outputs are bounded between Vdd and GND when transistors reach saturation. So from the perspective of hardware, a range limitation is always imposed on the signal.

Therefore, a clipping function should be represented in the analog channel model, as shown in Figure 4. We call this the

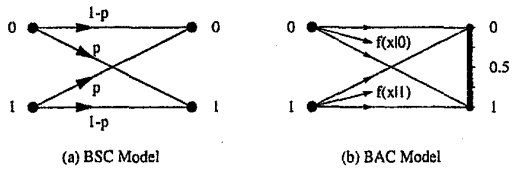

Fig. 5. *(a) BSC model and (b) BAC model*

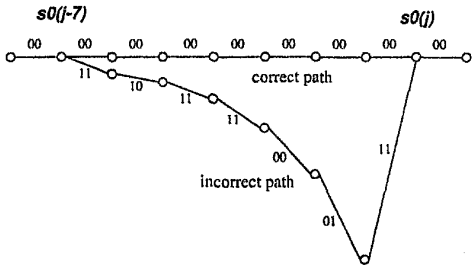

Fig. 6. *A minimum-weight error event (d=10) in Viterbi decoding with (2,1,7) convolutional code*

Binary Analog Channel (BAC) as a mathematical model for analog coding analysis. This model is more accurate that a AWGN-only model because of the clipping function is a good reflection of the real systems.

In convential coding theory, the Binary Symmetric Channel (BSC) model is used in digital coding analysis with binary inputs and outputs, shown in Figure 5. It is easily verified that BSC is a special case of BAC where the clipping reduces to a hard threshold as with a 1-bit ADC.

B. *Error-Event Probability of Analog Viterbi decoding*

In Viterbi decoding, error-event probability P_d is an important parameter for decoding performance measurement. The example in Figure 6 shows an error-event of Hamming weight 10 ($d = 10$), which is a minimum-weight error event for the (2,1,7) code. It is assumed that an all-zero sequence is transmitted, so the all-zero path is the correct path. If during decoding, the received sequence carries errors (1's in this case), then the decoder may make a wrong decision by choosing the incorrect path as the output. along the path get flipped over from 0 to 1.

In analog Viterbi decoding, the distance between two paths is the difference of two path metrics, which is an analog quantity and no longer a integer as for the Hamming distance in the BSC. The error event probability P_d depends on the sum of analog input values at the d error positions. In case of the minimum error-event, the error path has a weight of 10, then the sum of the 10 analog inputs determines whether such an error event can happen.

The mathematical details of the analysis and derivation will appear in an extended version of the paper.

To compare the performance of ideal analog decoding and digital decoding, we calculate P_d for different SNR and plot

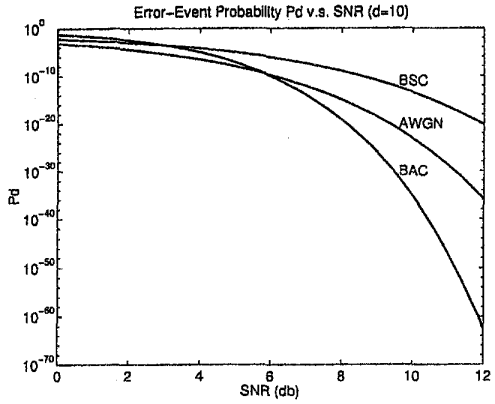

Fig. 7. *Comparison between P_d performance of digital and analog decoding, using the BCS and BAC models. Performance with AWGN model (without clipping or thresholding) is also shown.*

the curves, as shown in Figure 7.

To obtain estimates of the performance of real analog decoders, we model the effect of noise and imprecisions in the next section.

III. Analog Viterbi Decoder

A. Branch Metric Transfer Function (BMTF)

In an analog-input Viterbi decoder, the analog input is transformed into branch metrics by the branch-metric-calculation (BMC) circuit. In digital decoders, BMC is performed by A/D converters and analog inputs are quantized into digital bits. In an analog decoder, the analog input is directly transformed into another analog value. We normalize both the input and the output scales of a BMC to unity, and call this characteristic the branch metric transfer function (BMTF). The BMTF's of the four analog-input Viterbi decoders are shown in Figure 8. For digital decoders, the BMTF's are the input/output characteristics of the quantizers. For an ideal analog decoder, a clipped linear function reflects the saturation of the analog channel as discussed earlier.

B. Analog ACS Model and Simulated Performance

An analog Viterbi decoder ACS processor model, based on a state-parallel analog ACS chip we previously implemented [1], is shown in Figure 9. The example ACS processor shown is for state-0 (ACS0); there are 64 similar ACS processors in the whole ACS unit, configured in parallel and interconnected through a shuffle-exchange type network defined by the 64-state trellis. We model the analog circuit imperfection into three categories. The first is the nonlinear effect of the BMC, which is defined by BMTF. The second is circuit noise (thermal noise) in the signal loop, which for simplicity is lumped into two independent AWGN sources in the adders. The third

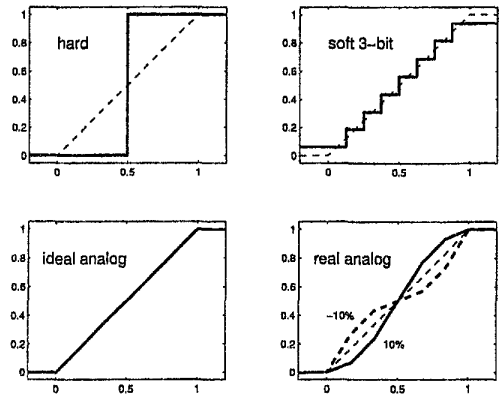

Fig. 8. *Branch metric transfer functions for four different Viterbi decoders: (a) hard-decision digital decoder, (b) 3-bit soft-decision digital decoder, (c) ideal analog decoder and, (d) real analog decoder with 10% nonlinear distortion*

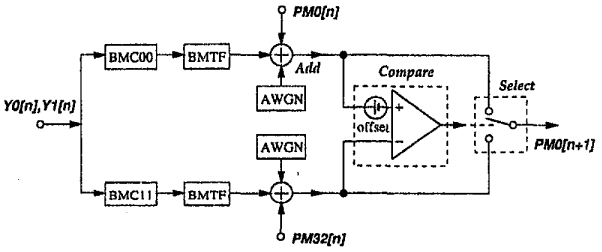

Fig. 9. *Analog Viterbi decoder ACS processor model (state-0)*

imperfection is the presence of comparator offset, which also includes fabrication mismatches.

We have conducted extensive random coding simulations on the four types of Viterbi decoders. The test input is the output of the BAC channel. We use 600,068 analog samples in order to generate 300,000 decoder output bits. All decoders use the same trace-back path memory of length 35. For each decoder, we recorded the bit-error-rate (BER) for SNR =3.0 dB, 3.2 dB, and 3.4 dB.

Figure 10 shows the simulated BER performance of hard-decision (1-bit soft-decision), 2-bit soft-decision, 3-bit soft-decision, 4-bit soft-decision and ideal analog decoders. Two facts are clearly demonstrated: (1) soft-decision is superior to hard-decision as is well known, and (2) 3-bit soft-decision is close in performance to ideal analog Viterbi decoding.

Figure 11 shows the simulated BER performance of a real analog decoder with different levels of ACS noise (AWGN): σ_{ACS} = 0.1, 0.07, 0.05, and 0.035. It is clearly demonstrated that when $\sigma_{ACS} \leq 0.05$, the performance of the analog decoder matches or exceeds that of a 3-bit soft-decision decoder[1].

Figure 12 shows the simulated BER performance of a real analog decoder with different levels of comparator offset. We simulated the worst case dedicated in the all-zero input sce-

[1]Note that ACS noise does not suffer from clipping effect.

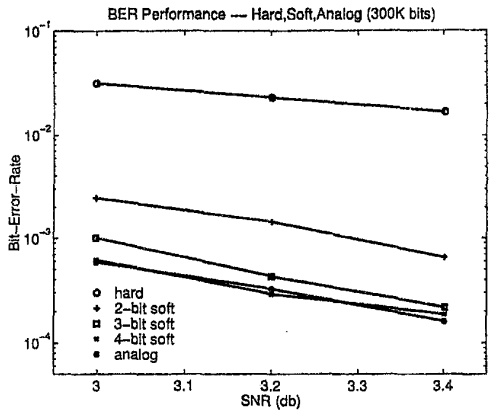

Fig. 10. *Performance of hard-decision, soft-decision, and ideal analog Viterbi decoders*

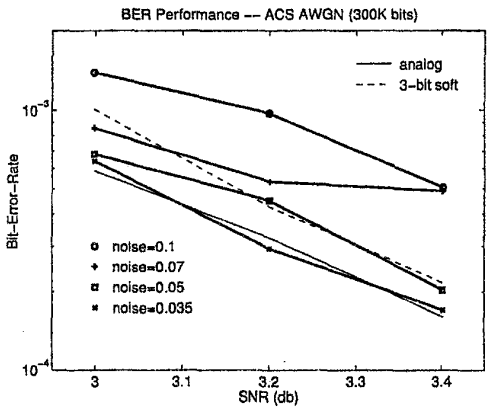

Fig. 11. *Performance of real analog Viterbi decoder with ACS noise*

nario: the comparator in ACS0 has the biggest negative offset $-\Delta v$, while all other 63 comparators have offsets randomly selected from a uniform distribution over the [$-\Delta v$, Δv] interval[2]. The simulation results testify that analog Viterbi is robust to comparator offset, tolerating up to 15% of the range in comparison with a 3-bit soft-decision digital implementation.

Figure 13 shows the simulated BER performance of a real analog decoder with non-linear BMTF as shown in Figure 8. The concave-convex curve is based the nonlinear effects of CMOS transistors and operational amplifiers. The simulation shows that analog Viterbi decoder can tolerate 10% of BMTF nonlinearity, in comparison with the 3-bit soft-decision digital case.

IV. Conclusions

We introduced a BAC model for analog channel, and applied it to the analysis of analog Viterbi decoding performance.

[2]A negative offset for ACS0 biases the decision made at state-0 against the all-zero path, which deteriorates the decoder gain.

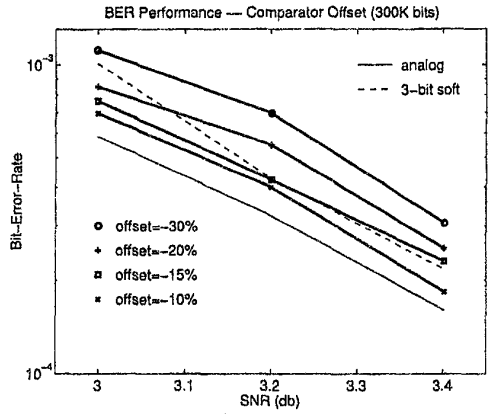

Fig. 12. *Performance of real analog Viterbi decoder with comparator offset*

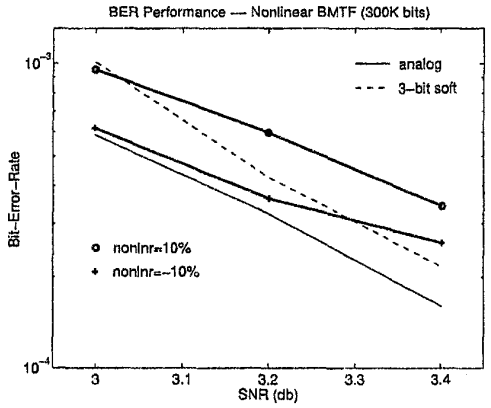

Fig. 13. *Performance of real analog Viterbi decoder with nonlinear BMTF*

We also introduced an analog Viterbi decoder ACS model to simulate real analog Viterbi decoder performance. The results showed that analog Viterbi decoders are able to outperform digital Viterbi decoders, and can achieve 3-bit or higher decoding resolution. This makes analog VLSI implementations attractive for communication systems where low-power operation and high density are primary design constraints [1].

References

[1] Kai He and Gert Cauwenberghs, " An area-efficient analog VLSI architecture for state-parallel Viterbi decoding", *Proceedings of ISCAS'99*, vol. II, pp. 432-435, June, 1999.

[2] J. A. Heller and I. M. Jacobs, "Viterbi decoding for satellite and space communication," *IEEE Trans. Commun. Technol.*, vol. COM-19, pp. 835-848, Oct., 1971.

[3] A. J. Viterbi and J. K. Omura, *Principles of Digital Communication and Coding* , pp. 246-249, New York: McGraw-Hill, 1979.

[4] Shu Lin, Daniel J. Costello. Jr., *Error Control Coding: Fundamentals and Applications* , pp. 322-328, Englewood Cliffs, NJ: Prentice-Hall, 1983.