A Detector Array For Direct Control of a Deformable Mirror

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ABSTRACT

A wavefront sensing detector array is presented with capabilities suited towards high-order adaptive optics systems. The phase of the wavefront is sensed by modulating and synchronously sampling the fringes of a white light interferogram imaged onto the array. The nature of the modulation is characterized by a voltage signal, which is delivered as an input to the array. As a fringe moves across an individual detector, the null is sensed, triggering a sampling of the modulation signal. The sampled signal represents the phase of the wavefront and is held until the next null is sensed. The signal makes it possible to directly send commands to a deformable mirror to correct the phasefront. This chip is optically mapped such that each pixel in the array corresponds to an actuator on the deformable mirror. The array outputs both the photodetector current and the sampled modulation signal voltage from individual pixels by means of bit parallel row and column inputs. A prototype of this array has been fabricated in a 0.5um CMOS process with 21 x 21 detectors, suitable for (circular) deformable mirrors with up to 349 actuators. Experimental results suggest refresh rates in excess of 3kHz are attainable. This wavefront sensor could greatly simplify the process of controlling a deformable mirror for many applications, thereby increasing refresh rates and improving sensitivity.

Keywords: VLSI, wavefront sensing, adaptive optics, interferogram, phase modulation, deformable mirror, phototransistor, detector array

1. ADAPTIVE OPTICS AND PHASE RETRIEVAL

One of the biggest challenges with adaptive optical systems is phase retrieval, or wavefront sensing. This is the key to running a deformable mirror. Existing methods of phase retrieval can be multi-stage processes [eg, Glindemann 2000 and references therein]. They typically involve an image sensor, such as a CCD. An image (of an interferogram, for example) is acquired and processed, and after some computation the phase can be derived. Often, a history of images is needed to determine the necessary phase corrections needed to flatten the phasefront. After the image(s) has been processed, the phase corrections need to be determined to send the necessary actuator movements to the deformable mirror.

For astronomical applications, the trend is to move adaptive optics toward higher refresh rates. Higher refresh rates allow for better corrections to the phasefront, and result in higher Strehl ratios. High Strehl ratios are critical for high dynamic range coronagraphy. However, high refresh rates require fast phase retrieval. Currently, the desire is to push these refresh rates in excess of 2kHz. The ability to acquire a CCD image (even a small image), process it, and output the phase information at these speeds is at the edge of technology, and involves a lot of costly equipment as well as complex software.

Very Large Scale Integrated (VLSI) electronics can provide a good solution to this problem. VLSI allows some algorithms to be implemented on the same chip that the image sensor is located. By processing some of the information on the chip, time can be saved and in some instances more accurate solutions can be found. In the case of phase retrieval, probably the most profound benefit is the reduction in noise. Since no photoelectrons actually need to leave the chip in order to process information, read noise is reduced. The reduction of read noise means an increase in signal to noise ratio, increasing the number of available observations, or improving the science on existing observations.

The use of VLSI to solve problems in Adaptive Optics is not new. Various other approaches to solving problems in adaptive optics have been attempted in VLSI, with solutions intended for Shack-Hartman devices (P.M. Furth, 1998), and low-order correction (M. Vorontzov, 2000). The advantages of VLSI for future developments in Adaptive Optics is substantial, and offers benefits not found with other approaches.

One type of phase retrieval makes use of an interferogram. By interfering a reference beam (flat phasefront) with a test beam, a series of fringes results. These fringes create a sort of contour map of the wavefront in the test beam. There is some ambiguity in the raw interferogram however that needs to be resolved: the sign of the slope of the contour normals.

To determine the sign of the slope, at least two slightly different interferograms are needed. By looking at the direction of the movement of the fringes, slope can be determined. One way to create these slightly different interferograms is to modulate one of the flat fold mirrors in the test beam (refer to figure 1.1). By moving the mirror, this arm of the interferometer has changed path length. Knowing the movement of this mirror allows for precise determination of wavefronts in the interferogram(s).

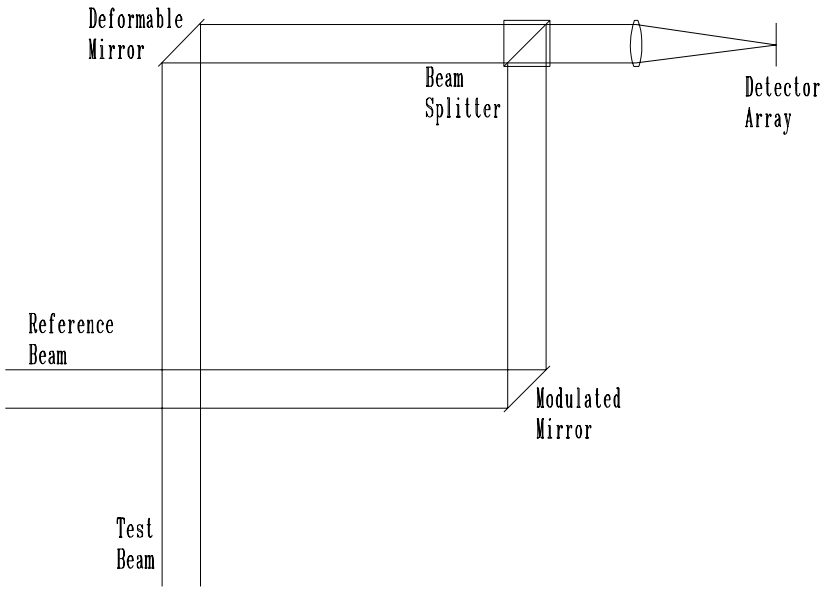

Figure 1.1 Schematic layout of two interfering beams in a phase-shifting (Mach-Zender) interferometer. By modulating a fold mirror in the reference beam, known phase error is introduced into that beam, making it possible to gather complete phase information from the interferogram. Lens depicted in front of detector array is intended for proper plate scale (mapping) only. See section 2.5.

2. DETECTOR ARRAY

The use of a modulated mirror in one beam of the interferometer allows for direct measurement of the phasefront in real time if the interferogram is imaged onto a detector array containing built-in processing circuitry. The modulation of the mirror causes fringes in the interferogram to move. If the light for this interferogram is sufficiently broadband and incoherent, there is only a very narrow region of path difference during which fringes will be observed, and there will only be a couple dark fringes in the band of coherence. While the modulated mirror moves fringes, a dark fringe will sweep across a pixel. By sensing where this dark fringe occurs, phase retrieval can be performed. This is the basis of this detector array. It is designed to be used in an interferometer as described above, and includes additional circuitry to sense a dark fringe and ouput the phase.

2.1 Modulation

One of the inputs to this chip is a modulation signal. This signal is a voltage delivered to all pixels, and has a waveform that characterizes the modulation of the mirror. The shape of the modulation can be catered to the application, and can be saw-tooth, sinusoidal, or virtually anything that allows the system to function optimally.

For fringe sensing, dark fringes were chosen as the trigger source because of the likelihood that most applications would have a very short coherence length and a broad bandwidth to maximize the number of incident photons. As the modulated mirror moves, the distance over which fringes are sensed is small compared with the peak-to-peak movement.

Although there will be fringes that are brighter than the baseline, the proportional difference between the baseline intensity and a dark fringe is much greater than the difference between the baseline and a bright fringe (which can never be more than a factor of two brighter than the baseline).

2.2 An Integrated Pixel

The detector for this device is a PNP phototransistor. Photodiodes were considered, but since this device is to be used under very low light conditions, a device with gain was desired. Avalanche photodiodes offer some gain, but are also noisy. Phototransistors offer gain, but are slow devices. Their speed limitations were considered to be a benefit over the noise considerations, and some initial gain was considered to be necessary. A PNP device is favored over an NPN device due to the available layers in the 0.5μm fabrication process.

The circuit for the fringe sensing starts with a current mirror of the phototransistor current. This current is amplified (by means of a larger mirror transistor) and at the same time sent through an inverting amplifier. The voltage between the transistors of the inverting amplifier is sent to another inverting amplifier. The second inverting amplifier creates the pulses that trigger a sample and hold switch. Both inverting amplifiers require an input bias voltage, and these voltages need to be adjusted based on the photocurrent. The sample and hold circuit is simply an nmos switch. The modulation signal goes through this switch to a capacitor. The voltage at the capacitor is always available for output. A copy of the phototransistor current is also always available for output. All of this circuitry is built into a single pixel, depicted in Fig. 2.1. For the prototype chip, an array of 21 x 21 of these detectors was chosen (see section 2.5).

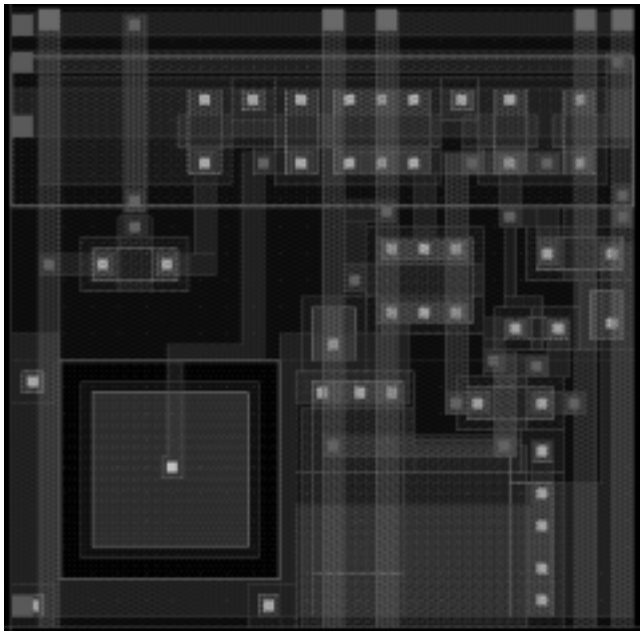

Figure 2.1 The layout of the pixel. At the lower left is the phototransistor. The sample and hold capacitor is at the lower center to left. Detector fill factor is approximately 10% by area.

2.3 Fringe Visibility

There is more to fringe visibility than just coherence length and bandwidth. For this detector array, the size of the detector also plays an important role. It is desirable to detect fringes that are relatively narrow, as would be found from a phasefront with a significant amount of slope. If the fringe width is narrower than the detector itself, then the width of a null sensed will be both wider than the fringe, and not as dark. If the null is not dark enough, the fringe will not be sensed at all. If the null is too wide, then the accuracy of the phase retrieval will be impaired.

For this array, a fill factor of ~10% was chosen. This makes the detector approximately 1/3rd of the pixel spacing. This should provide good fringe visibility for many applications. If larger fill factors are a requirement due to signal strength limitations, then the fill factor can be increased by use of a lenslet array in front of this chip, to concentrate the light onto the phototransistors. Using this technique, fill factors of nearly 100% can be achieved, with reduced narrow fringe visibility. This is a trade-off that needs to be considered prior to implementation.

2.4 Periphery

Each pixel has two outputs and three inputs, in addition to row select inputs. At the edge of the array is the row and column select circuit using 5-bit parallel inputs. To save space, a pseudo-nmos circuit was used, with dual inverted output to ensure rail to rail operation. Although the dual inverters may seem like a lot of extra transistors, both row select and not row select signals were needed, and the resulting circuit still has fewer transistors than a cmos 5-bit inverted nand gate.

A row select delivers an entire row of pixels to the output buffer, which contains switches activated by the column select. The output buffer will output a single pixel at a time, and will output the phototransistor current mirror and the sampled modulation signal voltage. The voltage output goes through a buffer which has linearity controlled by two bias voltages. This assures that the readout will be non-volatile.

A picture of the chip can be seen in Figure 2.2, with periphery circuits and additional test phototransistors (see section 3.1).

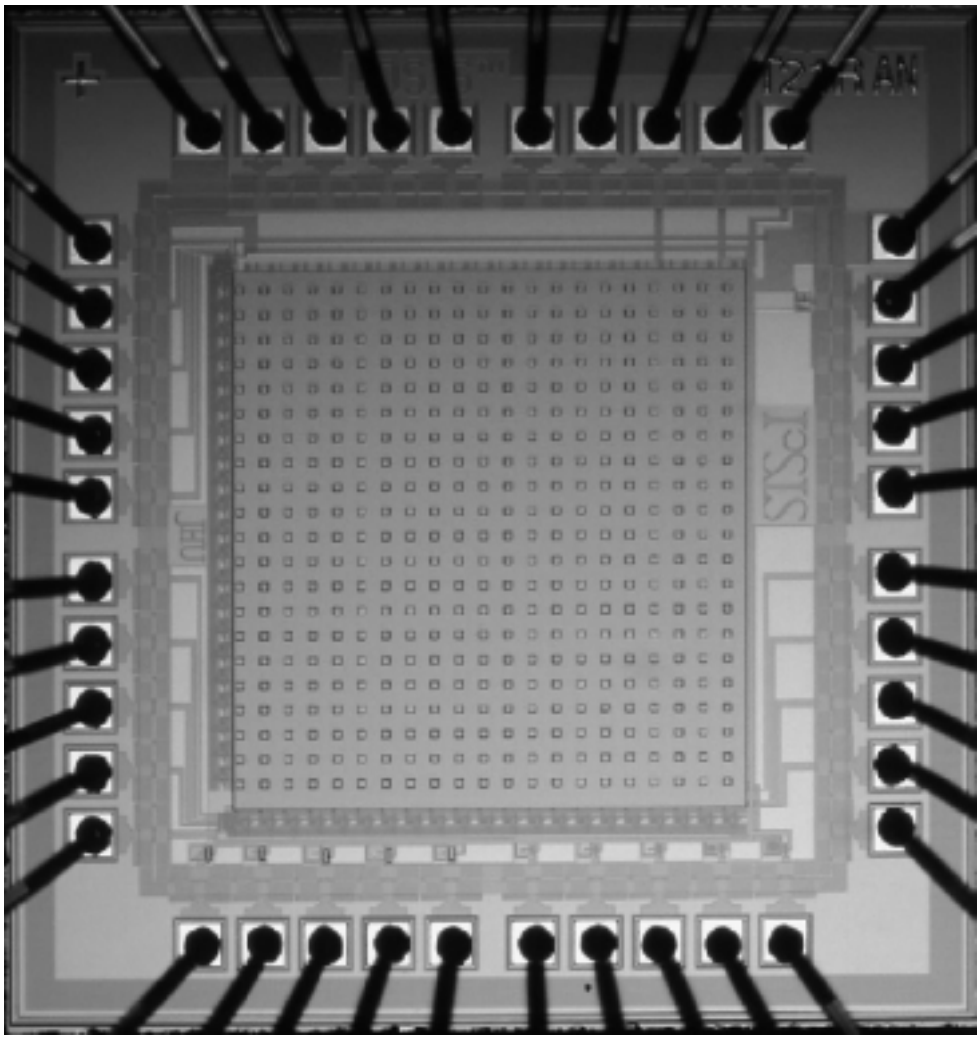

Figure 2.2 The detecor array, as fabricated. The row select can be found just to the left of the array, and the column select is at the bottom. Since the processing electronics can be affected by light, they are covered with metal (metal 3 layer in this process). The output buffer, for example, is just above the column select, but covered with metal. Below the column select is a series of phototransistors with various geometries to test other layout methods. An additional test phototransistor can be found above the STScI logo, second pin from the top.

2.5 Mapping

The output voltage of this device is intended to drive a deformable mirror with little or no computation. The input modulation signal has a DC offset, but once this offset is removed, the output voltage can be thought of as only needing to be amplified to drive the deformable mirror actuator. Each pixel corresponds to a single actuator location, and the output voltage is the resultant "piston" movement needed at the actuator. When using this device in an adaptive optics system, the optics need to map the center of each actuator on the center of each pixel, as seen in Figure 2.3.

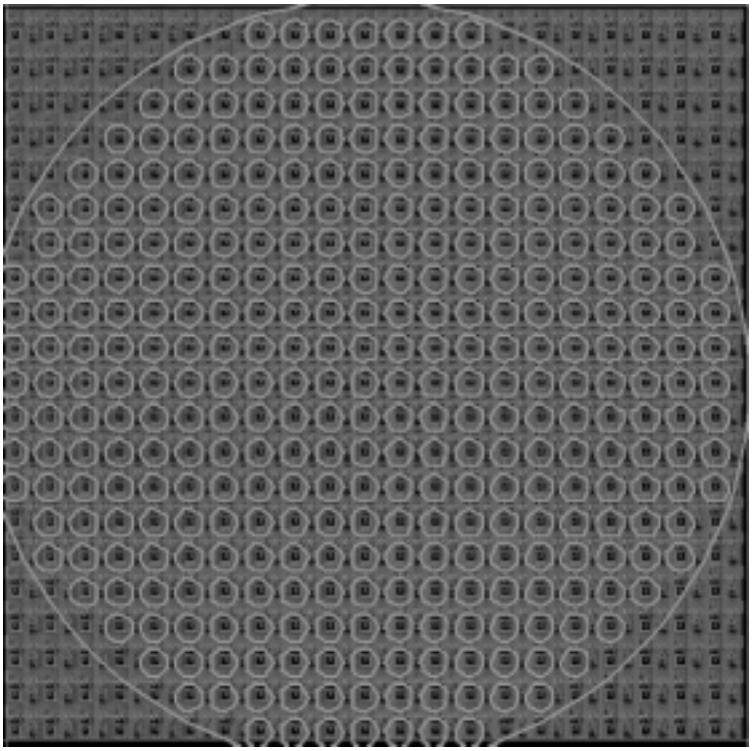

Figure 2.3 The detector array with a mapping of actuator positions overlaid. The overlay is of a 349 actuator Deformable Mirror with square grid spacing. Row and Column select and other periphery electronics are not shown.

3. TESTING

3.1 Phototransistor design

Several different phototransistor layouts were added to the periphery of the chip to determine what geometry might offer the optimal performance for this device in a future version. Since the fill factor was already determined, the actual physical dimensions of the transistor base were not important. The collector is at ground potential, and constitutes the substrate of the chip. Therefore, the emitter geometry was the focus of this exercise, although a couple of additional base sizes were also investigated. For a given base dimension, two to three emitter sizes were tried. One emitter was the maximum possible size, given the constraints of design rules. One emitter design was ~45% smaller in area. Another design implemented the use of parallel, minimum sized emitters. A set of transistors equal in base size to those in the array was installed. Other size bases were also installed for the sake of simply getting a better understanding of the relationship between size and speed of these devices. Another transistor was added that includes a clamped base voltage, using a bias voltage for control of the clamp voltage. This configuration was presumed to help the speed of the device.

Testing of these devices is not yet complete, however future versions of this chip would incorporate lessons learned from this testing into the design.

3.2 Array Test Setup

To simulate fringes, a red LED was used as the light source to illuminate the chip. A light tight holder was fabricated to hold the chip and allow the LED to shine on it. This chip carrier entirely surrounded the chip, and had a pin socket through it to allow for testing while on a circuit board. The LED was driven using a pulse width modulated square wave. To generate a modulation voltage signal, a saw-tooth waveform was generated with a DC offset voltage of 2.5V and a peak-to-peak voltage of roughly 400mV. The DC offset and P-P voltage assures that the ouput buffer can accurately copy the voltage.

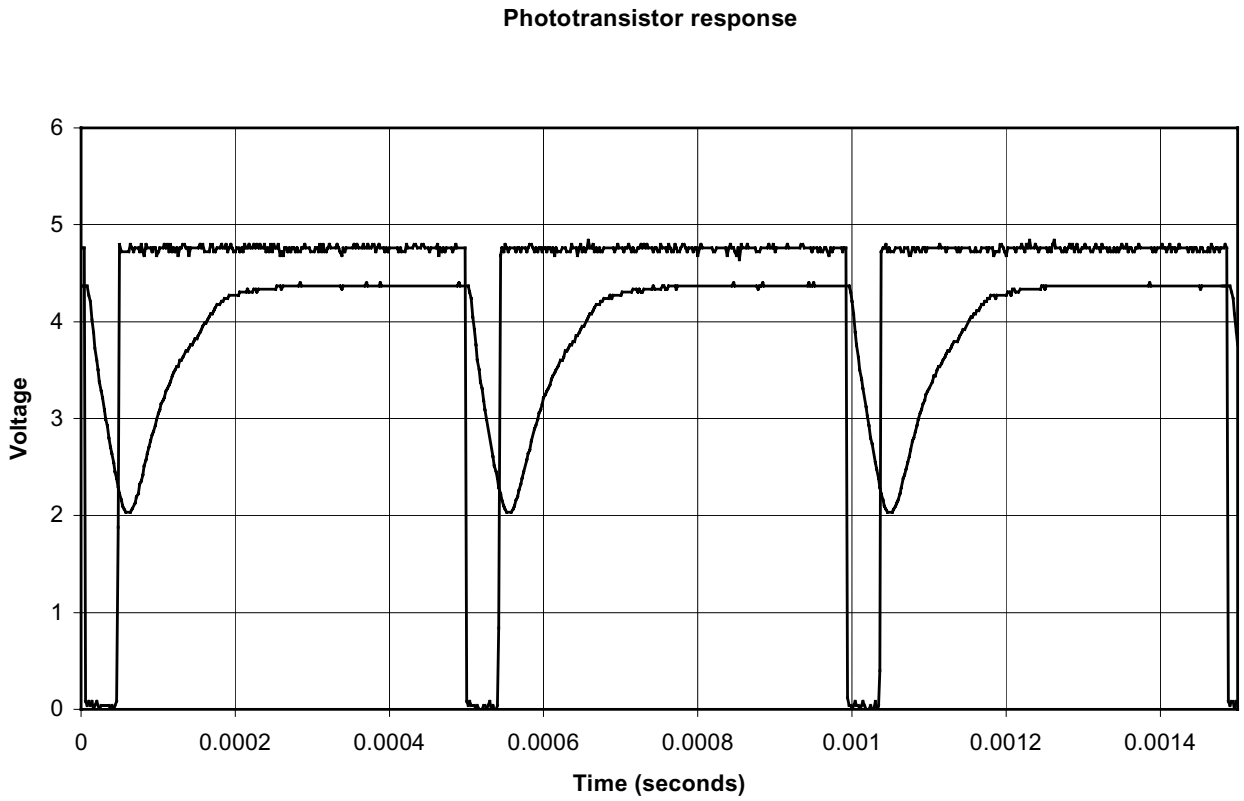

Figure 3.1 The response of the phototransistor to a pulsed LED. The voltage indicates the applied signal to the LED, which is represented by the ~10%-off duty cycle square-wave. The other curve shows the response of the phototransistor, measured as a voltage from the transimpedance amplifier connected to the output current of the array. Voltage shown does not represent actual measured voltage for the amplifier. The curve is shown to indicate the response time of the device.

The test setup started with a measurement of the photocurrent output from the array, in comparison with the LED signal. To measure the photocurrent, a low noise transimpendance amplifier was constructed. The current to the LED was lowered to determine the minimum operating flux. As the current was lowered, the modulation signal started to corrupt the photocurrent, suggesting a minor change to the layout of the sample and hold circuit or output buffer might be necessary. The nature of this leak was parasitic, as it occurred at very low incident fluxes. Measurement of the optical power from the LED indicated that this device would work with incident power exceeding 350pW per detector.

The response of the phototransistor to the LED is faster turning off, as shown in Figure 3.1. Narrowing the "off" state of the LED did not appreciably narrow the photocurrent null. Rather, it only reduced the depth of the null. The turn on and turn off times are not dependent on incident flux, so this is not a problem that can be solved without a change to the layout of the chip. Regardless, the bias voltages can be adjusted for photocurrent such that a lower "threshold" triggers the S/H switch. Figure 3.2 shows a worst-case scenario of the sample and hold response to the photocurrent, with the

threshold just below the baseline intensity. In practice, the bias voltages can be adjusted to trigger at roughly the half-max point. This reduces the sampling time somewhat. Setting the bias voltages to trigger at even lower thresholds results in sampling times that are much less uniform. With properly tuned bias voltages, the sampling state can be reduced to roughly 30% of the duty cycle at speeds up to 3kHz with reliable operation.

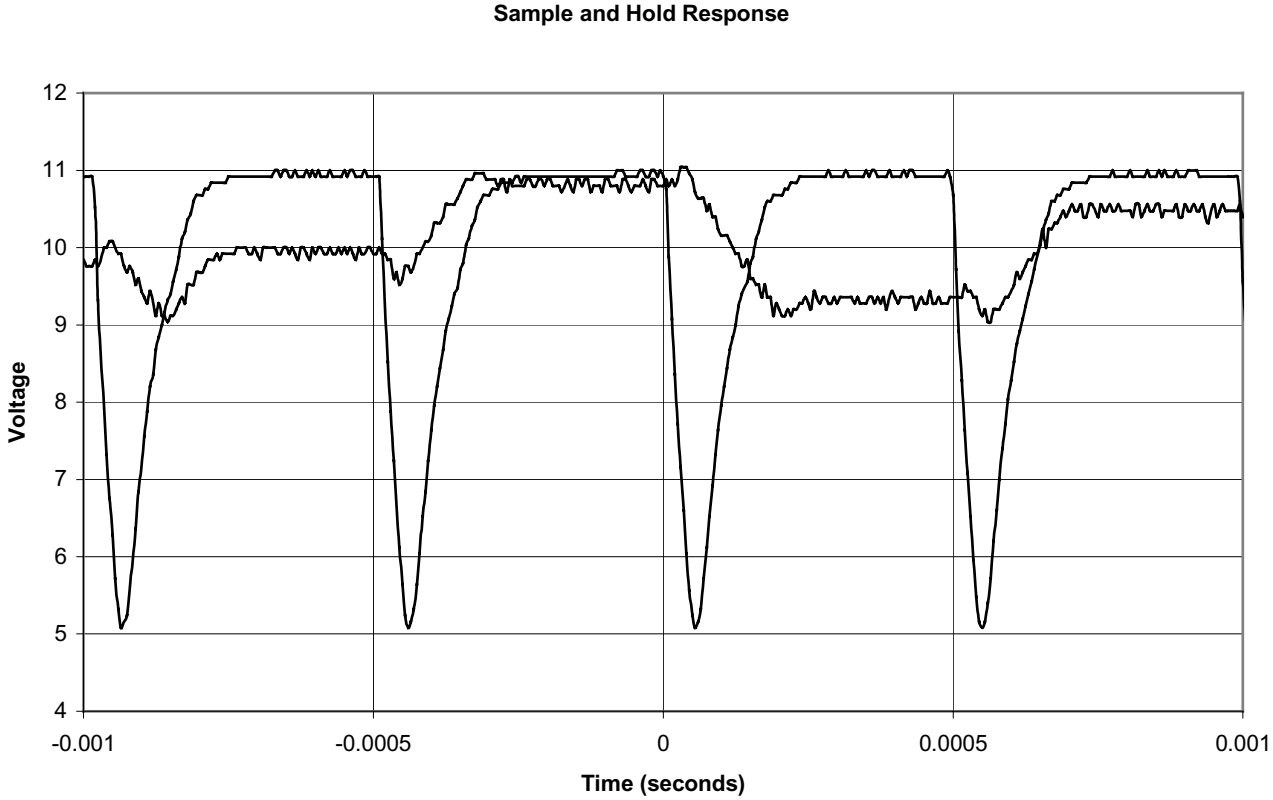

Figure 3.2 The relationship between the phototransistor signal and the sample and hold signal. When the LED is off, the modulation signal is sampled (seen above as following a saw-tooth curve during the sample state). When the LED is on, the sampled signal is held.

3.3 Spectral Response

The spectral responsivity of this device is an important consideration for implementation. A suitable wavelength range needs to be chosen such that the device will respond well, but not interfere with scientific goals. To measure the responsivity, a monochromator was used to illuminate the chip and the resulting photocurrent was measured. The results of this measurement are shown in Figure 3.4. The overall shape of the response curves looks similar to silicon, as would be expected, however this device shows an overlying sinusoidal dependence on wavelength. It is unclear what causes this modulation of the responsivity, but one possibility might be that multiple layers are causing a waveguide effect. The gap between layers can be sufficiently large to allow light to enter, and perhaps the result acts like a waveguide, allowing light to interfere constructively or destructively at the phototransistor. The periodic structure of the responsivity appears to have a frequency (in wavelength space) that varies with wavelength. This supports the waveguide possibility. It is unclear why the amplitude of this periodicity should be so large, even if there is a waveguide phenomenon occurring.

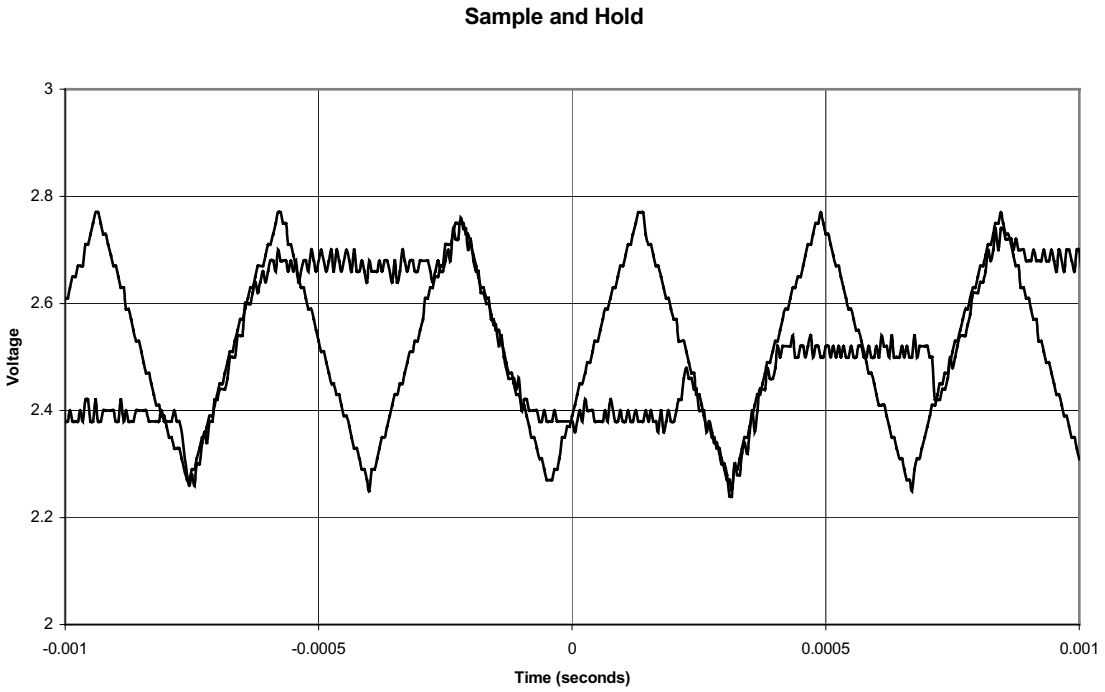

Figure 3.3 The modulation signal is shown with the sample and hold signal. This shows that the S/H circuit very quickly reaches the new voltage, and holds steady until the next sampling. This also shows the output buffer accurately copies the voltage from the S/H circuit.

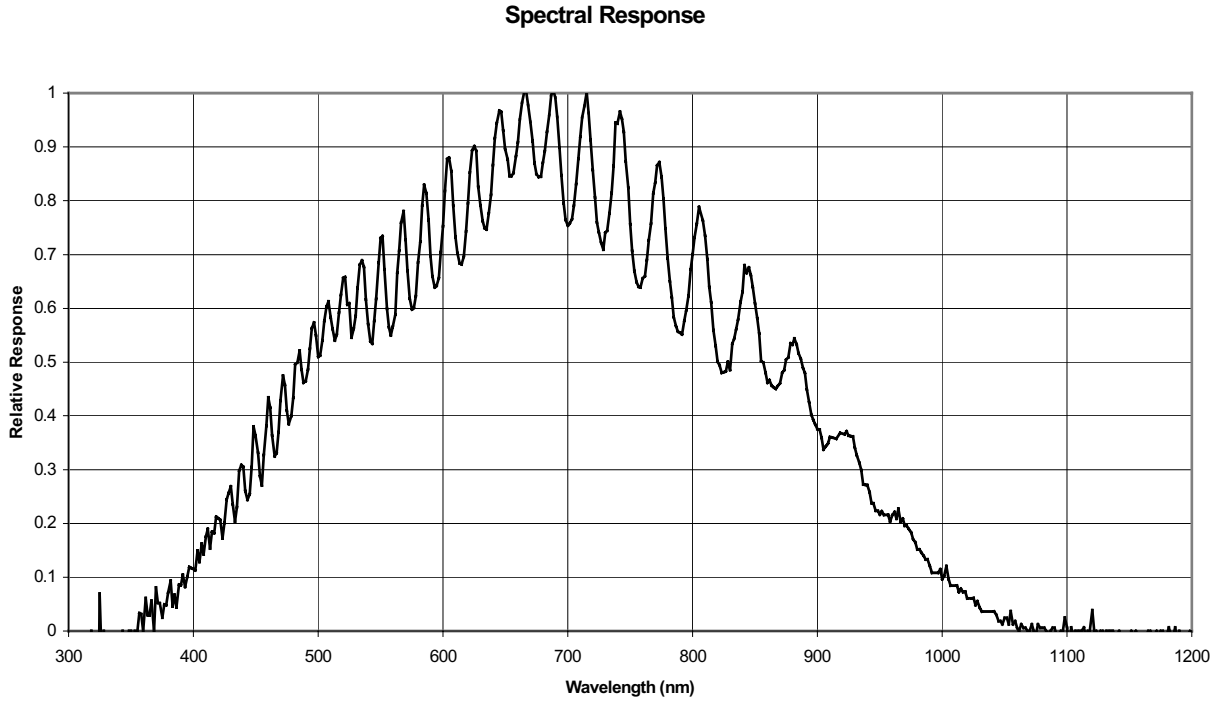

Figure 3.4 Phototransistor spectral response, normalized. Absolute responsivity measurement was not available, so all values are relative to the peak responsivity.

4. FUTURE DEVELOPMENTS & OTHER USES

The impedance of the photocurrent amplifier may be decreased for a future version, to improve response times. Although this will not improve the response of the phototransistor itself, it should reduce any added delays to the signals within a pixel by reducing the overall impedance. Such delays are not necessarily a defect for the intended application, but other possible uses for this chip might find improved response times desirable.

The noise of this device is inherently low due to processing within each pixel. However, this chip does show that there could possibly be a layout issue with the sample and hold circuit, as the modulation signal tends to "leak" into the photocurrent if the incident flux is not sufficiently high to mask it. This layout problem will be investigated for future chip development. Eliminating this parasitic leak could significantly reduce the required flux for proper operation. Disconnecting the modulation signal revealed that the characteristic phototransistor response curve could be reproduced at fluxes that were in excess of a factor of 10 times lower than those required for operation with the modulation signal.

Versions of this chip that were intended for use in a scientific instrument would likely include lower temperature operation to reduce noise and possibly further reduce the required flux.

This chip is easily scaled for array sizes that are much larger. Using a 6-bit parallel input, array sizes of up to 63 x 63 pixels are easily achieved. Such an array would be suitable for deformable mirrors with an excess of 3000 actuators, and would require only a 3mm x 3mm chip size. This opens the possibility of driving such a large deformable mirror at refresh rates in excess of 2kHz, with a relatively simple and inexpensive set of electronics. This is well suited to second-stage AO coronagraphy, for instance [eg Angel, 1994].

This chip could also be useful for non-astronomical applications. Since this device outputs a voltage that is proportional to the actual phase error (plus an offset), this chip might find use in many other devices that require high-speed phase retrieval. Since this device allows for a substantially reduced time delay between measurement and output of phase, it could be very useful for applications involving optical metrology measurements of dynamic systems. An example might be vibration analysis, allowing mode shapes to be determined during vibration. Perhaps this could also be applied to certain types of optical fabrication. A phase map of the surface could be obtained while it is being machined, allowing for corrections during fabrication.

5. ACKNOWLEDGEMENTS

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6. REFERENCES

1. A. Glindemann, S. Hippler, T. Berkefeld, and W. Hackenberg, Experimental Astronomy volume 10, pp5-47, 2000

2. P. M. Furth, N. Clark, A Two Dimensional Poisson-Equation Solver Implemented in Analog VLSI, 7th NASA Symposium on VLSI Design, 1998

3. M.A. Vorontsov, G.W. Carhart, M.H. Cohen and G. Cauwenberghs,"Adaptive Optics based on analog parallel stochastic optimization: analysis and experimantal demonstration," J. Opt. Soc. Am. A, vol. 17, no. 8, 2000

4. Angel, J. R. 1994 Nature, 368, 203

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