175 GMACS/mW Charge-Mode Adiabatic Mixed-Signal Array Processor

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Abstract

An adiabatic charge-recycling mixed-signal array with integrated resonant clock generator delivers 175 GMACS (multiply-and-accumulates per second) throughput for every mW of power, a ten-fold improvement over the dynamic power incurred when resonant line drivers are replaced with CMOS drivers. The 3-T CID/DRAM cell provides non-destructive 1b-1b multiply accumulation, and integrated quantizers yield 8-bit outputs with +/- 1 LSB worst-case mismatch. The 256 × 512 four-quadrant array is embedded in a processor for template-based face detection.

Keywords: adiabatic, charge-recycling, matrix-vector multiplication, pattern recognition, mixed-signal and charge-mode.

Introduction

Energy efficiency of embedded signal processors sets limits on their maximum computational throughput and minimum power dissipation. The dynamic power of conventional digital circuits can be minimized by optimizing logic design, clock frequencies, supply voltage and threshold voltage, particularly in subthreshold [1]. Adiabatic circuits recycle energy, reducing power dissipation further below fCV^2. Adiabatic techniques have been successfully applied to certain types of circuits with large capacitive loads such as LCD drivers [2] and bus drivers [3]. Adiabatic microprocessors have also been reported [4, 5] and yield power gains of up to 7. We present an adiabatic charge-mode mixed-signal array processor for general purpose matrix operations delivering 175 GMACS computational throughput for every mW of power. This constitutes a 10-fold reduction in power dissipation in its resonant mode, compared to its already intrinsically low power when operating in static CMOS driver mode.

Architecture and Circuit Implementation

Fig. 1 depicts a simplified architecture of the array processor. The unit cell in the analog array combines a CID (charge injection device) computational element with a DRAM storage element. The cell stores one bit of a matrix element, performs a one-quadrant binary-binary multiplication and accumulates the result across cells in each row. An active charge transfer from M2 to M3 can only occur if there is non-zero charge stored, and if the potential on the gate of M3 rises above that of M2. The cell performs non-destructive computation since the transferred charge is sensed capacitively at the output. Once computation is performed the charge is shifted back into the DRAM cell. Capacitive coupling of all cells in a single row

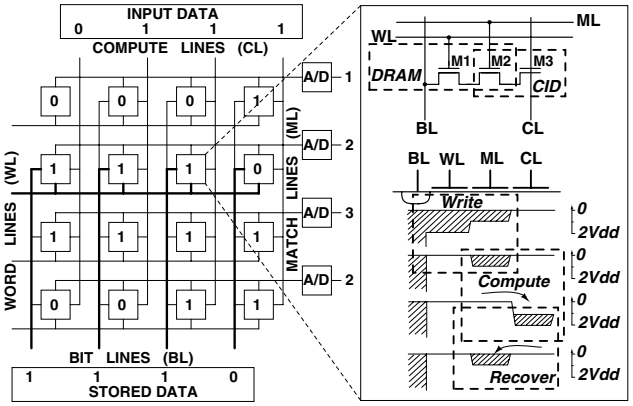


Fig. 1. Array processor architecture (left), circuit diagram of CID computational cell with integrated DRAM storage (right, top), and charge transfer diagram for active write and compute operations (right, bottom). A 1-bit binary data example is shown.

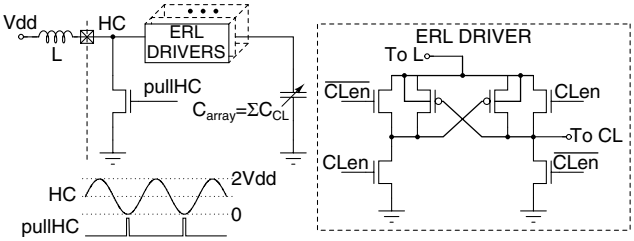


Fig. 2. Resonant clock generator for adiabatic power supply.

into a single match line (ML) implements zero-latency analog accumulation along each row. An array of cells thus performs analog multiplication of a binary matrix with a binary vector. The analog output vector is quantized by row-parallel oversampling ADCs to provide convenient digital output. The architecture easily extends to multi-bit data processing [6].

The computing array dissipates power only due to switching compute lines (CL). When compute lines are pulsed with a rectangular digital waveform the power dissipation is equal to $fC_{array}Vdd^2$. We utilize the charge shifted in the CID/DRAM cell to perform adiabatic computing on the full array as schematically shown in Fig. 2. An off-chip inductor is connected through an energy recovery logic (ERL) driver [5] to the capacitance of all active compute lines, C_{array}. The inductor is tuned such that the LC tank resonates when half of compute lines are switching. Due to resonance, much of the circuit power is derived from the LC, not from the DC power supply. Due to resistive losses the tank is supplied with external energy by pulsing $pullHC$ at the resonant frequency. Fig. 3 shows the block diagram of the array with signal paths for store, refresh, compute and charge recycle functions marked. The input shift register supplies both data to be stored as well as input data.

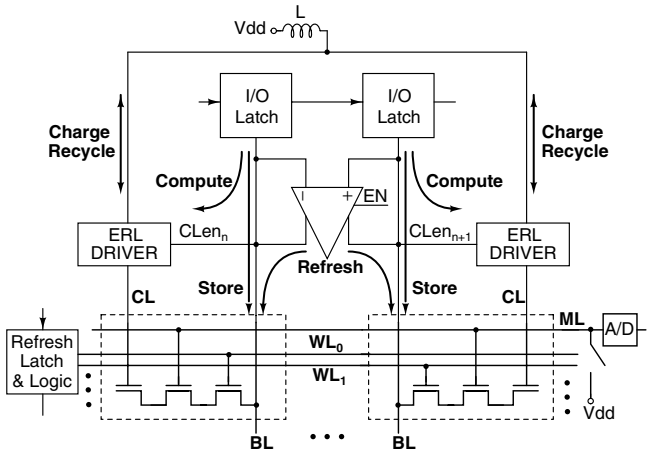
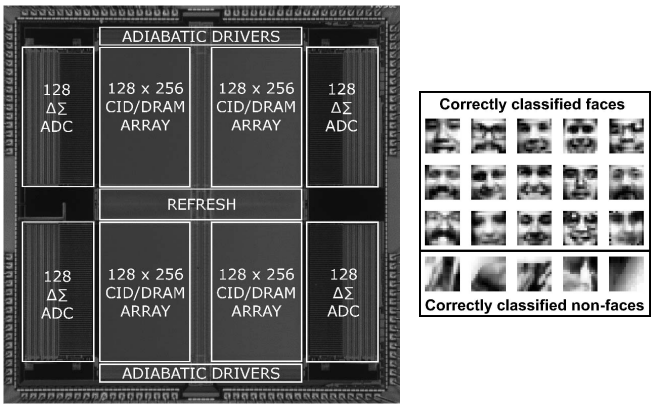


Fig. 3. Circuit diagram of functions peripheral to the cell including store, refresh and charge-recycling adiabatic compute.



(a) (b)

Fig. 4. (a) Chip micrograph and system floorplan; (b) face detection experimental results.

The data to be stored is loaded into the DRAM cell while the sense amplifier is disabled. It is then periodically refreshed after several compute cycles. In the compute cycle the input data enables adiabatic ERL drivers. They connect the off-chip inductance to the on-chip capacitance of active compute lines to enable charge recycling through resonance.

Experimental Results

A prototype mixed-signal array processor was integrated on a $4 \times 4\ \mathrm{mm}^2$ die and fabricated in 0.35 μm CMOS technology. The chip contains four computing arrays, each consisting of 128×256 CID/DRAM cells, and a row-parallel bank of 128 8-bit $\Delta\Sigma$ algorithmic ADCs [6]. Fig. 4(a) depicts the micrograph and system floorplan of the chip. Vertical folded bit lines (BL) extend across the array, with two rows of sense amplifiers at the top and bottom of the array. The refresh alternates between even and odd columns, with separate word lines (WL). All of the supporting digital clocks and control signals are generated on-chip. Experimentally measured row-to-row mismatch falls within +/- 1 LSB for over 97% of rows.

The array processor functionality has been validated in a real-time face detection application. A pattern recognition engine was trained on MIT CBCL face data set and programmed

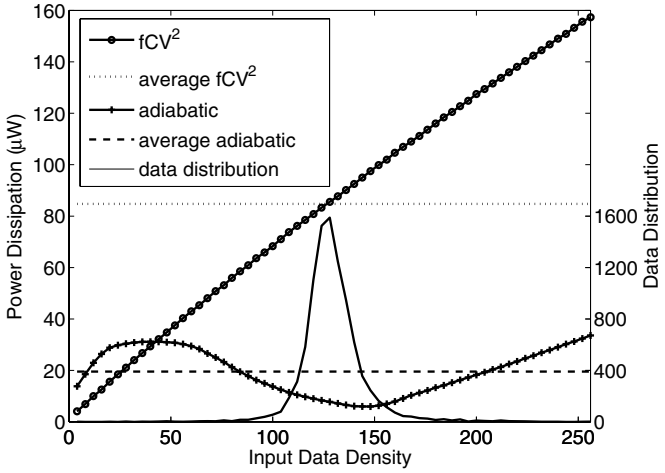


Fig. 5. Experimentally measured array power dissipation as a function of input data statistics, in adiabatic resonant mode and static CMOS mode.

on the processor with visual templates stored in DRAM. Classification performance on the test set is identical to emulation in software. Examples of classifications of faces and non-faces by the processor are given in Fig. 4(b). As only active compute lines are connected to the off-chip inductor, the capacitance of the LC tank depends on the data statistics. Fig. 5 shows power consumption of the CID/DRAM array in static CMOS driver mode and in adiabatic mode, both experimentally measured at 11.3 kHz computing frequency, as a function of input data density (number of logic-"1" bits in the input vector). We also plot data distribution of randomly sampled images from MIT CBCL face data set. Most of natural scene images have equal probability of ones and zeros resulting in normal distribution. It can be observed that the resonant frequency is tuned for the 50% data density with 8.25 μW minimum power dissipation. This corresponds to 10-fold reduction in power dissipation over fCV^2 power. At 11.3 kHz frequency the processor performs 128×256 binary multiply-and-accumulate operations on each of the four arrays corresponding to 1.45 GMACS computational throughput, yielding energy efficiency of 175 GMACS/mW.

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